

MOSFET – Power, Single, N-Channel

40 V, 4.9 mΩ, 70 A

NVD5C460N

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	40	V
Gate-to-Source Voltage			V _{GS}	± 20	V
Continuous Drain Current R _{θJC} (Notes 1 & 3)	Steady State	T _C = 25 °C	I _D	70	A
		T _C = 100 °C		50	
Power Dissipation R _{θJC} (Note 1)		T _C = 25 °C	P _D	47	W
		T _C = 100 °C		23	
Continuous Drain Current R _{θJA} (Notes 1, 2 & 3)	Steady State	T _A = 25 °C	I _D	18	A
		T _A = 100 °C		13	
Power Dissipation R _{θJA} (Notes 1 & 2)		T _A = 25 °C	P _D	3.0	W
		T _A = 100 °C		1.5	
Pulsed Drain Current	T _A = 25 °C, t _p = 10 μs		I _{DM}	379	A
Operating Junction and Storage Temperature			T _J , T _{stg}	–55 to 175	°C
Source Current (Body Diode)			I _S	39	A
Single Pulse Drain-to-Source Avalanche Energy (T _J = 25 °C, I _{L(pk)} = 6.5 A)			E _{AS}	147	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T _L	260	°C

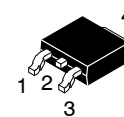
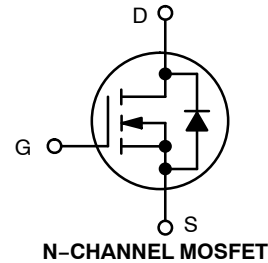
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain) (Note 1)	$R_{\theta JC}$	3.2	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	48.6	

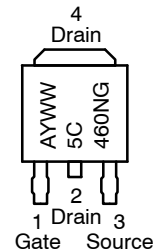
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(on)}$	I_D
40 V	4.9 mΩ @ 10 V	70 A



DPAK3
CASE 369C
STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENT



- A = Assembly Location
 Y = Year
 WW = Work Week
 5C460N = Device Code
 G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NVD5C460N

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			20		mV/ $^{\circ}\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}$	$T_J = 25\text{ }^{\circ}\text{C}$		10	μA
			$T_J = 125\text{ }^{\circ}\text{C}$		250	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 60\text{ }\mu\text{A}$	2.0		4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			6.8		mV/ $^{\circ}\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 25\text{ A}$		4.2	4.9	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = 3\text{ V}, I_D = 25\text{ A}$		62		S

CHARGES, CAPACITANCES AND GATE RESISTANCES

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 25\text{ V}$		1600		pF
Output Capacitance	C_{oss}			800		
Reverse Transfer Capacitance	C_{rss}			38		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 32\text{ V}, I_D = 25\text{ A}$		26		nC
Threshold Gate Charge	$Q_{G(TH)}$			4.7		
Gate-to-Source Charge	Q_{GS}			7.5		
Gate-to-Drain Charge	Q_{GD}			5.1		
Plateau Voltage	V_{GP}			4.6		V

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DS} = 32\text{ V}, I_D = 25\text{ A}, R_G = 2.5\text{ }\Omega$		11		ns
Rise Time	t_r			27		
Turn-Off Delay Time	$t_{d(off)}$			21		
Fall Time	t_f			5		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 25\text{ A}$	$T_J = 25\text{ }^{\circ}\text{C}$		0.85	1.2	V
			$T_J = 125\text{ }^{\circ}\text{C}$		0.73		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 25\text{ A}$		30			ns
Charge Time	t_a			15			
Discharge Time	t_b			15			
Reverse Recovery Charge	Q_{RR}			10			nC

4. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

5. Switching characteristics are independent of operating junction temperatures.



TYPICAL CHARACTERISTICS

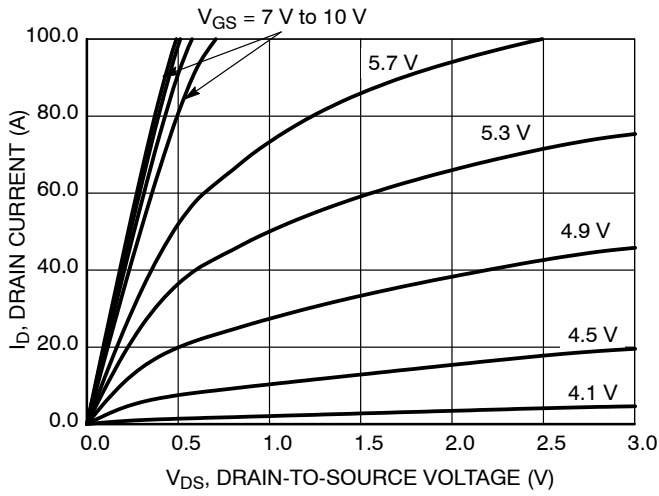


Figure 1. On-Region Characteristics

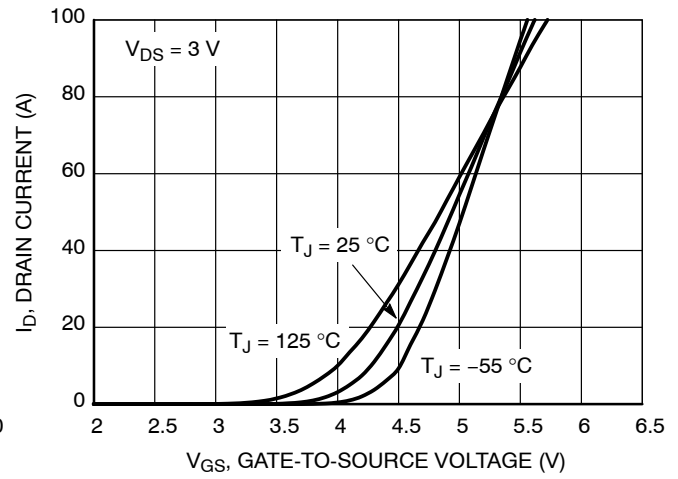


Figure 2. Transfer Characteristics

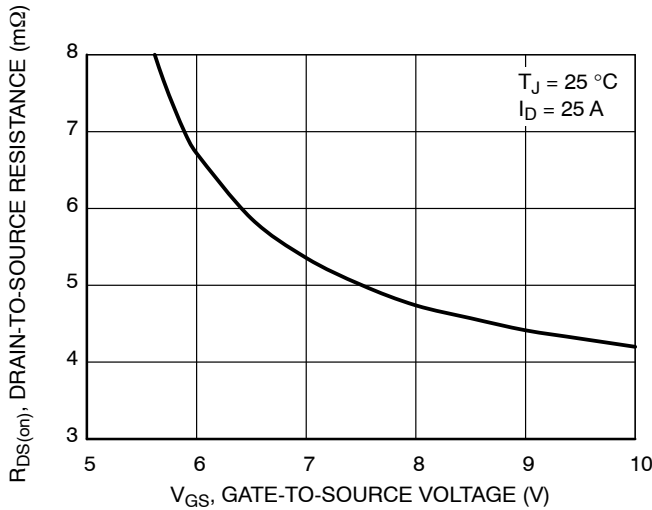


Figure 3. On-Resistance vs. Gate-to-Source Voltage

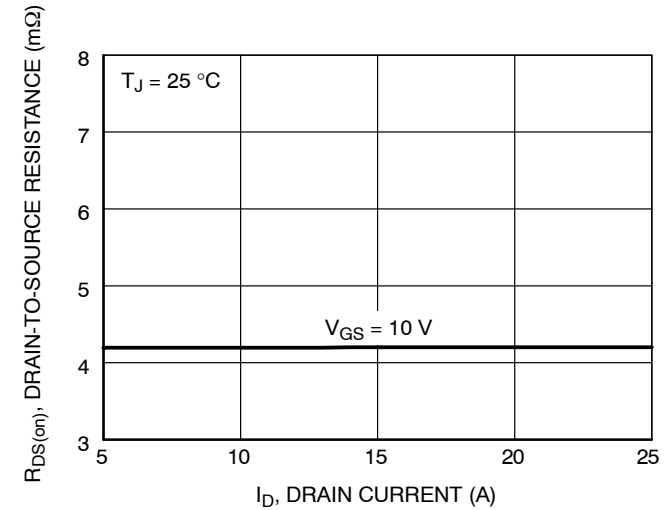


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

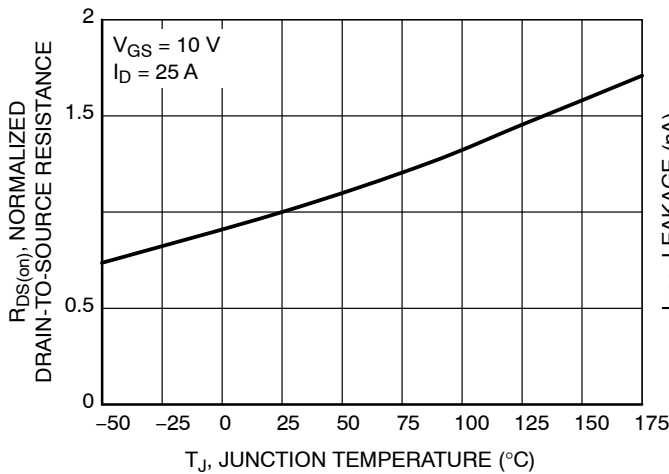


Figure 5. On-Resistance Variation with Temperature

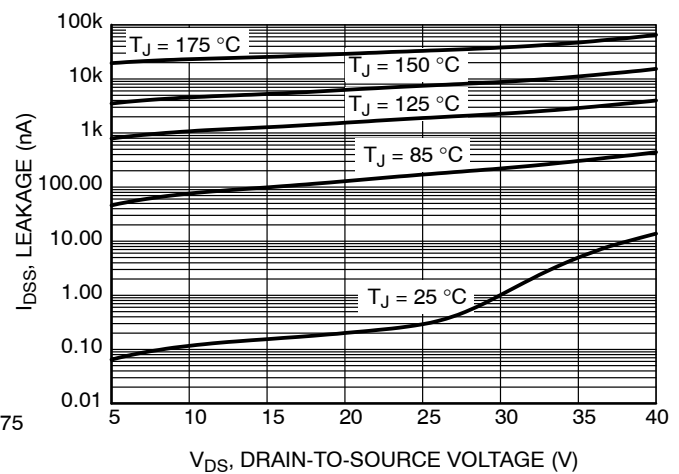


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

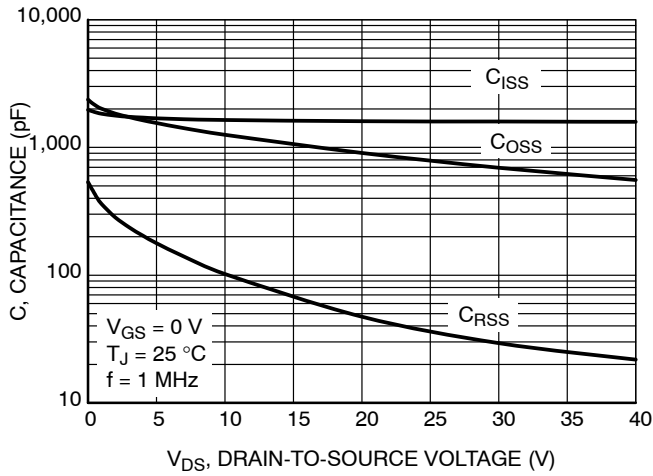


Figure 7. Capacitance Variation

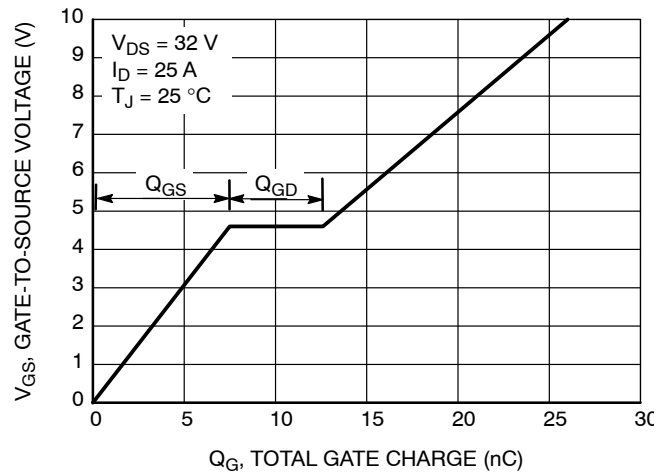


Figure 8. Gate-to-Source vs. Total Charge

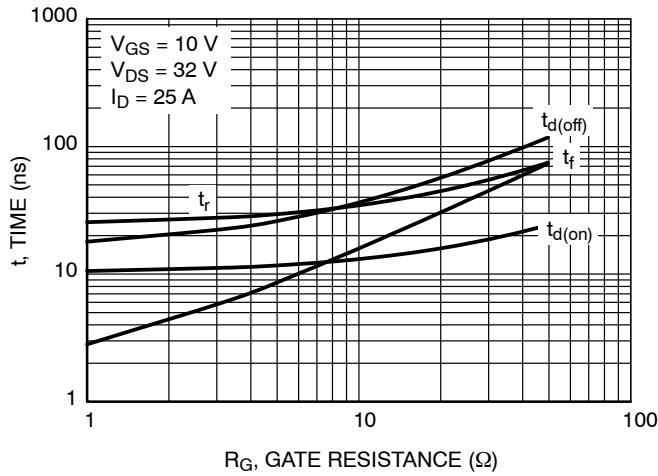


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

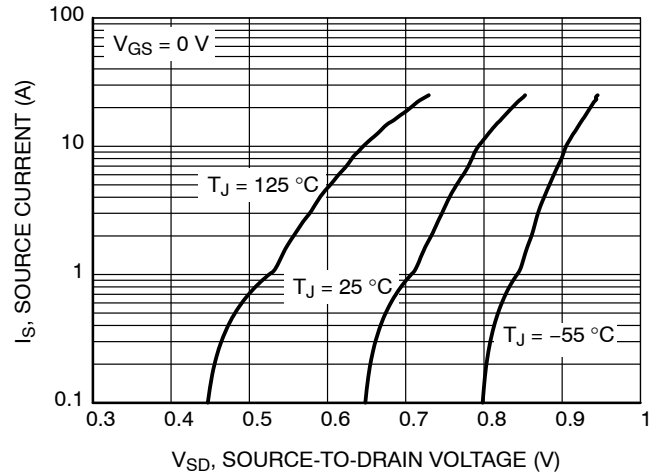


Figure 10. Diode Forward Voltage vs. Current

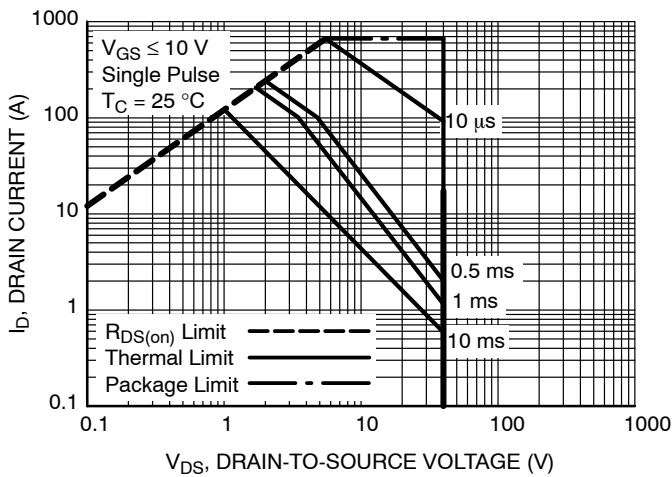


Figure 11. Maximum Rated Forward Biased Safe Operating Area

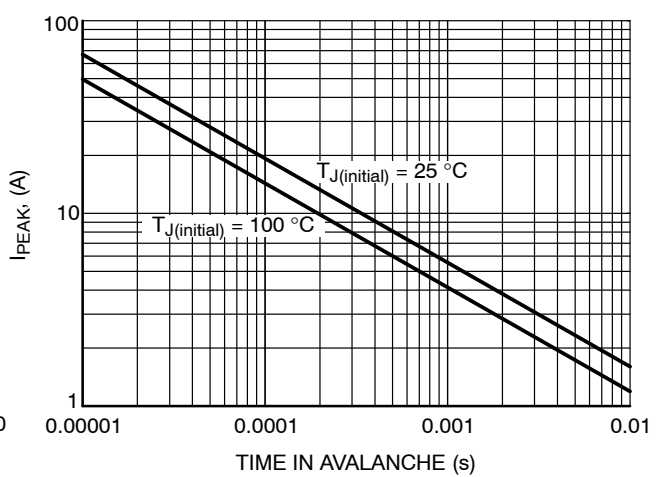


Figure 12. Maximum Drain Current vs. Time in Avalanche

NVD5C460N

TYPICAL CHARACTERISTICS

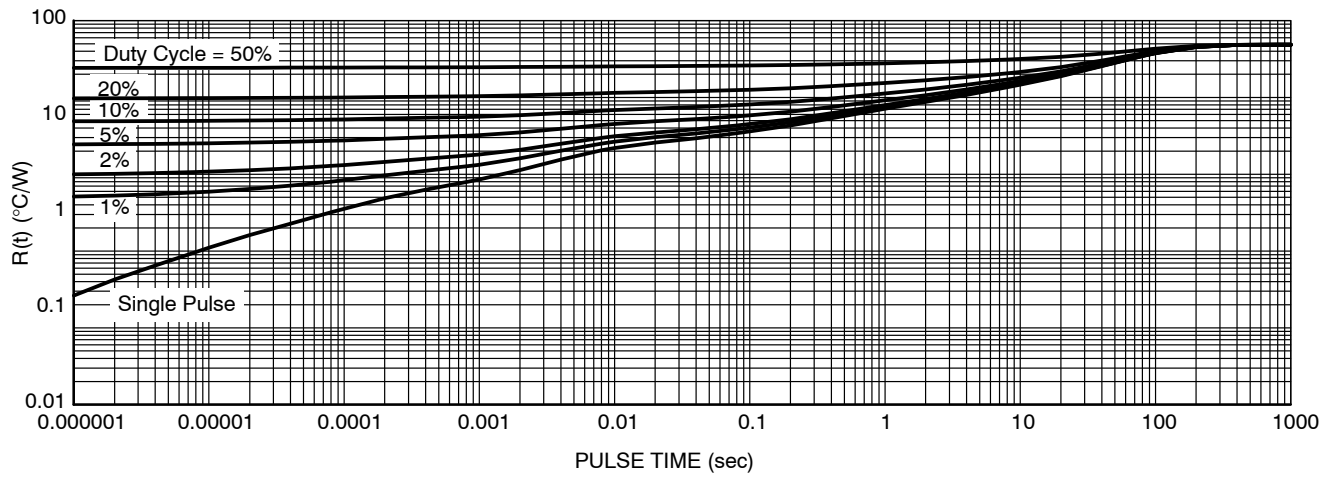


Figure 13. Thermal Response

ORDERING INFORMATION

Order Number	Package	Shipping [†]
NVD5C460NT4G	DPAK3 (Pb-Free)	2500 / Tape & Reel

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).



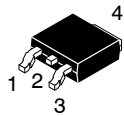
NVD5C460N

REVISION HISTORY

Revision	Description of Changes	Date
1	Document rebranded to onsemi format.	10/3/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

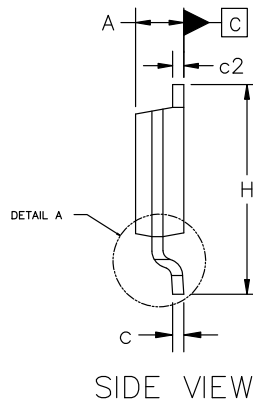
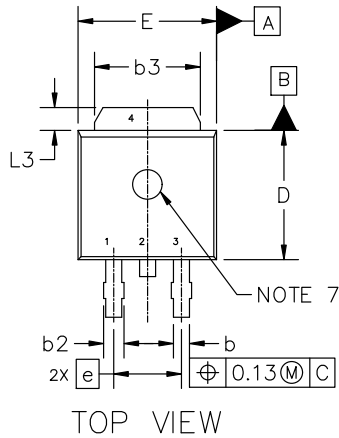




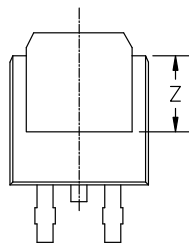
DPAK-3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE K

DATE 14 MAY 2026

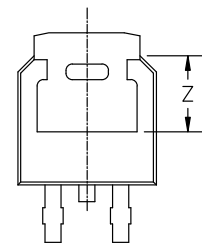
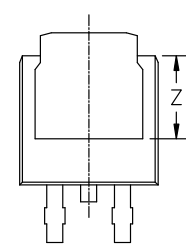
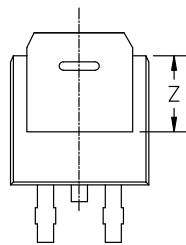
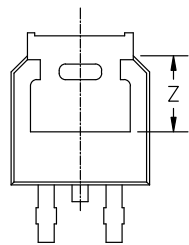
SCALE 1:1



MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---



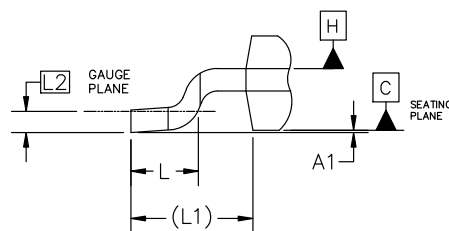
BOTTOM VIEW



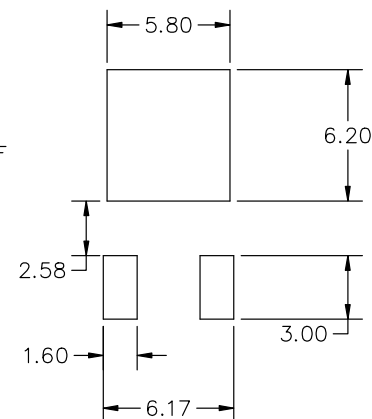
ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



DETAIL A
ROTATED 90° CW



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

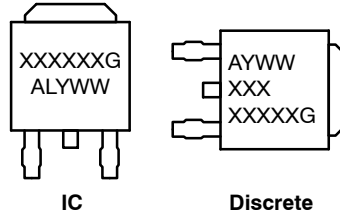
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**DPAK–3 6.10x6.54x2.28, 2.29P
 CASE 369C
 ISSUE K**

DATE 13 MAY 2026

**GENERIC
MARKING DIAGRAM***



XXXXXX = Device Code
 A = Assembly Location
 L = Wafer Lot
 Y = Year
 WW = Work Week
 G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 3: PIN 1. ANODE 2. CATHODE 3. ANODE 4. CATHODE	STYLE 4: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE	STYLE 5: PIN 1. GATE 2. ANODE 3. CATHODE 4. ANODE
STYLE 6: PIN 1. MT1 2. MT2 3. GATE 4. MT2	STYLE 7: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 8: PIN 1. N/C 2. CATHODE 3. ANODE 4. CATHODE	STYLE 9: PIN 1. ANODE 2. CATHODE 3. RESISTOR ADJUST 4. CATHODE	STYLE 10: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. ANODE

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