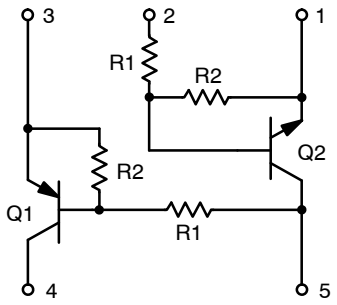
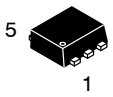
# Dual Common Base-Collector Bias Resistor Transistors

## NPN and PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

# EMC2DXV5T1G, EMC3DXV5T1G, EMC4DXV5T1G, EMC5DXV5T1G




**SOT−553**
**CASE 463B**

The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base−emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the EMC2DXV5T1G series, two complementary BRT devices are housed in the SOT−553 package which is ideal for low power surface mount applications where board space is at a premium.

### Features

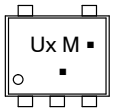
- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These are Pb−Free Devices

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted, common for $Q_1$ and $Q_2$, − minus sign for $Q_1$ (PNP) omitted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Collector-Base Voltage | $V_{CBO}$ | 50 | Vdc |
| Collector-Emitter Voltage | $V_{CEO}$ | 50 | Vdc |
| Collector Current | $I_C$ | 100 | mAdc |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### MARKING DIAGRAM




Ux = Specific Device Code
x = C, 3, E, or 5
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 2.

## THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| **ONE JUNCTION HEATED** | | | |
| Total Device Dissipation<br>$T_A$ = 25°C<br>Derate above 25°C | $P_D$ | <br>357 (Note 1)<br>2.9 (Note 1) | <br>mW<br>mW/°C |
| Thermal Resistance, Junction-to-Ambient | $R_{\theta JA}$ | 350 (Note 1) | °C/W |
| **BOTH JUNCTIONS HEATED** | | | |
| Total Device Dissipation<br>$T_A$ = 25°C<br>Derate above 25°C | $P_D$ | <br>500 (Note 1)<br>4.0 (Note 1) | <br>mW<br>mW/°C |
| Thermal Resistance, Junction-to-Ambient | $R_{\theta JA}$ | 250 (Note 1) | °C/W |
| Junction and Storage Temperature | $T_J$, $T_{stg}$ | −55 to +150 | °C |

1. FR−4 @ Minimum Pad

## DEVICE ORDERING INFORMATION, MARKING AND RESISTOR VALUES

| Device | Marking | Transistor 1 − PNP | | Transistor 2 − NPN | | Package | Shipping† |
|---|---|---|---|---|---|---|---|
| | | R1 (K) | R2 (K) | R1 (K) | R2 (K) | | |
| EMC2DXV5T1G | UC | 22 | 22 | 22 | 22 | SOT−553<br>(Pb−Free) | 4000 / Tape & Reel |
| NSVEMC2DXV5T1G* | UC | 22 | 22 | 22 | 22 | | 4000 / Tape & Reel |
| EMC3DXV5T1G | U3 | 10 | 10 | 10 | 10 | | 4000 / Tape & Reel |
| EMC5DXV5T1G | U5 | 4.7 | 10 | 47 | 47 | | 4000 / Tape & Reel |
| **DISCONTINUED** (Note 2) | | | | | | | |
| EMC3DXV5T5G | U3 | 10 | 10 | 10 | 10 | SOT−553<br>(Pb−Free) | 8000 / Tape & Reel |
| EMC4DXV5T1G | UE | 10 | 47 | 47 | 47 | | 4000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable.

2. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

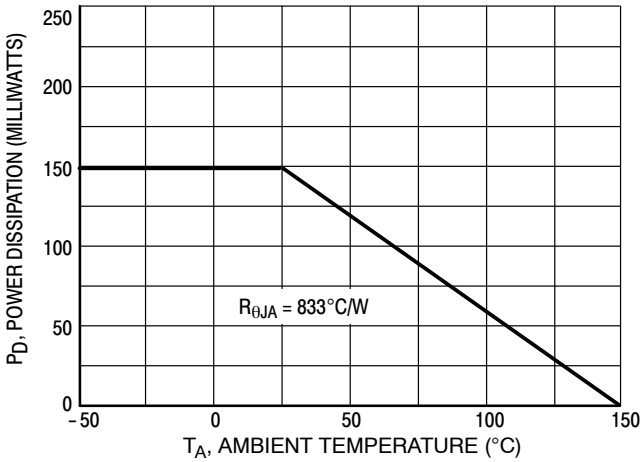



**Figure 1. Derating Curve**

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Q1 TRANSISTOR: PNP**<br>**OFF CHARACTERISTICS** | | | | | | |
| Collector-Base Cutoff Current ($V_{CB}$ = 50 V, $I_E$ = 0) | | $I_{CBO}$ | – | – | 100 | nAdc |
| Collector-Emitter Cutoff Current ($V_{CB}$ = 50 V, $I_B$ = 0) | | $I_{CEO}$ | – | – | 500 | nAdc |
| Emitter-Base Cutoff Current ($V_{EB}$ = 6.0 V, $I_C$ = 0) | EMC2DXV5T1G<br>EMC3DXV5T1G<br>EMC4DXV5T1G<br>EMC5DXV5T1G | $I_{EBO}$ | –<br>–<br>–<br>– | –<br>–<br>–<br>– | 0.2<br>0.5<br>0.2<br>1.0 | mAdc |
| **ON CHARACTERISTICS** | | | | | | |
| Collector-Base Breakdown Voltage ($I_C$ = 10 μA, $I_E$ = 0) | | $V_{(BR)CBO}$ | 50 | – | – | Vdc |
| Collector-Emitter Breakdown Voltage ($I_C$ = 2.0 mA, $I_B$ = 0) | | $V_{(BR)CEO}$ | 50 | – | – | Vdc |
| DC Current Gain ($V_{CE}$ = 10 V, $I_C$ = 5.0 mA) | EMC2DXV5T1G<br>EMC3DXV5T1G<br>EMC4DXV5T1G<br>EMC5DXV5T1G | $h_{FE}$ | 60<br>35<br>80<br>20 | 100<br>60<br>140<br>35 | –<br>–<br>–<br>– | |
| Collector–Emitter Saturation Voltage ($I_C$ = 10 mA, $I_B$ = 0.3 mA) | | $V_{CE(SAT)}$ | – | – | 0.25 | Vdc |
| Output Voltage (on) ($V_{CC}$ = 5.0 V, $V_B$ = 2.5 V, $R_L$ = 1.0 kΩ) | | $V_{OL}$ | – | – | 0.2 | Vdc |
| Output Voltage (off) ($V_{CC}$ = 5.0 V, $V_B$ = 0.5 V, $R_L$ = 1.0 kΩ) | | $V_{OH}$ | 4.9 | – | – | Vdc |
| Input Resistor | EMC2DXV5T1G<br>EMC3DXV5T1G, EMC4DXV5T1G<br>EMC5DXV5T1G | R1 | 15.4<br>7.0<br>3.3 | 22<br>10<br>4.7 | 28.6<br>13<br>6.1 | kΩ |
| Resistor Ratio | EMC2DXV5T1G<br>EMC3DXV5T1G<br>EMC4DXV5T1G<br>EMC5DXV5T1G | R1/R2 | 0.8<br>0.8<br>0.17<br>0.38 | 1.0<br>1.0<br>0.21<br>0.47 | 1.2<br>1.2<br>0.25<br>0.56 | |
| **Q2 TRANSISTOR: NPN**<br>**OFF CHARACTERISTICS** | | | | | | |
| Collector-Base Cutoff Current ($V_{CB}$ = 50 V, $I_E$ = 0) | | $I_{CBO}$ | – | – | 100 | nAdc |
| Collector-Emitter Cutoff Current ($V_{CB}$ = 50 V, $I_B$ = 0) | | $I_{CEO}$ | – | – | 500 | nAdc |
| Emitter-Base Cutoff Current ($V_{EB}$ = 6.0 V, $I_C$ = 0) | EMC2DXV5T1G<br>EMC3DXV5T1G<br>EMC4DXV5T1G, EMC5DXV5T1G | $I_{EBO}$ | –<br>–<br>– | –<br>–<br>– | 0.2<br>0.5<br>0.1 | mAdc |
| **ON CHARACTERISTICS** | | | | | | |
| Collector-Base Breakdown Voltage ($I_C$ = 10 μA, $I_E$ = 0) | | $V_{(BR)CBO}$ | 50 | – | – | Vdc |
| Collector-Emitter Breakdown Voltage ($I_C$ = 2.0 mA, $I_B$ = 0) | | $V_{(BR)CEO}$ | 50 | – | – | Vdc |
| DC Current Gain ($V_{CE}$ = 10 V, $I_C$ = 5.0 mA) | EMC2DXV5T1G<br>EMC3DXV5T1G<br>EMC4DXV5T1G, EMC5DXV5T1G | $h_{FE}$ | 60<br>35<br>80 | 100<br>60<br>140 | –<br>–<br>– | |
| Collector–Emitter Saturation Voltage ($I_C$ = 10 mA, $I_B$ = 0.3 mA) | | $V_{CE(SAT)}$ | – | – | 0.25 | Vdc |
| Output Voltage (on) ($V_{CC}$ = 5.0 V, $V_B$ = 2.5 V, $R_L$ = 1.0 kΩ) | | $V_{OL}$ | – | – | 0.2 | Vdc |
| Output Voltage (off) ($V_{CC}$ = 5.0 V, $V_B$ = 0.5 V, $R_L$ = 1.0 kΩ) | | $V_{OH}$ | 4.9 | – | – | Vdc |
| Input Resistor | EMC2DXV5T1G<br>EMC3DXV5T1G<br>EMC4DXV5T1G, EMC5DXV5T1G | R1 | 15.4<br>7.0<br>33 | 22<br>10<br>47 | 28.6<br>13<br>61 | kΩ |
| Resistor Ratio | EMC2DXV5T1G<br>EMC3DXV5T1G<br>EMC4DXV5T1G, EMC5DXV5T1G | R1/R2 | 0.8<br>0.8<br>0.8 | 1.0<br>1.0<br>1.0 | 1.2<br>1.2<br>1.2 | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## TYPICAL ELECTRICAL CHARACTERISTICS – EMC2DXV5T1 PNP TRANSISTOR

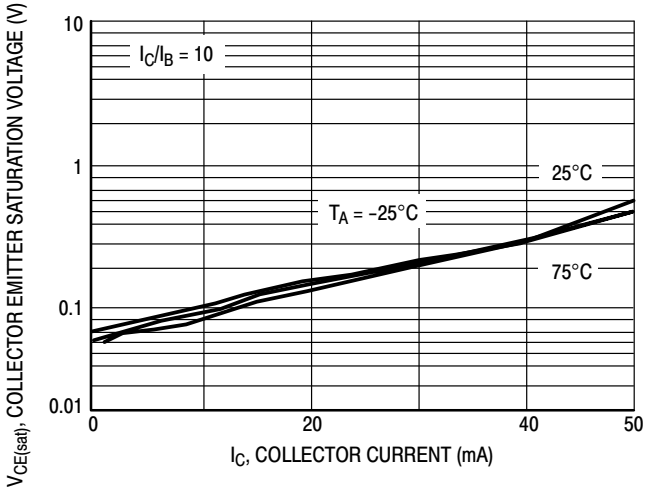



**Figure 2. $V_{CE(sat)}$ versus $I_C$**

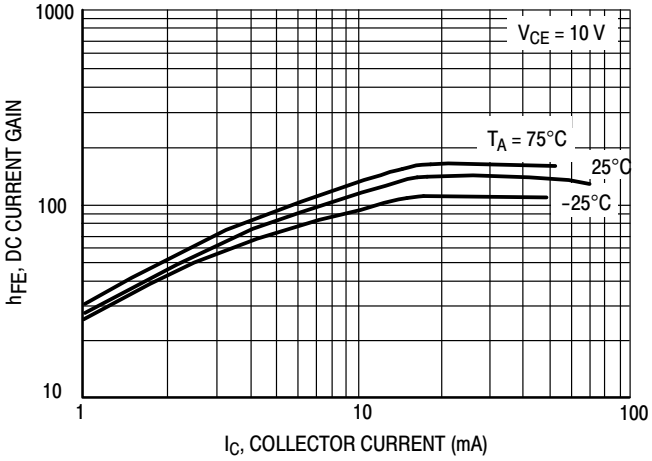



**Figure 3. DC Current Gain**

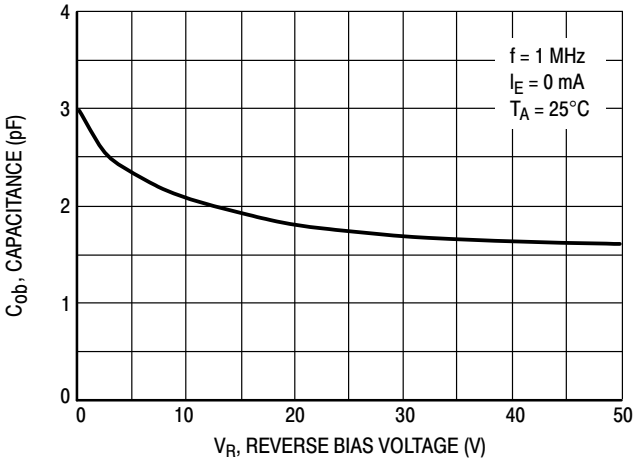



**Figure 4. Output Capacitance**

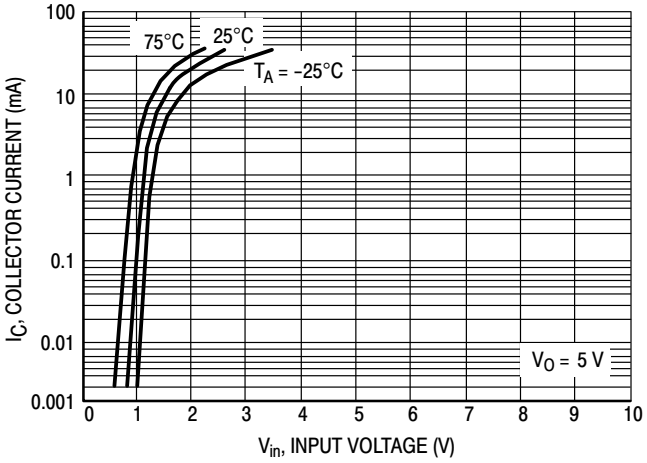



**Figure 5. Output Current versus Input Voltage**

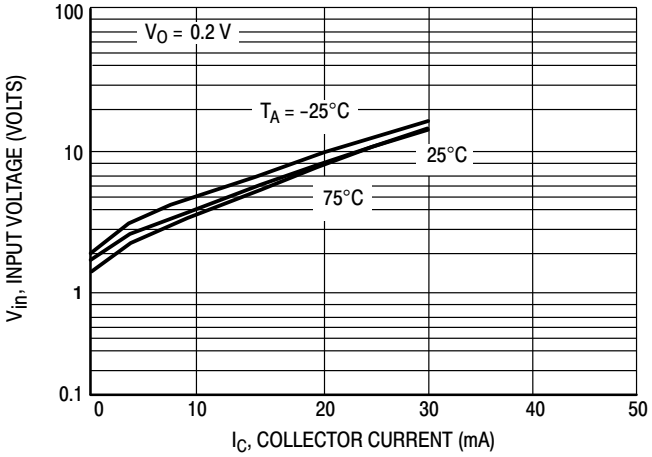



**Figure 6. Input Voltage versus Output Current**

## TYPICAL ELECTRICAL CHARACTERISTICS – EMC2DXV5T1 NPN TRANSISTOR

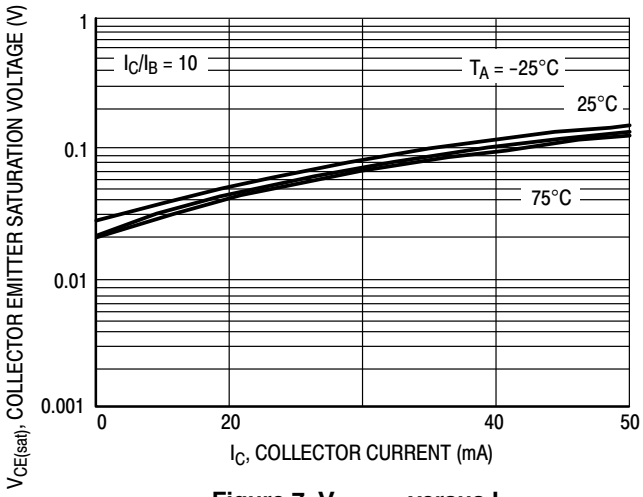



**Figure 7. $V_{CE(sat)}$ versus $I_C$**

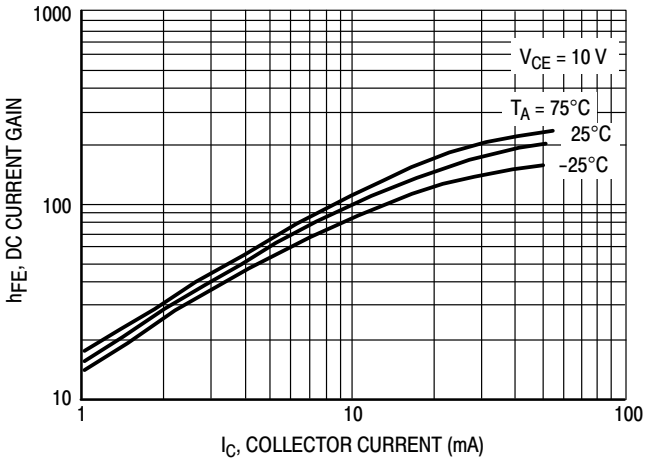



**Figure 8. DC Current Gain**

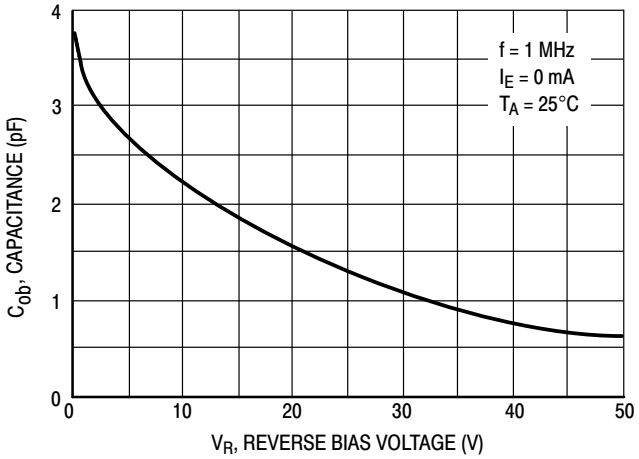



**Figure 9. Output Capacitance**

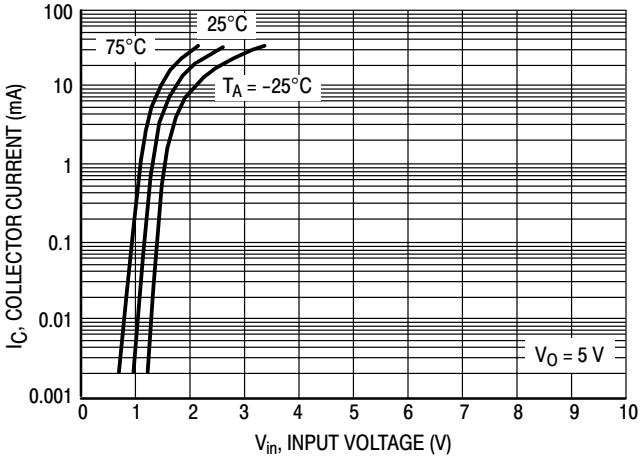



**Figure 10. Output Current versus Input Voltage**

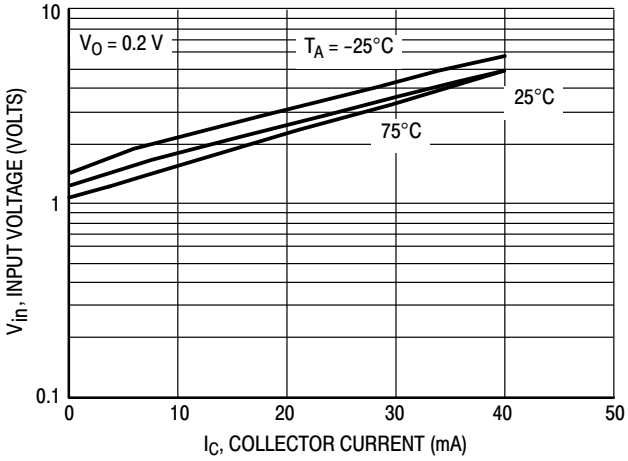



**Figure 11. Input Voltage versus Output Current**

## TYPICAL ELECTRICAL CHARACTERISTICS – EMC3DXV5T1 PNP TRANSISTOR

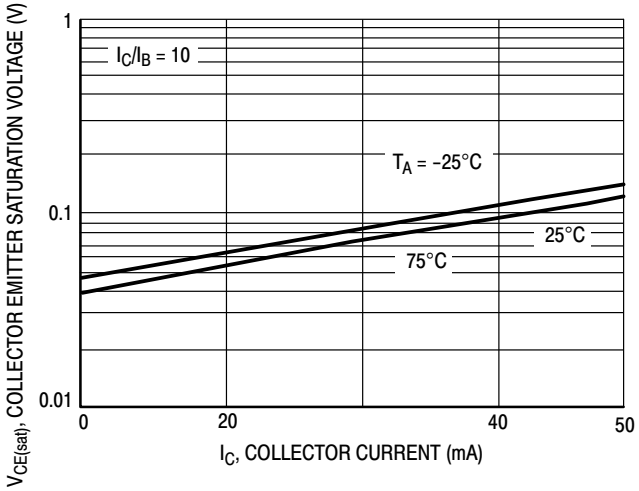



**Figure 12. $V_{CE(sat)}$ versus $I_C$**

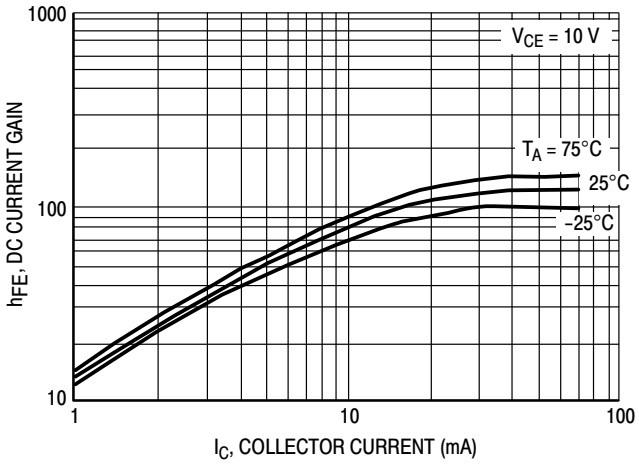



**Figure 13. DC Current Gain**

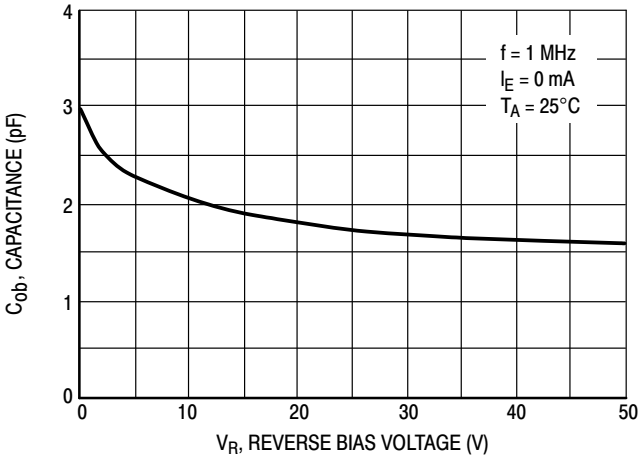



**Figure 14. Output Capacitance**

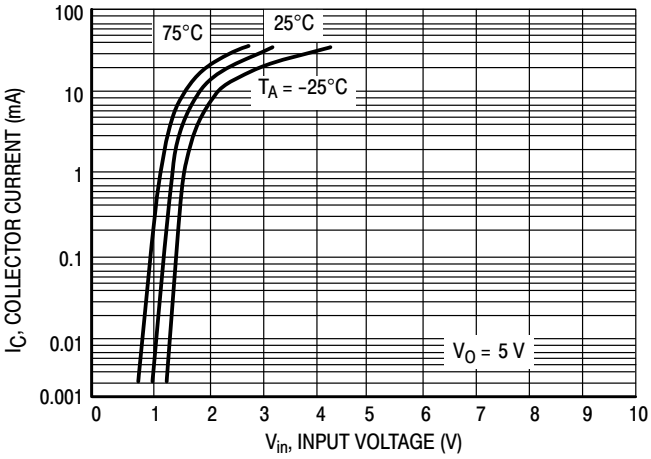



**Figure 15. Output Current versus Input Voltage**

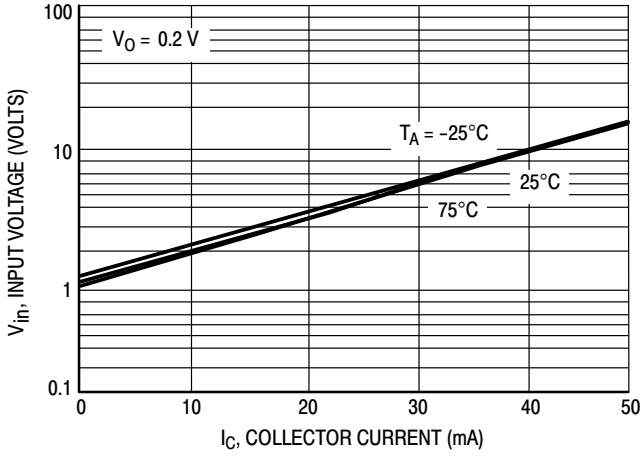



**Figure 16. Input Voltage versus Output Current**

## TYPICAL ELECTRICAL CHARACTERISTICS – EMC3DXV5T1 NPN TRANSISTOR

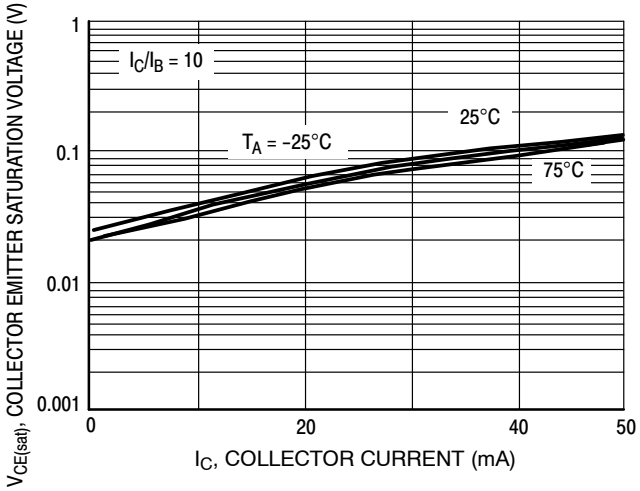



**Figure 17. $V_{CE(sat)}$ versus $I_C$**

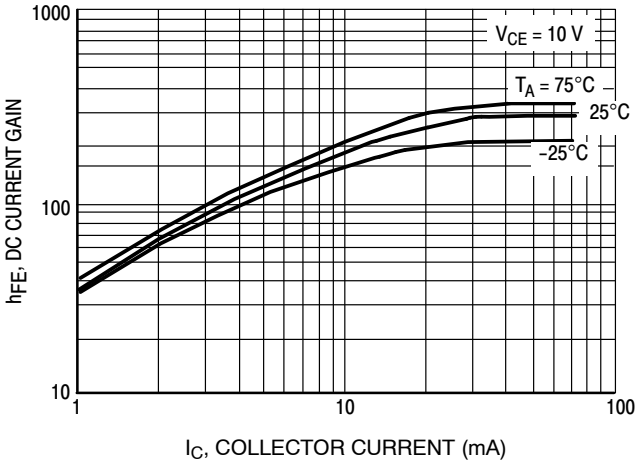



**Figure 18. DC Current Gain**

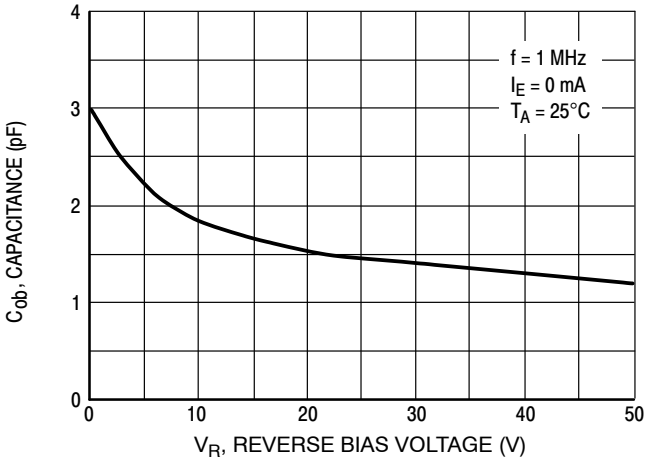



**Figure 19. Output Capacitance**

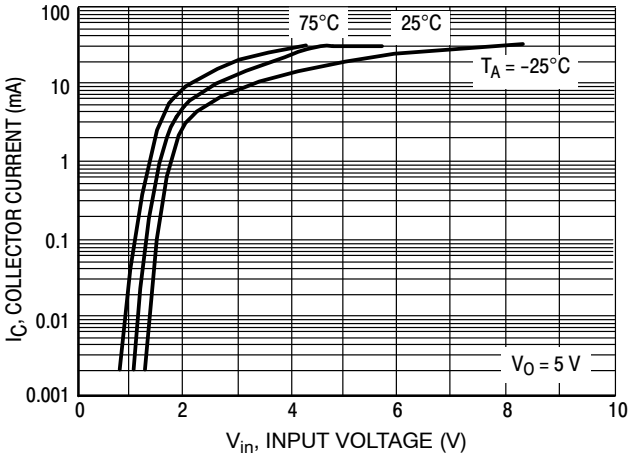



**Figure 20. Output Current versus Input Voltage**

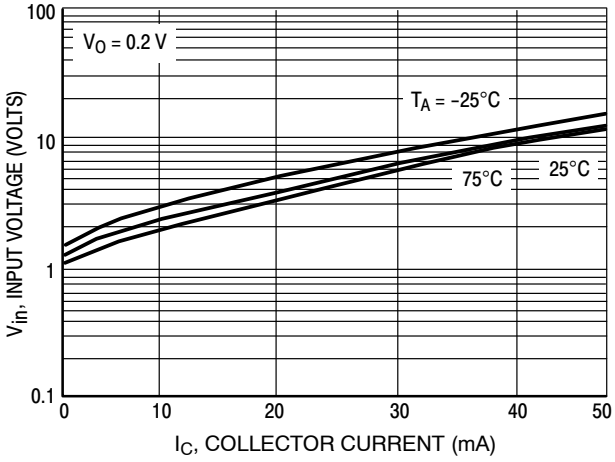



**Figure 21. Input Voltage versus Output Current**

## TYPICAL ELECTRICAL CHARACTERISTICS –EMC4DXV5T1 PNP TRANSISTOR

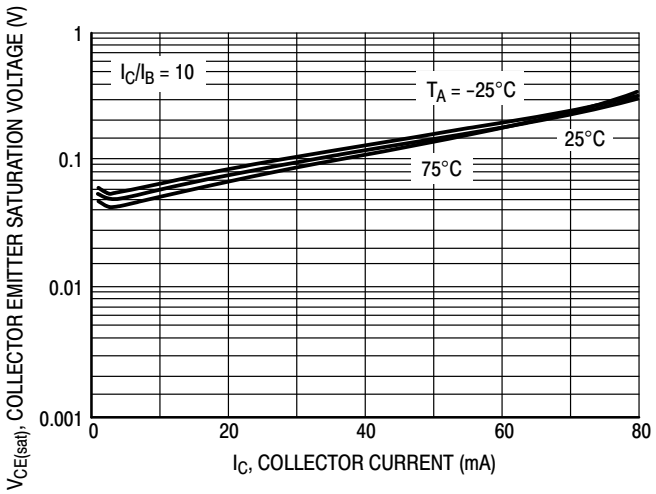



**Figure 22. $V_{CE(sat)}$ versus $I_C$**

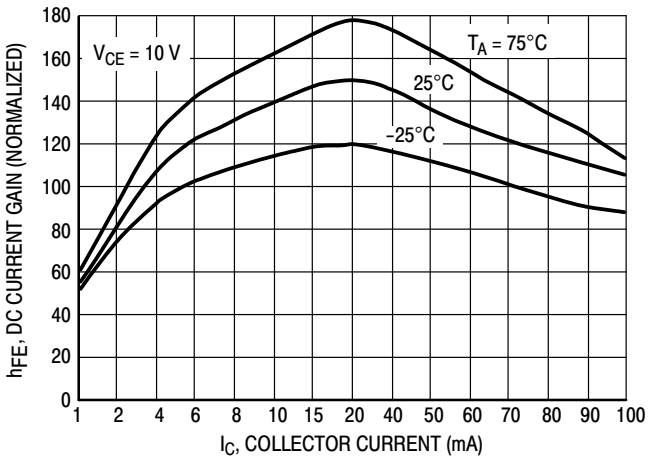



**Figure 23. DC Current Gain**

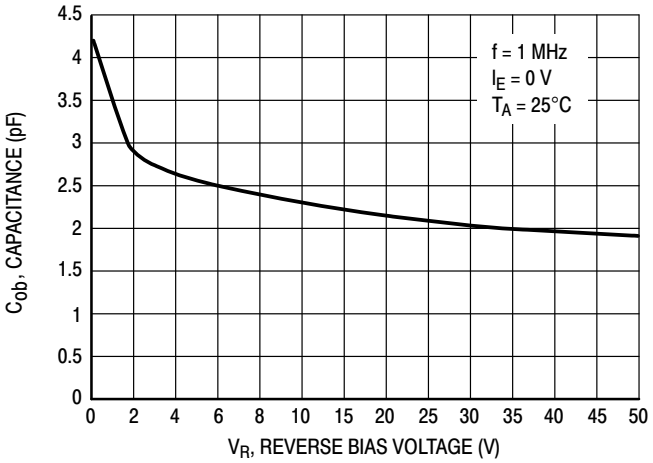



**Figure 24. Output Capacitance**

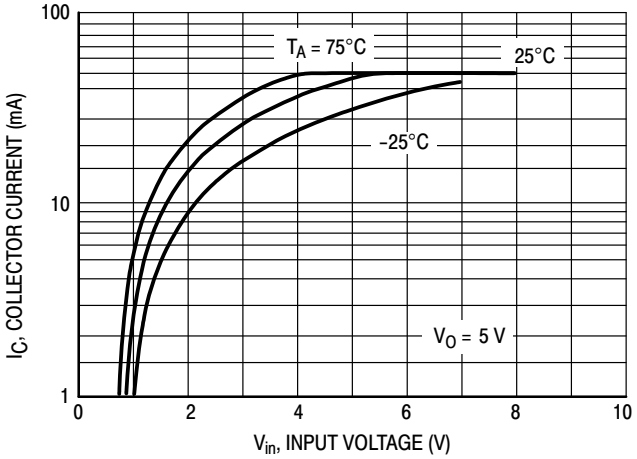



**Figure 25. Output Current versus Input Voltage**

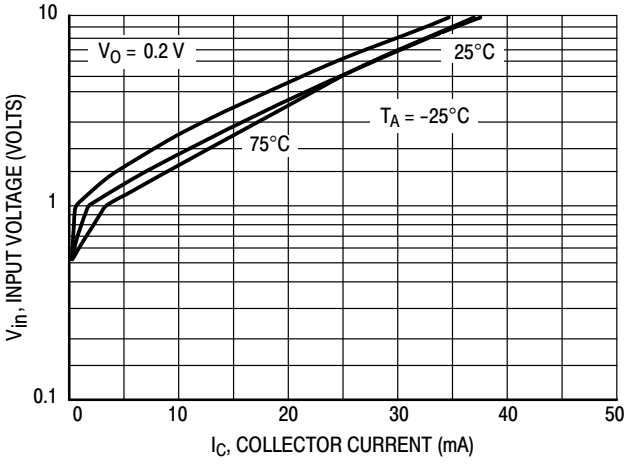



**Figure 26. Input Voltage versus Output Current**

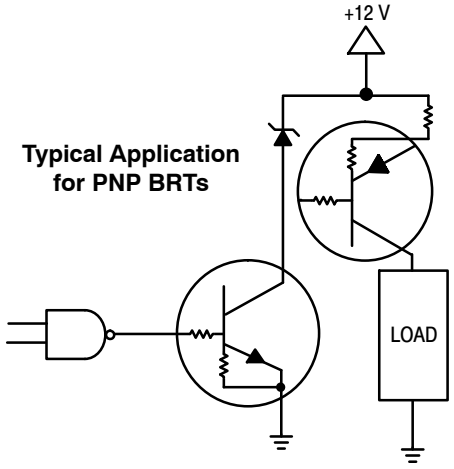



**Figure 27. Inexpensive, Unregulated Current Source**

## TYPICAL ELECTRICAL CHARACTERISTICS – EMC5DXV5T1 PNP TRANSISTOR

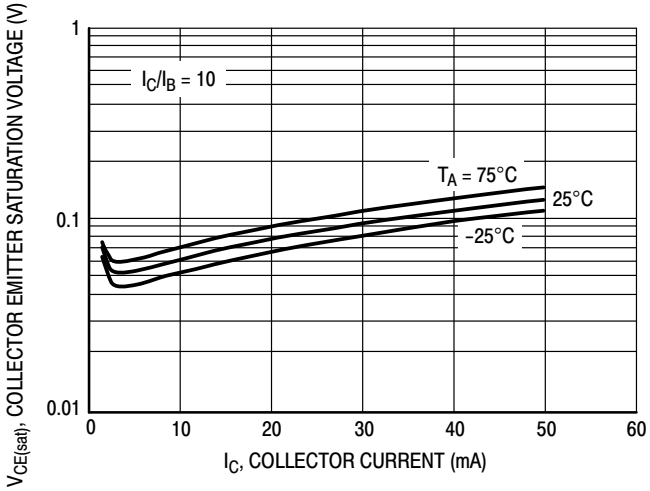



**Figure 28. $V_{CE(sat)}$ versus $I_C$**

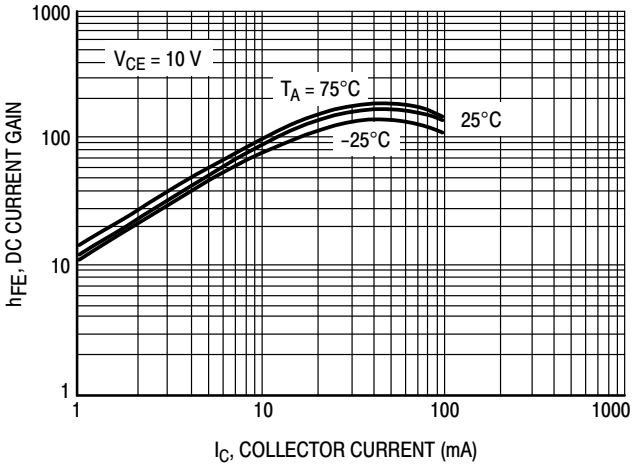



**Figure 29. DC Current Gain**

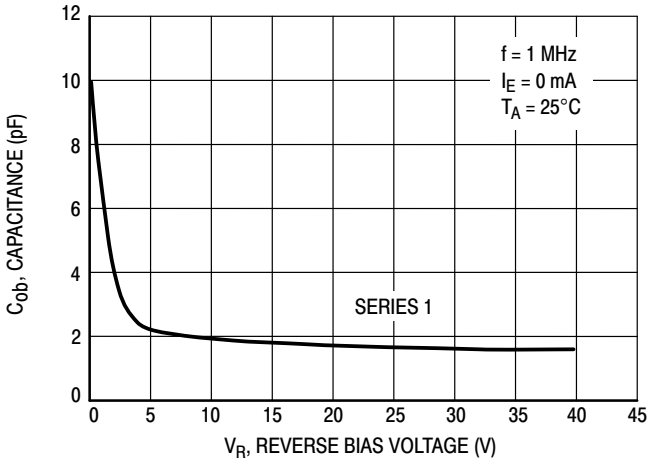



**Figure 30. Output Capacitance**

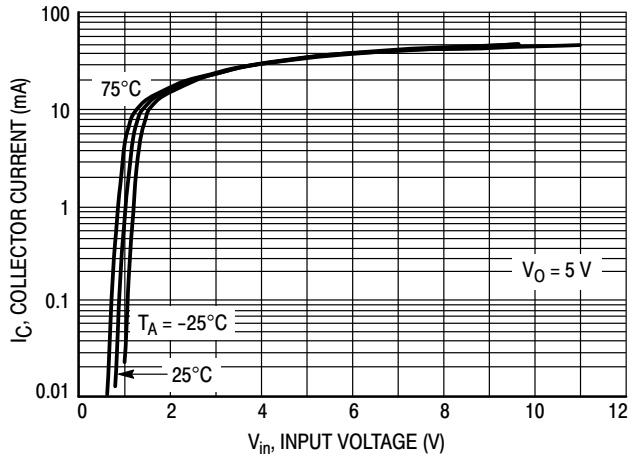



**Figure 31. Output Current versus Input Voltage**

## TYPICAL ELECTRICAL CHARACTERISTICS – EMC4DXV5T1, EMC5DXV5T1 NPN TRANSISTOR

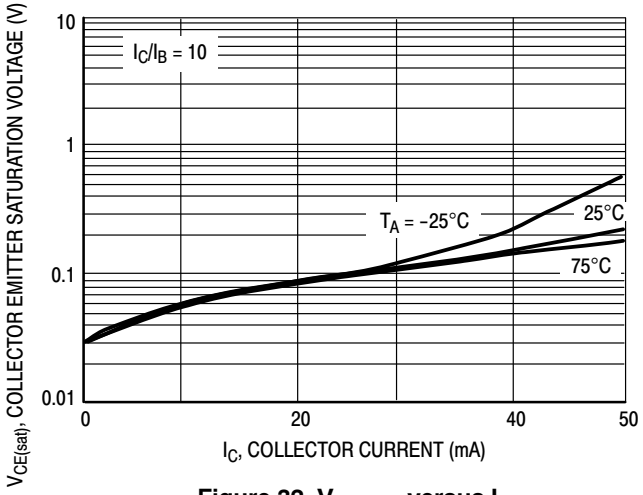



**Figure 32. $V_{CE(sat)}$ versus $I_C$**

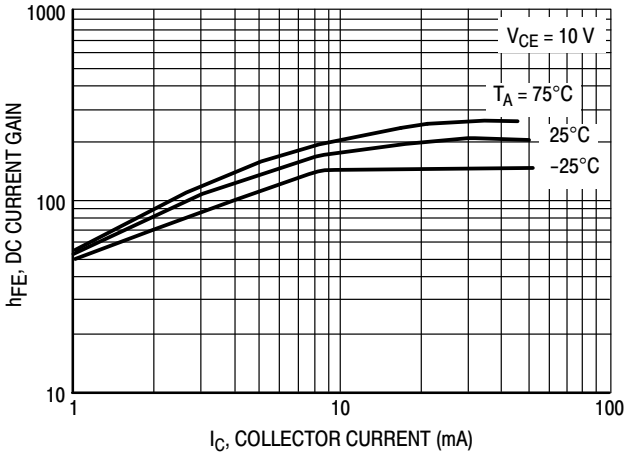



**Figure 33. DC Current Gain**

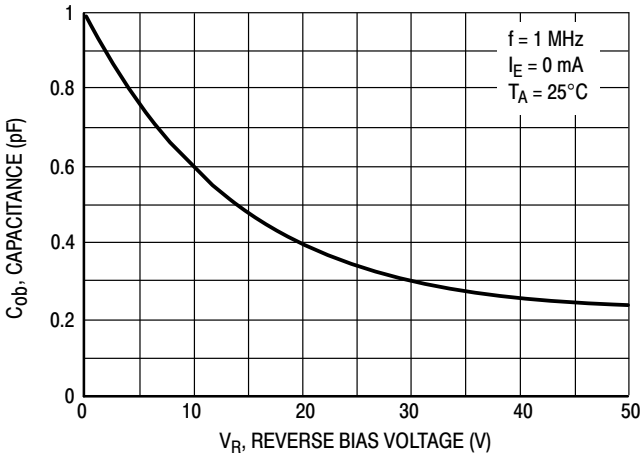



**Figure 34. Output Capacitance**

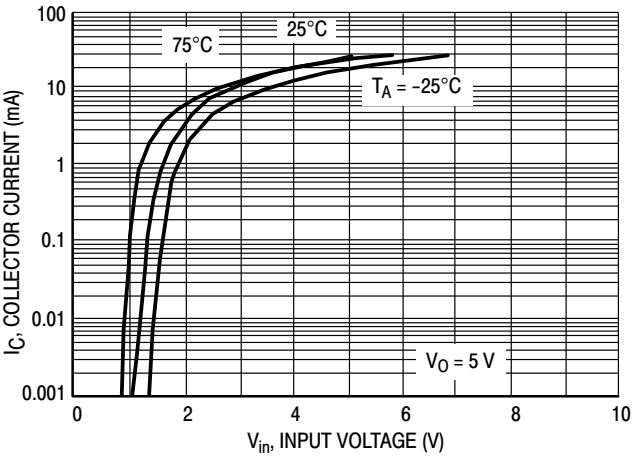



**Figure 35. Output Current versus Input Voltage**

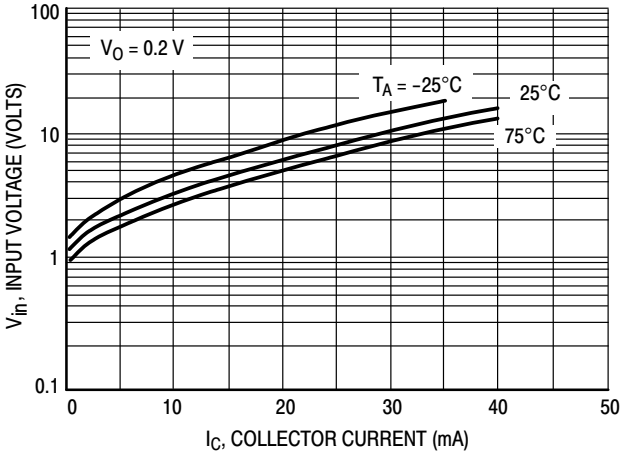
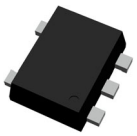
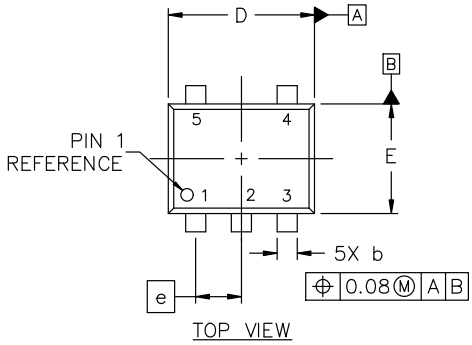



**Figure 36. Input Voltage versus Output Current**



**SOT−553−5 1.60x1.20x0.55, 0.50P**
CASE 463B
ISSUE D

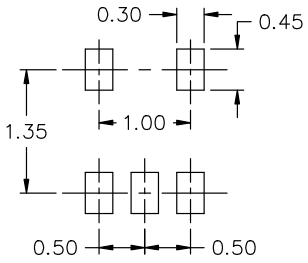
DATE 21 FEB 2024




NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.50 | 0.55 | 0.60 |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.08 | 0.13 | 0.18 |
| D | 1.55 | 1.60 | 1.65 |
| E | 1.15 | 1.20 | 1.25 |
| e | 0.50 BSC | | |
| H | 1.55 | 1.60 | 1.65 |
| L | 0.10 | 0.20 | 0.30 |




RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

**GENERIC MARKING DIAGRAM***


XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR 1
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

| | | |
|---|---|---|
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| **DESCRIPTION:** | **SOT−553−5 1.60x1.20x0.55, 0.50P** | **PAGE 1 OF 1** |

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