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Regulator - TinyPower™, Buck-Boost: 2.5 A, 1.8 MHz

FAN49100

WLCSP20 2.015x1.615x0.586
CASE 567QK

Description

The FAN49100 is a high efficiency buck−boost switching mode regulator which accepts input voltages either above or below the regulated output voltage. Using fullbridge architecture with synchronous rectification, the FAN49100 is capable of delivering up to 2.5 A at 3.6 V input while regulating the output at 3.3 V. The FAN49100 exhibits seamless transition between step−up and step−down modes reducing output disturbances.

At moderate and light loads, Pulse Frequency Modulation (PFM) is used to operate the device in power−save mode to maintain high efficiency. In PFM mode, the part still exhibits excellent transient response during load steps. At moderate to heavier loads or Forced PWM mode, the regulator switches to PWM fixed−frequency control. While in PWM mode, the regulator operates at a nominal fixed frequency of 1.8 MHz, which allows for reduced external component values.

The FAN49100 is available in a 20−bump 1.615 mm x 2.015 mm with 0.4 mm pitch WLCSP.

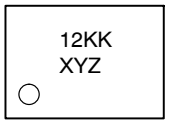
Features

- 24 μA Typical PFM Quiescent Current
- Above 95% Efficiency
- Total Layout Area = 11.61 mm^2
- Input Voltage Range: 2.5 V to 5.5 V
- 1.8 MHz Fixed−Frequency Operation in PWM Mode
- Automatic / Seamless Step−up and Step−down
- Mode Transitions
- Forced PWM and Automatic PFM / PWM Mode Selection
- 0.5 μA Typical Shutdown Current
- Low Quiescent Current Pass−Through Mode
- Internal Soft−Start and Output Discharge
- Low Ripple and Excellent Transient Response
- Internally Set, Automatic Safety Protections (UVLO, OTP, SCP, OCP)
- Package: 20 Bump, 0.4 mm Pitch WLCSP
- This Device is Pb−Free, Halogen Free / BFR Free

Applications

- Smart Phones
- Tablets, Netbooks, Ultra−Mobile PCs
- Portable Devices with Li−ion Battery
- 2G / 3G / 4G Power Amplifiers
- NFC Applications

MARKING DIAGRAM



12	= Alphanumeric Device Marking
KK	= Lot Run Code
X	= Alphabetical Year Code
Y	= 2−weeks Date Code
Z	= Assembly Plant Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

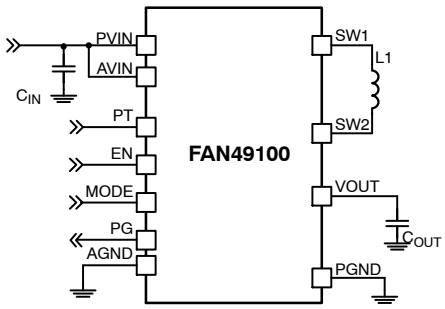


Figure 1. Typical Application

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Table 1. ORDERING INFORMATION

Part Number	Default Voltage (Note 1)	Output Discharge	Temperature Range	Package	Shipping†	Device Marking
FAN49100AUC330X	3.3 V	Yes	−40 to 85°C	20−Ball (WLCSP)	Tape and Reel	FD
FAN49100AUC360X	3.6 V					FE

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. Additional VOUT values are available, contact **onsemi** representative.

BLOCK DIAGRAM

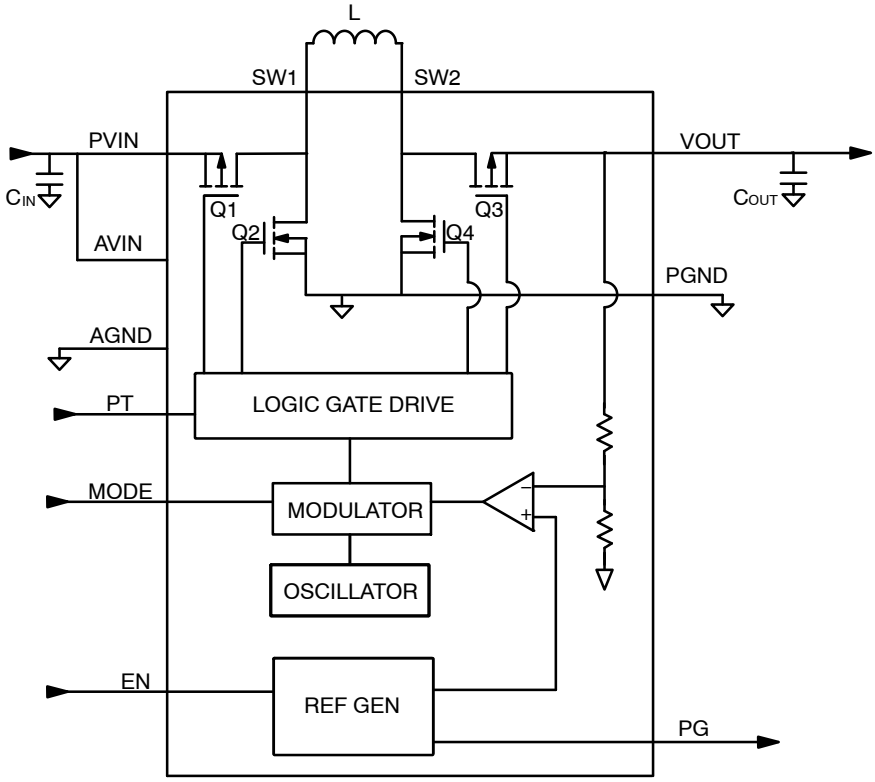

Figure 2. Block Diagram

PIN CONFIGURATION

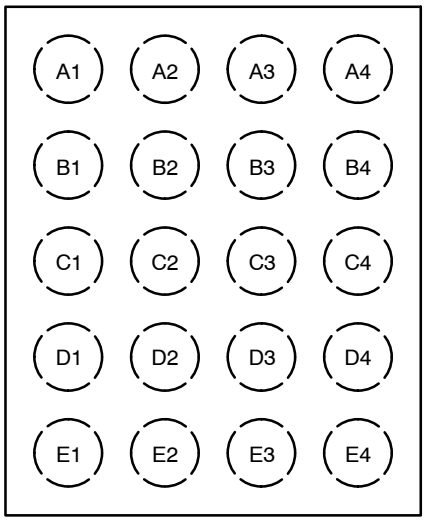

Figure 3. Top View (Bump Down)

Table 2. PIN DEFINITIONS (Note 2)

Pin #	Name	Description
A3, A4	PVIN	**Power Input Voltage.** Connect to input power source. Connect to C_{IN} with minimal path.
A1	AVIN	**Analog Input Voltage.** Analog input for device. Connect to C_{IN} and PVIN.
A2	EN	**Enable.** A HIGH logic level on this pin forces the device to be enabled. A LOW logic level forces the device into shutdown. EN pin can be tied to VIN or driven via a GPIO logic voltage.
B3, B4	SW1	**Switching Node 1.** Connect to inductor L1.
E1	AGND	**Analog Ground.** Control block signal is referenced to this pin. Short AGND to PGND at GND pad of $C_{OUT.}$
B1, C1, C2, C3, C4, D1	PGND	**Power Ground.** Low−side MOSFET of buck and main MOSFET of boost are referenced to this pin. C_{IN} and C_{OUT} should be returned with a minimal path to these pins.
D2	MODE	**Forced PWM / AUTO Mode.** HIGH logic level on this pin forces the chip to stay in PWM mode, while LOW logic level allows the chip to automatically switch between PFM and PWM modes. Don't leave the pin floating.
D3, D4	SW2	**Switching Node 2.** Connect to inductor L1.
E2	PG	**Power Good.** This is an open−drain output and normally High Z. An external pull−up resistor from VOUT can be used to generate a logic HIGH. PG is pulled LOW if output falls out of regulation due to current overload or if thermal protection threshold is exceeded. If EN is LOW, PG is high impedance.
B2	PT	**Pass−Through.** HIGH logic level forces Pass−Through mode. A LOW logic level forces normal operation. Don't leave the pin floating.
E3, E4	VOUT	**Output Voltage.** Buck−Boost Output. Connect to output load and $C_{OUT.}$

2. Refer to Layout Recommendation section located near the end of the datasheet.

Table 3. ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, Unless otherwise specified)

Symbol	Parameter		Min.	Max.	Unit
PVIN/AVIN	PVIN/AVIN Voltage		−0.3	6.5	V
VOUT	VOUT Voltage		−0.3	6.5	V
SW1, SW2	SW Nodes Voltage		−0.3	7.0	V
	Other Pins		−0.3	6.5	V
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22−A114	2000		V
		Charged Device Model per JESD22−C101	1000		
T_J	Junction Temperature		−40	+150	°C
T_{STG}	Storage Temperature		−65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 4. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
PVIN	Supply Voltage Range	2.5		5.5	V
I_{OUT}	Output Current (Note 3)	0		2.5	A
L	Inductor (Note 4)		1		μH
C_{OUT}	Output Capacitance (Note 4)		47		μF
T_A	Operating Ambient Temperature	−40		+85	°C
T_J	Operating Junction Temperature	−40		+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Maximum current may be limited by the thermal conditions of the end application, PCB layout, and external component selection in addition to the device's thermal properties. Refer to the Application Information and Application Guidelines sections for more information.
4. Refer to the Application Guidelines section for details on external component selection.

Table 5. THERMAL PROPERTIES

Symbol	Parameter	Min.	Typ.	Max.	Unit
θ_{JA}	Junction−to−Ambient Thermal Resistance (Note 5)		66		°C/W

5. See Thermal Considerations in the Application Information section.

Table 6. ELECTRICAL CHARACTERISTICS (Note 6, 7)
Minimum and maximum values are at PVIN = AVIN = 2.5 V to 5.5 V, T_A = −40°C to +85°C. Typical values are at T_A = 25°C, PVIN = AVIN = VEN = 3.6 V, VOUT = 3.3 V.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
POWER SUPPLIES						
I_Q	Quiescent Current	PFM Mode, I_{OUT} = 0 mA (Note 8)		24		μA
		PT Mode, I_{OUT} = 0 mA		27		
I_{SD}	Shutdown Supply Current	EN = GND, PVIN = 3.6 V		0.5	5.0	
V_{UVLO}	Under−Voltage Lockout Threshold	Falling PVIN	1.95	2.00	2.05	V
V_{UVHYST}	Under−Voltage Lockout Hysteresis			200		mV
EN, MODE, PT						
V_{IH}	HIGH Level Input Voltage		1.1			V
V_{IL}	LOW Level Input Voltage				0.4	V
I_{IN}	Input Bias Current Into Pin	Input Tied to GND or PVIN		0.01	1.00	μA
PG						
V_{PG}	PG LOW	I_{PG} = 5 mA			0.4	V
I_{PG_LK}	PG Leakage Current	V_{PG} = 5 V			1	μA
SWITCHING						
f_{SW}	Switching Frequency	PVIN = 3.6 V, T_A = 25°C	1.6	1.8	2.0	MHz
I_{p_LIM}	Peak PMOS Current Limit	PVIN = 3.6 V	4.6	5.2	5.9	A
ACCURACY						
V_{OUT_ACC}	DC Output Voltage Accuracy	PVIN = 3.6 V, Forced PWM, I_{OUT} = 0 mA, VOUT = 3.3 V	3.267	3.300	3.333	V
		PVIN = 3.6 V, PFM Mode, I_{OUT} = 0 mA, VOUT = 3.3 V	3.267	3.375	3.458	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Refer to Typical Characteristics waveforms/graphs for Closed−Loop data and its variation with input voltage and ambient temperature. Electrical Characteristics reflects Open−Loop steady state data. System Characteristics reflects both steady state and dynamic Close−Loop data associated with the recommended external components.
7. Minimum and Maximum limits are verified by design, test, or statistical analysis. Typical (Typ.) values are not tested, but represent the parametric norm.
8. Device is not switching.

Table 7. SYSTEM CHARACTERISTICS

The following table is verified by design and bench test while using circuit of Figure 1 with the recommended external components. Typical values are at T_A = 25°C, PVIN = AVIN = V_{EN} = 3.6 V, VOUT = 3.3 V. These parameters are not verified in production.

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{OUT_ACC}	Total Accuracy (Includes DC Accuracy and Load Transient) (Note 9)			±5		%
ΔV_{OUT}	Load Regulation	I_{OUT} = 0.4 A to 2.5 A, PVIN = 3.6 V		−0.10		%/A
ΔV_{OUT}	Line Regulation	3.0 V ≤ PVIN ≤ 4.2 V, I_{OUT} = 1.5 A		−0.06		%/V
V_{OUT_RIPPLE}	Ripple Voltage	PVIN = 4.2 V, VOUT = 3.3 V, I_{OUT} = 1 A, PWM Mode		4		mV
		PVIN = 3.6 V, VOUT = 3.3 V, I_{OUT} = 100 mA, PFM Mode		22		
		PVIN = 3.0 V, VOUT = 3.3 V, I_{OUT} = 1 A, PWM Mode		14		
η	Efficiency	PVIN = 3.0 V, VOUT = 3.3 V, I_{OUT} = 75 mA, PFM		90		%
		PVIN = 3.0 V, VOUT = 3.3 V, I_{OUT} = 500 mA, PWM		96		
		PVIN = 3.8 V, VOUT = 3.3 V, I_{OUT} = 100 mA, PFM		91		
		PVIN = 3.8 V, VOUT = 3.3 V, I_{OUT} = 600 mA, PWM		96		
		PVIN = 3.4 V, VOUT = 3.3 V, I_{OUT} = 300 mA, PWM		93		
T_{SS}	Soft−Start	EN HIGH to 95% of Target VOUT, I_{OUT} = 68 mA		260		μs
ΔV_{OUT_LOAD}	Load Transient	PVIN = 3.4 V, I_{OUT} = 0.5 A ⇔ 1 A, T_R = T_F = 1 μs		±45		mV
		PVIN = 3.4 V, I_{OUT} = 0.5 A ⇔2.0 A, T_R = T_F = 1 μs, Pulse Width = 577 μs		±125		
ΔV_{OUT_LINE}	Line Transient	PVIN = 3.0 V ⇔ 3.6 V, T_R = T_F = 10 μs, I_{OUT} = 1 A		±60		mV

9. Load transient is from 0.5 A ⇔1 A.

TYPICAL CHARACTERISTICS

Unless otherwise noted, PVIN = AVIN = VEN = 3.6 V, VOUT = 3.3 V, circuit of Figure 1 with the recommended external components, AUTO Mode

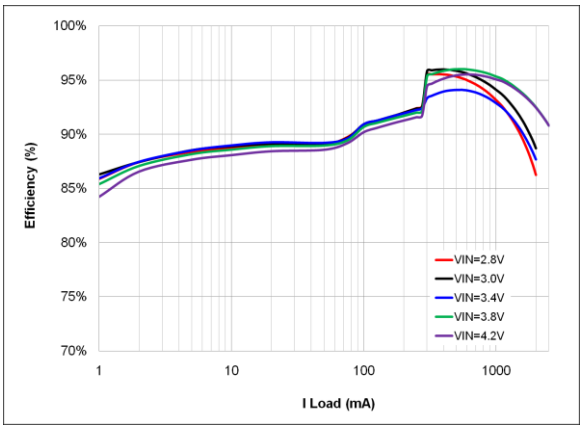

Figure 4. Efficiency vs. Load

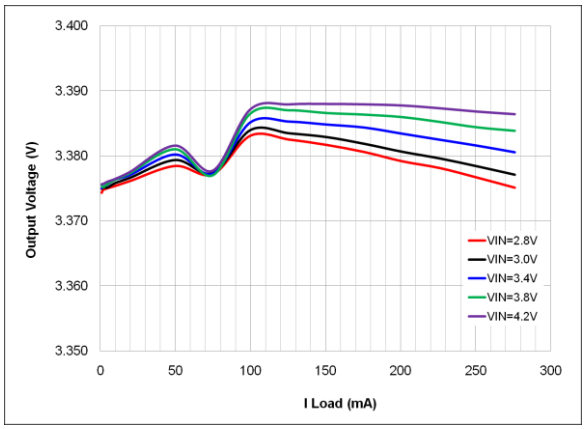

Figure 5. Output Regulation vs. Load

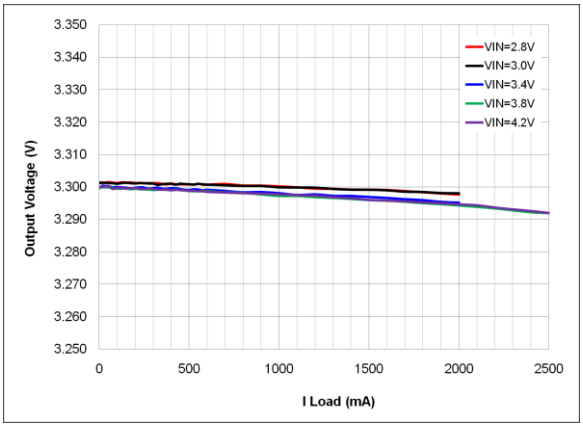

Figure 6. Output Regulation vs. Load, PWM Mode

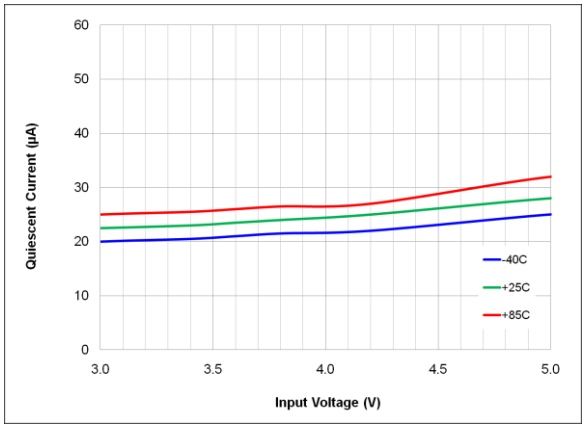

Figure 7. Quiescent Current (No Switching) vs. Input Voltage

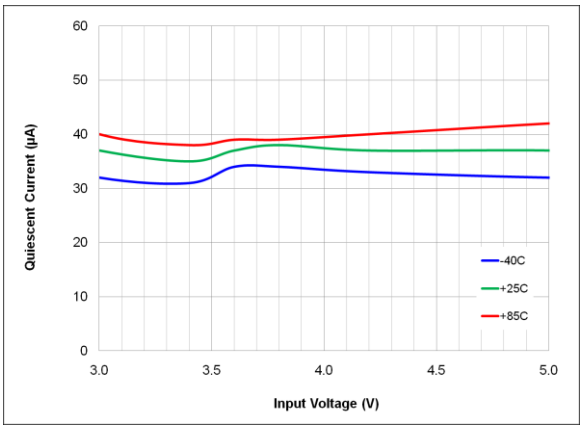

Figure 8. Quiescent Current (Switching) vs. Input Voltage

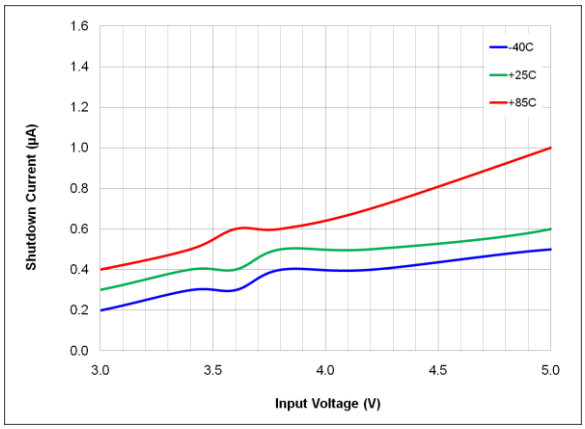

Figure 9. Shutdown Current vs. Input Voltage

TYPICAL CHARACTERISTICS (continued)

Unless otherwise noted, PVIN = AVIN = VEN = 3.6 V, VOUT = 3.3 V, circuit of Figure 1 with the recommended external components, AUTO Mode

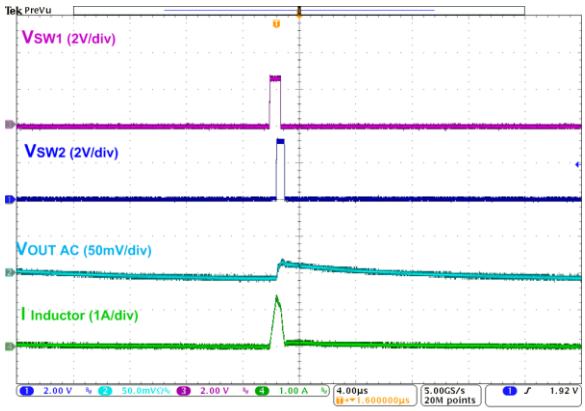

Figure 10. Output Ripple, VIN = 2.8 V, I_{OUT} = 20 mA, Boost Operation

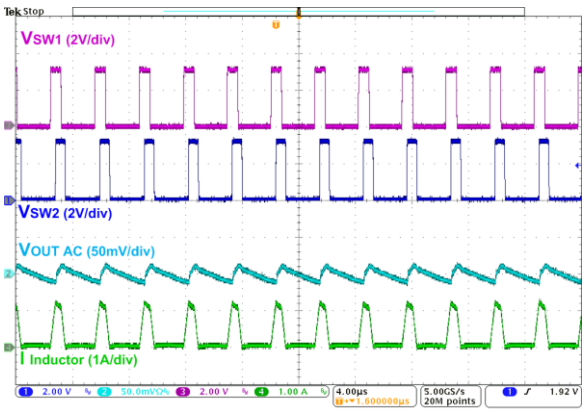

Figure 11. Output Ripple, VIN = 3.3 V, I_{OUT} = 200 mA, Buck−Boost Operation

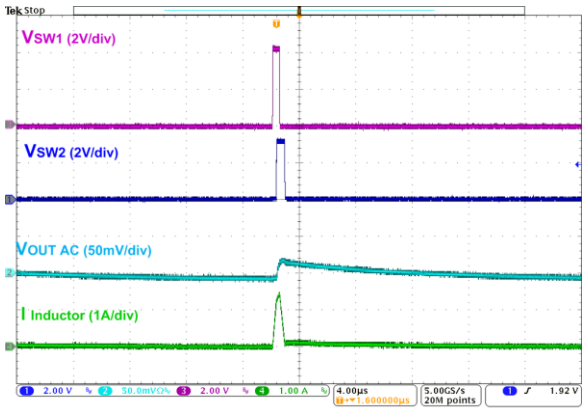

Figure 12. Output Ripple, VIN = 4.2 V, I_{OUT} = 20 mA, Buck Operation

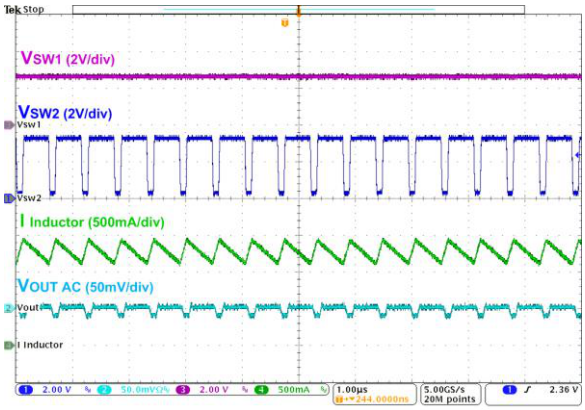

Figure 13. Output Ripple, VIN = 2.5 V, I_{OUT} = 1000 mA, Boost Operation

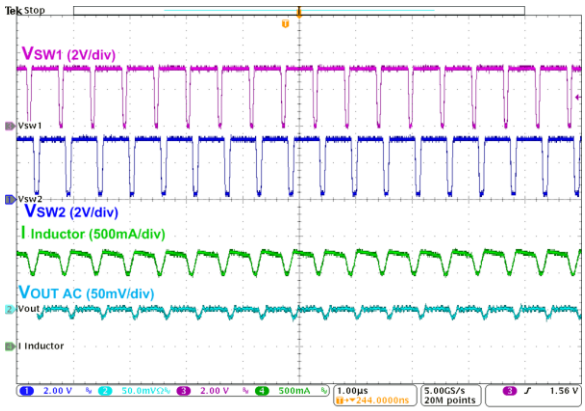

Figure 14. Output Ripple, VIN = 3.3 V, I_{OUT} = 1000 mA, Buck−Boost Operation

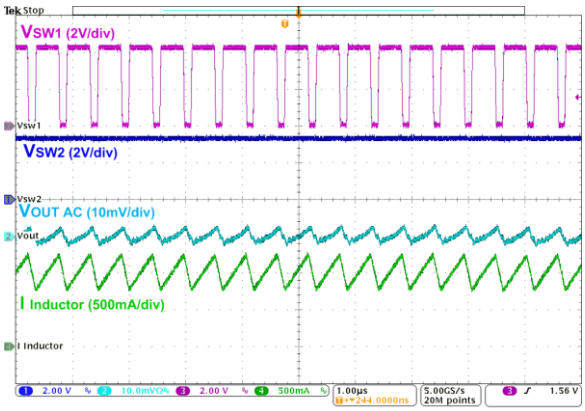

Figure 15. Output Ripple, VIN = 4.5 V, I_{OUT} = 1000 mA, Buck Operation

TYPICAL CHARACTERISTICS (continued)

Unless otherwise noted, PVIN = AVIN = VEN = 3.6 V, VOUT = 3.3 V, circuit of Figure 1 with the recommended external components, AUTO Mode

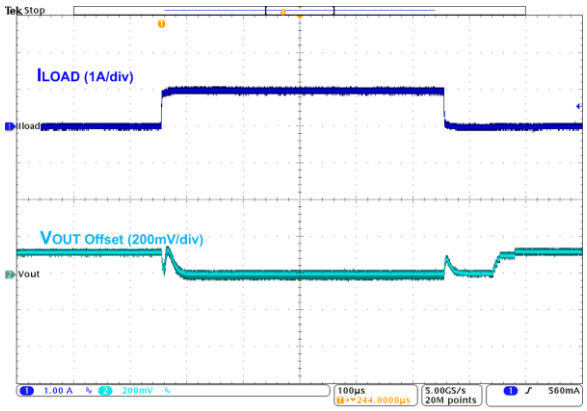

Figure 16. Load Transient, 0 mA ⇔ 1000 mA, 1 μs Edge, VIN = 3.60 V

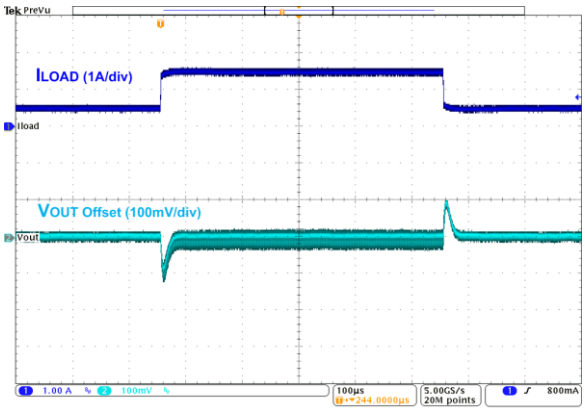

Figure 17. Load Transient, 500 mA ⇔ 1500 mA, 1 μs Edge, VIN = 3.60 V

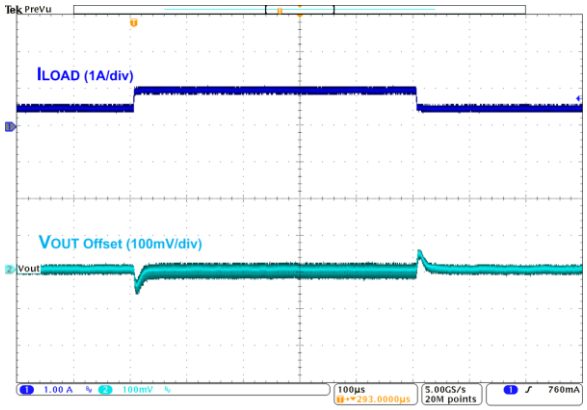

Figure 18. Load Transient, 500 mA ⇔ 1000 mA, 1 μs Edge, VIN = 3.40 V

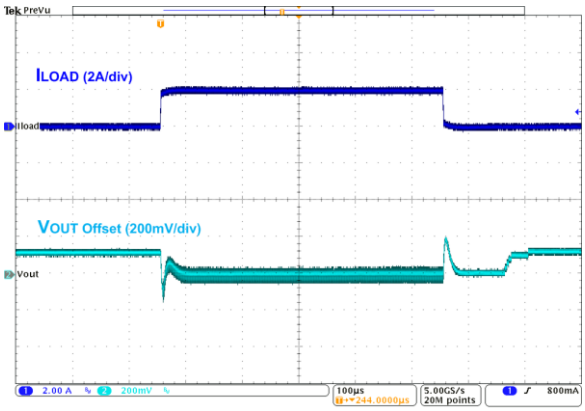

Figure 19. Load Transient, 0 mA ⇔ 2000 mA, 1 μs Edge, VIN = 3.60 V

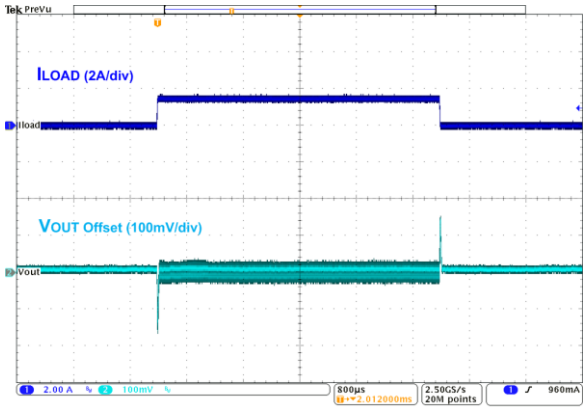

Figure 20. Load Transient, 0 mA ⇔ 1500 mA, 10 μs Edge, VIN = 2.80 V, PWM Mode

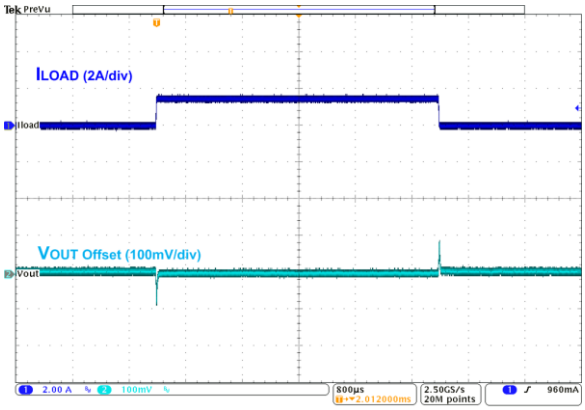

Figure 21. Load Transient, 0 mA ⇔ 1500 mA, 10 μs Edge, VIN = 4.20 V, PWM Mode

TYPICAL CHARACTERISTICS (continued)

Unless otherwise noted, PVIN = AVIN = VEN = 3.6 V, VOUT = 3.3 V, circuit of Figure 1 with the recommended external components, AUTO Mode

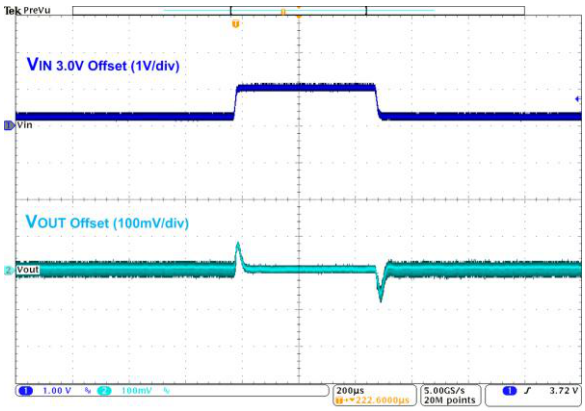

Figure 22. Line Transient, 3.2 ⇔ 4.0 VIN, 10 μs Edge, 1000 mA Load

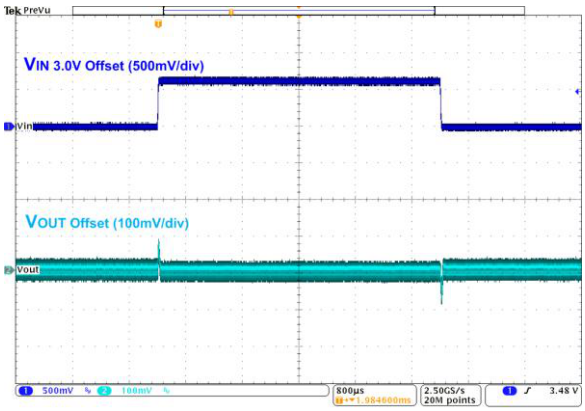

Figure 23. Line Transient, 3.0 ⇔ 3.6 VIN, 10 μs Edge, 1500 mA Load, PWM

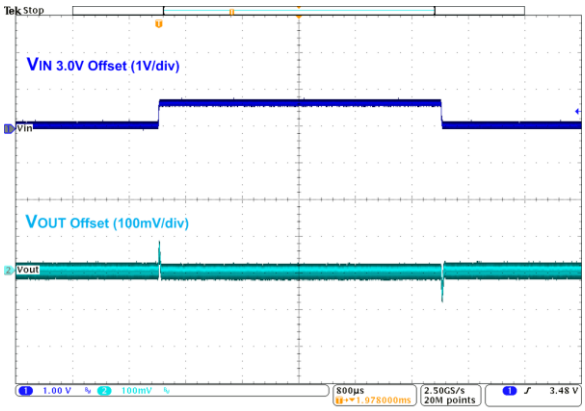

Figure 24. Line Transient, 3.0 ⇔ 3.6 VIN, 10 μs Edge, 1000 mA Load, PWM

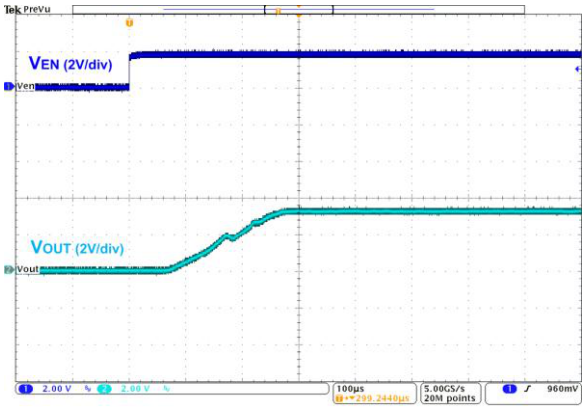

Figure 25. Startup, VIN = 3.6 V, I_{OUT} = 0 mA

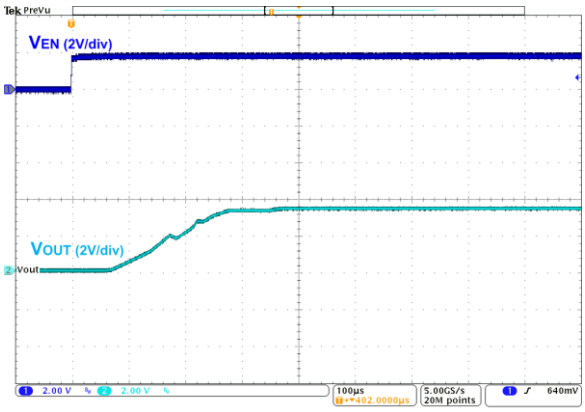

Figure 26. Startup, VIN = 3.6 V, I_{OUT} = 68 mA

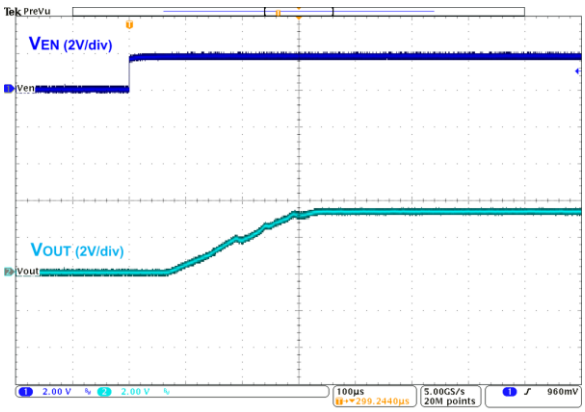

Figure 27. Startup, VIN = 3.6 V, I_{OUT} = 1000 mA

TYPICAL CHARACTERISTICS (continued)

Unless otherwise noted, PVIN = AVIN = VEN = 3.6 V, VOUT = 3.3 V, circuit of Figure 1 with the recommended external components, AUTO Mode

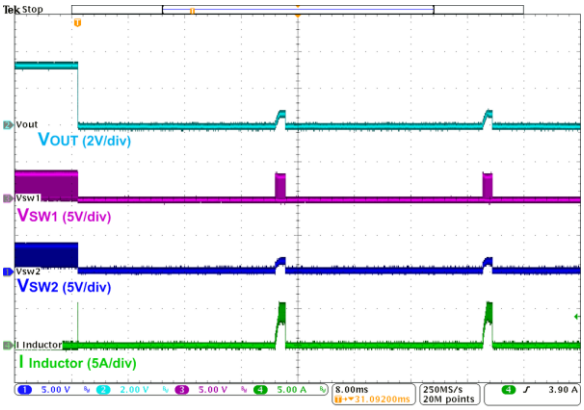

Figure 28. Short−Circuit Protection

APPLICATION INFORMATION

Functional Description

FAN49100 is a fully integrated synchronous, full bridge DC−DC converter that can operate in buck operation (during high PVIN), boost operation (for low PVIN) and a combination of buck−boost operation when PVIN is close to the target VOUT value. The PWM/PFM controller switches automatically and seamlessly between buck, buck−boost and boost modes.

The FAN49100 uses a four−switch operation during each switching period when in the buck−boost mode. Mode operation is as follows: referring to the power drive stage shown in Figure 29, if PVIN is greater than target VOUT, then the converter is in buck mode: Q3 is ON and Q4 is OFF continuously leaving Q1, Q2 to operate as a current−mode controlled PWM converter. If PVIN is lower than target VOUT then the converter is in boost mode with Q1 ON and Q2 OFF continuously, while leaving Q3, Q4 to operate as a current−mode boost converter. When PVIN is near VOUT, the converter goes into a 3−phase operation in which combines a buck phase, a boost phase and a reset phase; all switches are switching to maintain an average inductor volt−second balance.

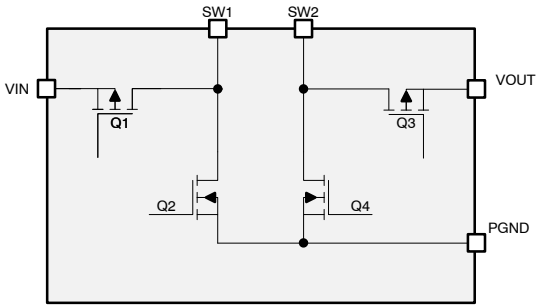

Figure 29. Simplified Block Diagram

PFM/PWM Mode

The FAN49100 uses a current−mode modulator to achieve smooth transitions between PWM and PFM operation. In Pulsed Frequency Modulation (PFM), frequency is reduced to maintain high efficiency. During PFM operation, the converter positions the output voltage typically 75 mV higher than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. As the load increased from light loads, the converter enters PWM operation typically at 300 mA of current load. The converter switching frequency is typically 1.8 MHz during PWM operation for moderate to heavy load currents.

PT (Pass−Through) Mode

In Pass−Through mode, all of the switches are not switching and VOUT tracks PVIN (VOUT = PVIN − $I_{OUT} \times (Q1_{RDSON} + Q3_{RDSON} + L_{DCR})$. In PT mode only Over−Temperature (OTP) and Under Voltage Lockout (UVLO) protection circuits are activated. There is no Over−Current Protection (OCP) in PT mode.

Shutdown and Startup

When the EN pin is LOW, the IC is shut down, all internal circuits are off, and the part draws very little current. During shutdown, VOUT is isolated from PVIN. Raising EN pin activates the device and begins the softstart cycle. During soft−start, the modulator's internal reference is ramped slowly to minimize surge currents on the input and prevent overshoot of the output voltage. If VOUT fails to reach target VOUT value after 1 ms, a FAULT condition is declared.

Over−Temperature (OTP)

The regulator shuts down when the die temperature exceeds 150°C. Restart occurs when the IC has cooled by approximately 20°C.

Output Discharge

When the regulator is disabled and driving the EN pin LOW, a 230 Ω internal resistor is activated between VOUT and GND. The Output Discharge is not activated during a FAULT state condition.

Over−Current Protection (OCP)

If the peak current limit is activated for a typical 700 µs, a FAULT state is generated, so that the IC protects itself as well as external components and load.

FAULT State

The regulator enters the FAULT state under any of the following conditions:

- VOUT fails to achieve the voltage required after soft−start
- Peak current limit triggers
- OTP or UVLO are triggered

Once a FAULT is triggered, the regulator stops switching and presents a high−impedance path between PVIN and VOUT. After waiting 30 ms, a restart is attempted. The regulator shuts down when the die temperature exceeds 150°C. Restart occurs when the IC has cooled by approximately 20°C.

Power Good

PG, an open−drain output, is LOW during FAULT state and HIGH for Power Good. The PG pin is provided for signaling the system when the regulator has successfully completed soft−start and no FAULTs have occurred. PG pin also functions as a warning flag for high die temperature and overload conditions.

- PG is released HIGH when the soft−start sequence is successfully completed.
- PG is pulled LOW when a FAULT is declared.

Any FAULT condition causes PG to be de−asserted.

Thermal Considerations

For best performance, the die temperature and the power dissipated should be kept at moderate values. The maximum power dissipated can be evaluated based on the following relationship:

$$P_{D(max)} = \left\{ \frac{T_{J(max)} - T_A}{\Theta_{JA}} \right\}$$

where $T_{J(max)}$ is the maximum allowable junction temperature of the die; T_A is the ambient operating temperature; and θ_{JA} is dependent on the surrounding PCB layout and can be improved by providing a heat sink of surrounding copper ground. The addition of backside copper with through−holes, stiffeners, and other enhancements can help reduce θ_{JA}. The heat contributed by the dissipation of devices nearby must be included in design considerations. Following the layout recommendation may lower the θ_{JA}.

APPLICATION GUIDELINES

Table 8. RECOMMENDED EXTERNAL COMPONENTS

Reference Designator	Description	Quantity	Part Number
L	1 µH, Isat(max) = 4.2 A, 36 mΩ(max), 2016	1	Cyntec HTEH20161T−1R0MSR
C_{OUT}	47 µF (x2), 6.3 V, X5R, 1608	2	Murata GRM188R60J476ME15
C_{IN}	22 µF, 10 V, X5R, 1608	1	Murata GRM187R61A226ME15

Alternative External Components

It is recommended to use the external components in Table 8. Alternative components that are suitable for a design's specific requirements must also meet the IC's requirements for proper device operation.

De−rating factors should be taken into consideration to ensure selected components meet minimum requirements.

Output Capacitor (COUT)

As shown in the recommended layout, C_{OUT} must connect to the VOUT pin with the lowest impedance trace possible. Additionally, C_{OUT} must connect to the GND pin with the lowest impedance possible.

Smaller−than−recommended value output capacitors may be used for applications with reduced load current requirements. When selecting capacitors for minimal solution size, it must be noted that the effective capacitance (C_{EFF}) of small, high−value, ceramic capacitors will decrease as bias voltage increases. The effects of Bias Voltage (DC Bias Characteristics), Tolerance, and Temperature should be included when determining a component's effective capacitance.

The FAN49100 is guaranteed for stable operation with no less than the minimum effective output capacitance values shown in Table 9.

Table 9. REQUIRED MINIMUM EFFECTIVE OUTPUT CAPACITANCE VERSUS MAXIMUM LOAD

Maximum Load Current	Inductor (μH)	Required Minimum Effective Output Capacitance (μF)
≤ 2000 mA	1.0	15
	0.47	9
≤ 1500 mA	1.0	12
≤ 1000 mA	1.0	9
≤ 600 mA	1.0	7
≤ 500 mA	1.0	6

Table 10. EFFECTIVE CAPACITANCE VERSUS PART NUMBER

PN	Size (mm) LW x H	Nominal Value (μF)	Rating (V)	Tol. (%)	Bias (V)	Effective Capacitance (μF) Due to Bias, Temperature and Tolerance
Murata GRM188R60J476ME15	1608 x 1.0	47	6.3	20	3.4	8.5
Murata GRM187R61A226ME15	1608 x 0.8	22	10	20	3.4	6.3
					5	4.2
Murata GRM188R61A106KE69	1608 x 1.0	10	10	10	3.4	3.2
					5	2.3

Input Capacitor (C_{IN})

As shown in the recommended layout, C_{IN} must connect to the PVIN pin with the lowest impedance trace possible. Additionally, C_{IN} must connect to the GND pin with the lowest impedance possible.

The FAN49100 is guaranteed for stable operation with a minimum effective capacitance of 2 μF. It is recommended to use a high quality input capacitor rated at 10 μF nominal or greater. Additional capacitance is required when the FAN49100's power source is not located close to the device.

Inductor (L)

As shown in the recommended layout, the inductor (L) must connect to the SW1 and SW2 pins with the lowest impedance trace possible.

The recommended nominal inductance value is 1.0 μH. A value of 0.47 μH can be used, but higher peak currents should be expected.

The FAN49100 employs peak current limiting, and the peak inductor current can reach I_{P_LIM} before limiting, therefore current saturation should be considered when choosing an inductor.

LAYOUT RECOMMENDATIONS

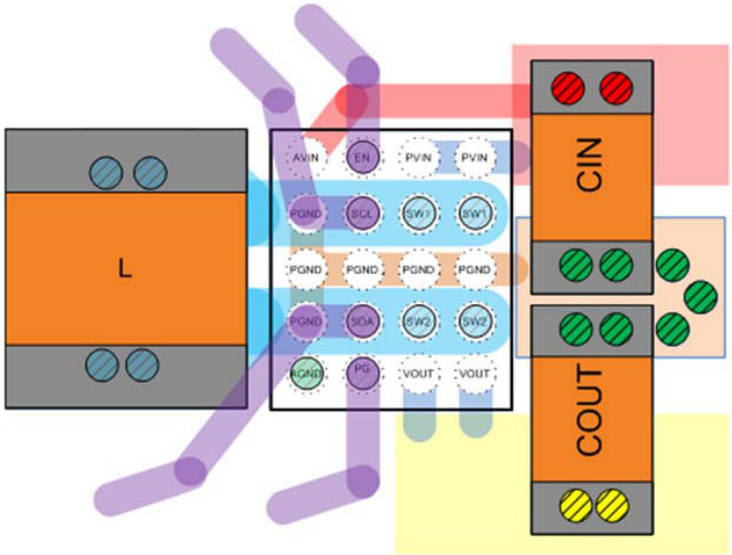

Figure 30. Component Placement and Routing for FAN49100

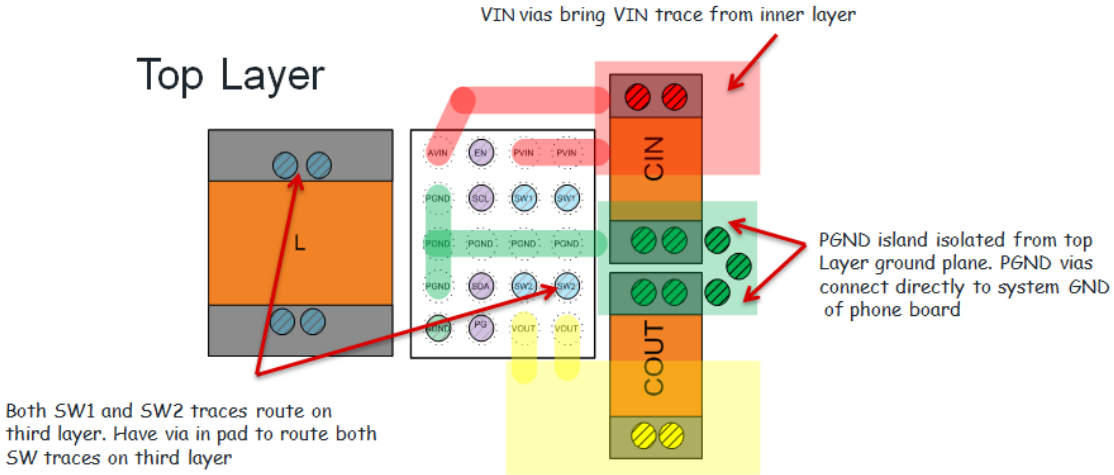

Figure 31. Top Layer Routing for FAN49100

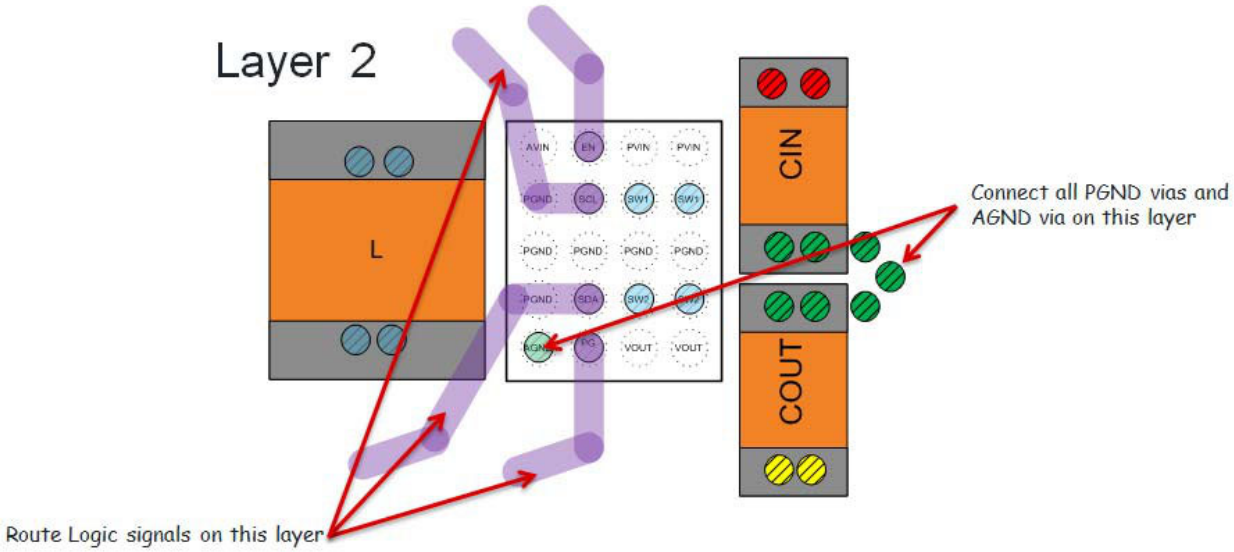

Figure 32. Layer 2 Routing for FAN49100

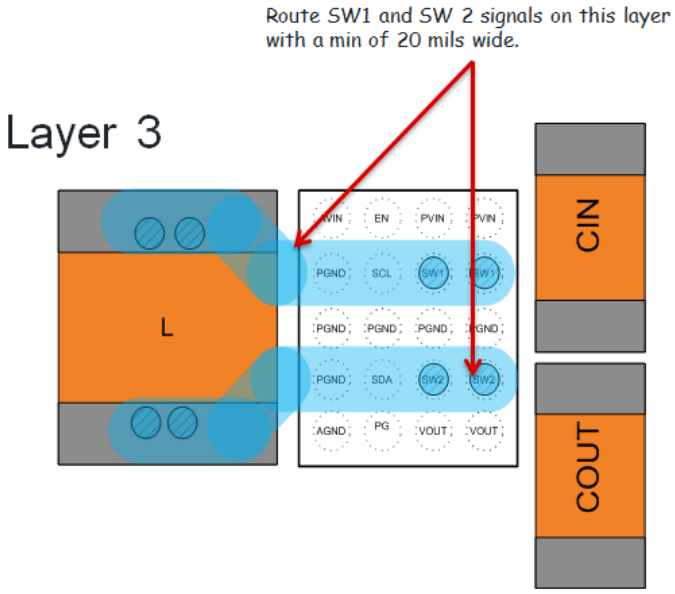

Figure 33. Layer 3 Routing for FAN49100

Table 11. PHYSICAL DIMENSIONS This table information applies to the Package drawing on the following page.

Product	D	E	X	Y
FAN49100AUC330X	2.015 ±0.030	1.615 ±0.030	0.2075	0.2075
FAN49100AUC360X	2.015 ±0.030	1.615 ±0.030	0.2075	0.2075

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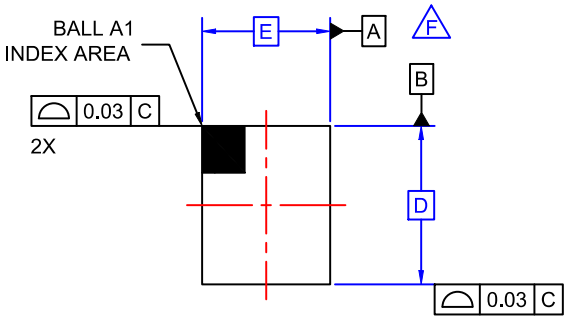
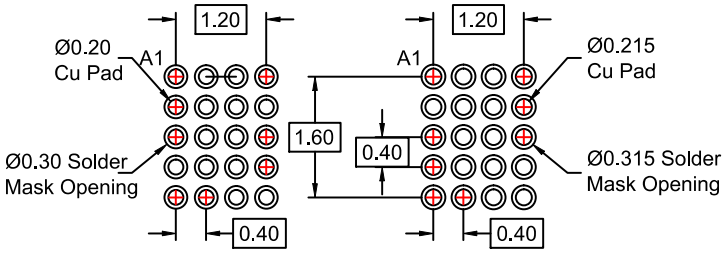
ISSUE O

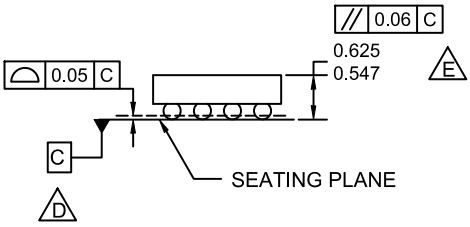
DATE 31 OCT 2016

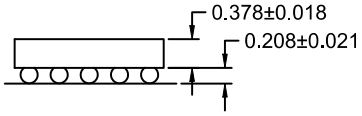


TOP VIEW

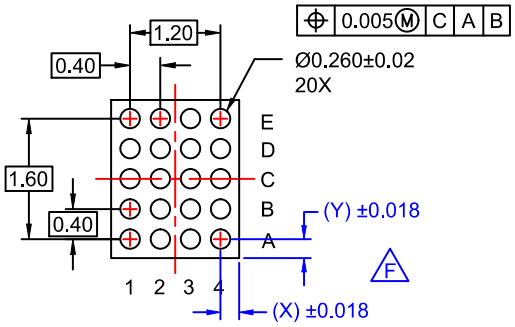


RECOMMENDED LAND PATTERN
(NSMD TYPE)





SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 2009.
D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).
F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

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