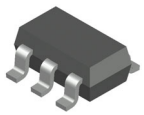
High Efficiency Serial LED Driver and OLED Supply with 20 V Integrated Switch

FAN5331



SOT−23 (5−LEAD)
CASE 527 AH

Description

The FAN5331 is a general purpose, fixed−frequency boost converter designed to operate at high switching frequencies in order to minimize switching noise measured at the battery terminal of hand−held communications equipment. Quiescent current in normal mode of operation as well as in shutdown mode is designed to be minimal in order to extend battery life. Normal mode of operation or shutdown mode can be selected by a logic level shutdown circuitry.

The low ON−resistance of the internal N−channel switch ensures high efficiency and low power dissipation. A cycle−by−cycle current limit circuit keeps the peak current of the switch below a typical value of 1 A. The FAN5331 is available in a 5−lead SOT− 23 package.

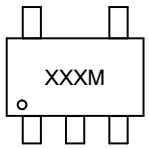
Features

- 1.6 MHz Switching Frequency
- Low Noise
- Low $R_{DS(ON)}$: 0.5 Ω
- Adjustable Output Voltage
- 1 A Peak Switch Current
- 1 W Output Power Capability
- Low Shutdown Current: <1 μA
- Cycle−by−Cycle Current Limit
- Over−Voltage Protection
- Fixed−Frequency PWM Operation
- Internal Compensation
- 5−lead SOT−23 Package

Typical Application

- Cell Phones
- PDAs
- Handheld Equipment
- Display Bias
- LED Bias

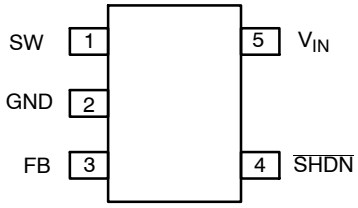
MARKING DIAGRAM



XXX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

PIN ASSIGNMENT



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

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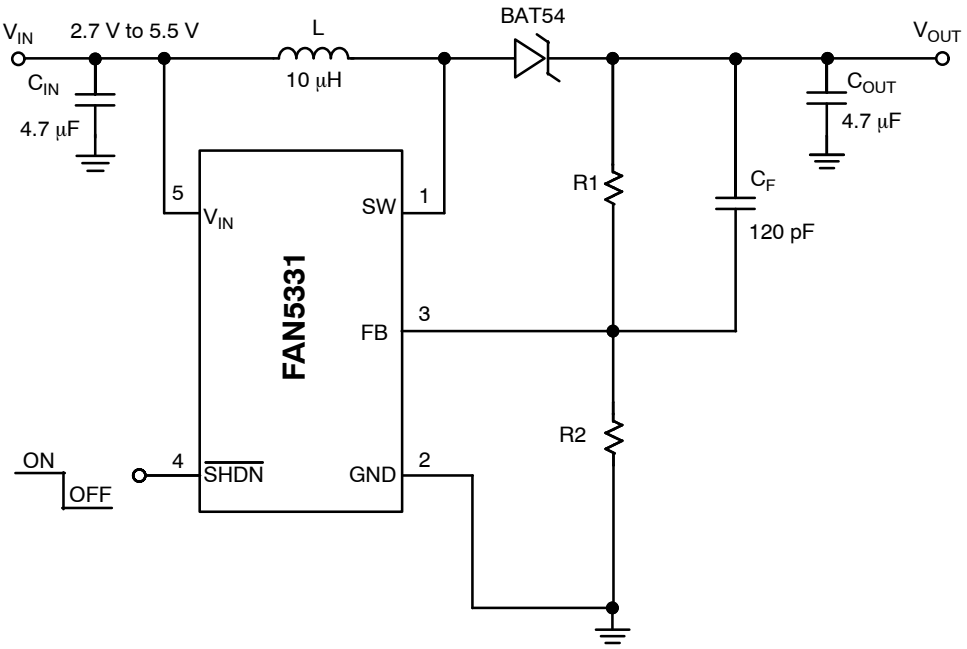


Figure 1. Typical Application Diagram

PIN DESCRIPTION

Pin No.	Pin Name	Pin Description
1	SW	Switching node.
2	GND	Analog and power ground.
3	FB	Feedback node that connects to an external voltage divider.
4	$\overline{SHDN}$	Shutdown control pin. Logic HIGH enables, logic LOW disables the device.
5	VIN	Input voltage.

ABSOLUTE MAXIMUM RATINGS

Parameter		Min	Max	Unit
V_{IN} to GND		–	6.0	V
FB, $\overline{SHDN}$ to GND		−0.3	V_{IN} + 0.3	V
SW to GND		−0.3	23	V
Lead Soldering Temperature (10 seconds)		–	300	°C
Junction Temperature		–	150	°C
Storage Temperature		−55	150	°C
Thermal Resistance (Θ_{JA})		–	265	°C/W
Electrostatic Discharge Protection (ESD) Level (Note 1)	HBM	2.5	–	kV
	CDM	1	–	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Unit
Input Voltage	2.7	–	5.5	V
Output Voltage	V_{IN}	–	20	V
Operating Ambient Temperature	−40	25	85	°C
Output Capacitance (Note 2)	1.6	–	–	μF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Using EIA/JESD22A114B (Human Body Model) and EIA/JESD22C101−A (Charge Device Model).
2. This load capacitance value is required for the loop stability. Tolerance, temperature variation, and voltage dependency of the capacitance must be considered. Typically a 4.7 μF ceramic capacitor is required to achieve specified value at V_{OUT} = 15 V.

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, V_{IN} = 3.6 V, T_A = −40°C to +85°C, Typical values are at T_A = 25°C, Test Circuit, Figure 2.

Parameter	Conditions	Min	Typ	Max	Units
Switch Current Limit	V_{IN} = 3.2 V	0.7	1	–	A
Load Current Capability	V_{OUT} = 15 V, $V_{IN} \geq$ 2.7 V	35	–	–	mA
	V_{OUT} = 15 V, $V_{IN} \geq$ 3.2 V	50	–	–	mA
Switch On−resistance	V_{IN} = 5 V	–	0.5	–	Ω
	V_{IN} = 3.6 V	–	0.7	–	Ω
Quiescent Current	$V_{\overline{SHDN}}$ = 3.6 V, No Switching	–	0.7	–	mA
	$V_{\overline{SHDN}}$ = 3.6 V, Switching	–	1.6	3.0	mA
OFF Mode Current	$V_{\overline{SHDN}}$ = 0 V	–	0.1	2	μA
Shutdown Threshold	Device ON	1.5	–	–	V
	Device OFF	–	–	0.5	V
Shutdown Pin Bias Current	$V_{\overline{SHDN}}$ = 0 V or $V_{\overline{SHDN}}$ = 5.5 V	–	10	–	nA
Feedback Voltage	I_{Load} = 0 mA	1.205	1.230	1.255	V
Feedback Pin Bias Current		–	10	–	nA
Feedback Voltage Line Regulation	2.7 V < V_{IN} < 5.5 V, I_{LOAD} = 0 mA	–	0.6	1.2	%
Switching Frequency		1.15	1.6	1.85	MHz
Maximum Duty Cycle		87	93	–	%
Enable Delay	V_{IN} = 2.7 V, I_{OUT} = 35 mA, V_{OUT} = 15 V	–	0.8	5	mS
Power on Delay	V_{IN} = 2.7 V, I_{OUT} = 35 mA, V_{OUT} = 15 V	–	0.8	5	mS
Switch Leakage Current	No Switching, V_{IN} = 5.5 V	–	–	1	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

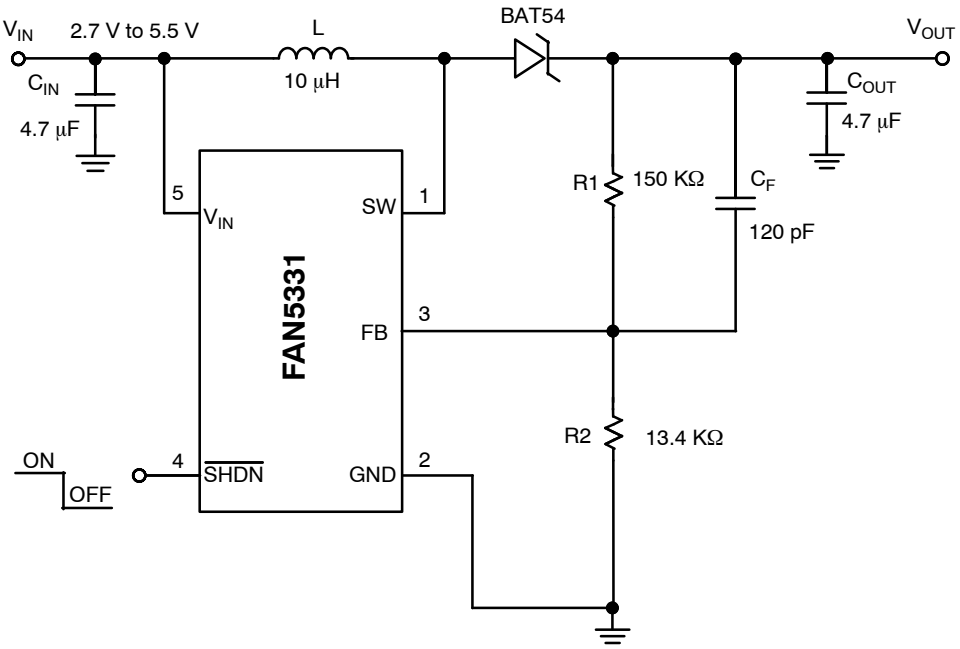


Figure 2. Test Circuit

TYPICAL CHARACTERISTICS

T_A = 25°C, Test Circuit Figure 2, unless otherwise noted.

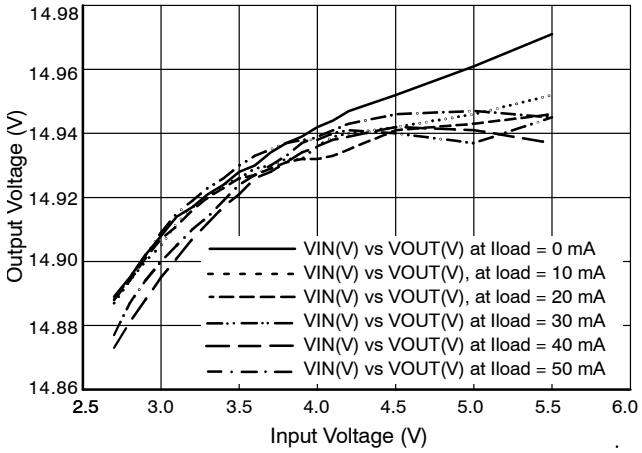


Figure 3. Output Voltage vs Input Voltage

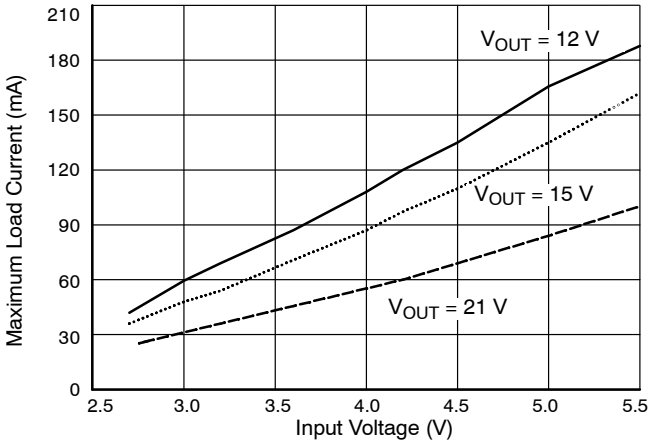


Figure 4. Maximum Load Current vs Input Voltage

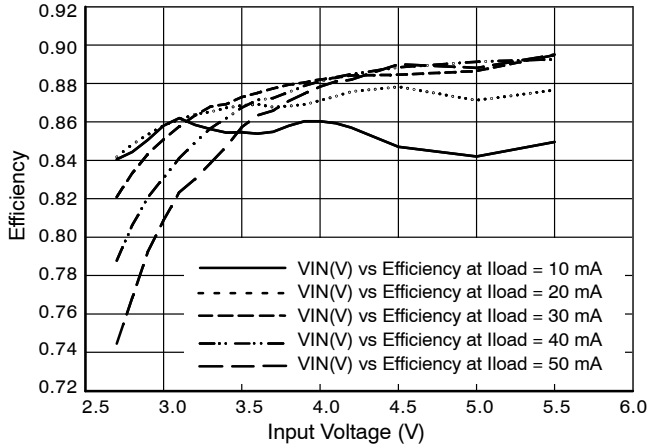


Figure 5. Efficiency vs Input Voltage

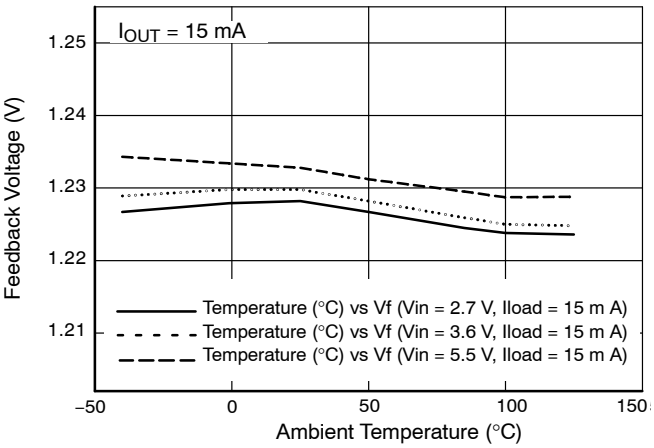


Figure 6. Feedback Voltage vs Ambient Temperature

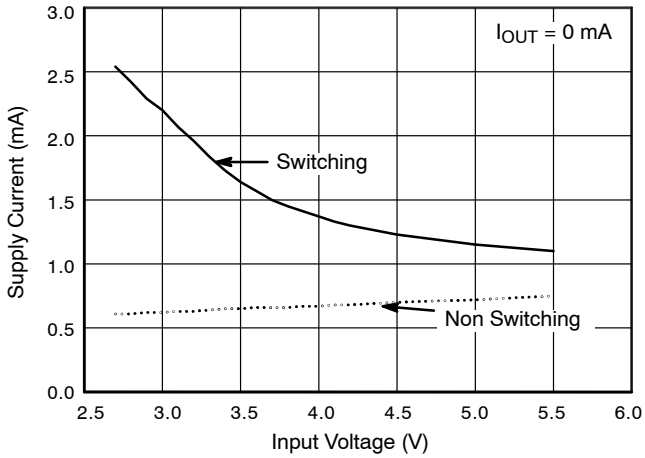


Figure 7. Supply Current vs Input Voltage

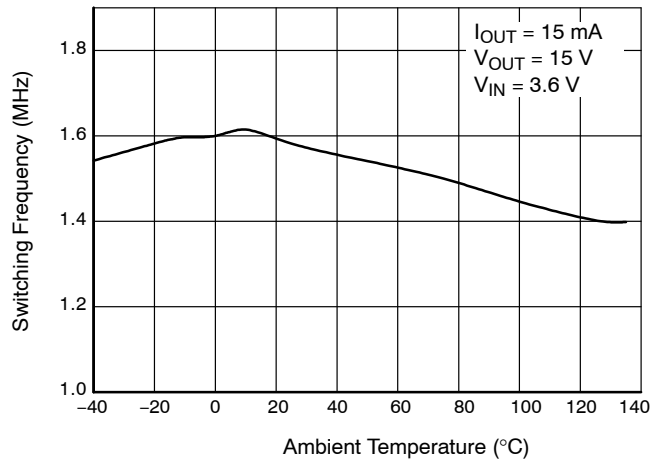


Figure 8. Switching Frequency vs Ambient Temperature

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, Test Circuit Figure 3, unless otherwise noted.

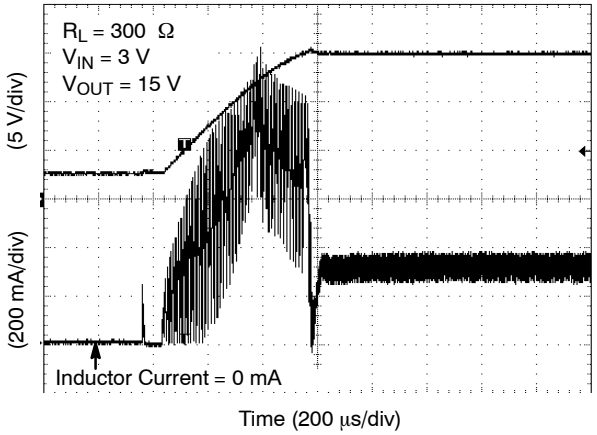


Figure 9. Startup After Enable

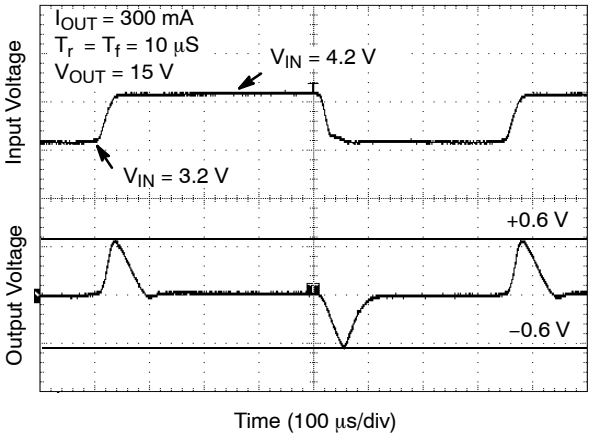


Figure 10. Line Transient Response

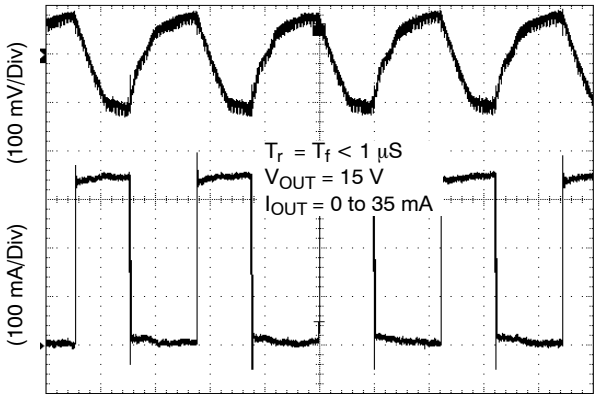


Figure 11. Load Transient Response

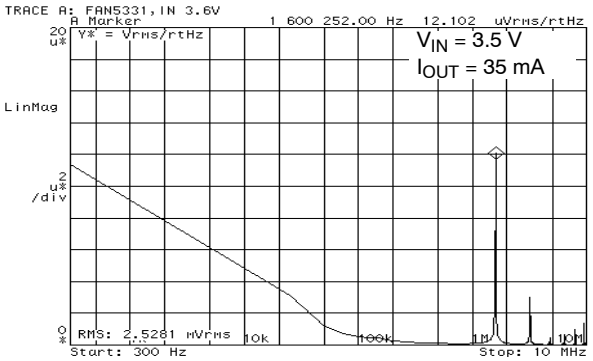


Figure 12. Output Power Spectral Density

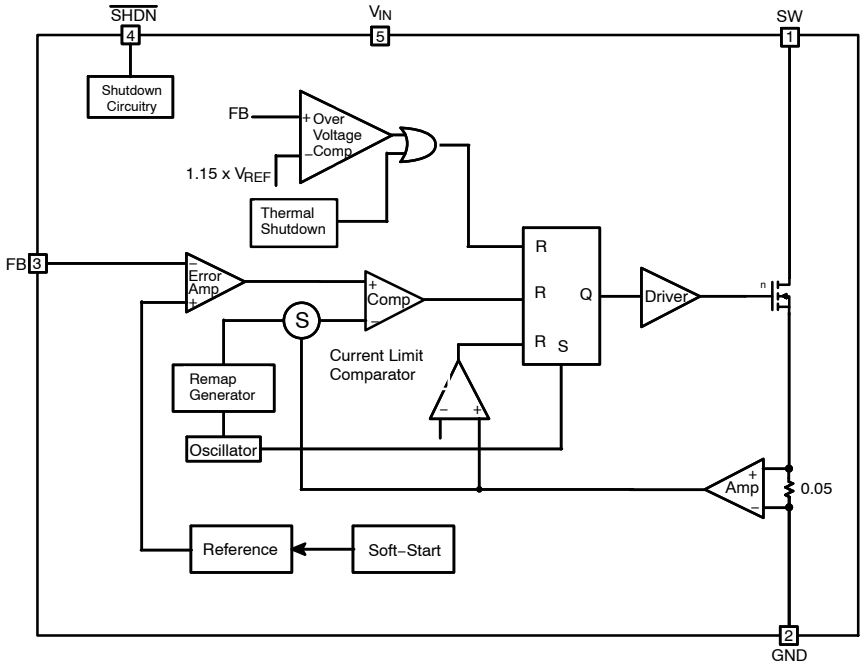


Figure 13. Block Diagram

CIRCUIT DESCRIPTION

The FAN5331 is a pulse−width modulated (PWM) current−mode boost converter. The FAN5331 improves the performance of battery powered equipment by significantly minimizing the spectral distribution of noise at the input caused by the switching action of the regulator. In order to facilitate effective noise filtering, the switching frequency was chosen to be high, 1.6 MHz. An internal soft start circuitry minimizes in−rush currents. The timing of the soft start circuit was chosen to reach 95% of the nominal output voltage within maximum 5 mS following an enable command when V_{IN} = 2.7 V, V_{OUT} = 15 V, I_{LOAD} = 35 mA and $C_{OUT\ (EFFECTIVE)}$ = 3.2 μF.

The device architecture is that of a current mode controller with an internal sense resistor connected in series with the N−channel switch. The voltage at the feedback pin tracks the output voltage at the cathode of the external Schottky diode (shown in the test circuit). The error amplifier amplifies the difference between the feedback voltage and the internal bandgap reference. The amplified error voltage serves as a reference voltage to the PWM comparator. The inverting input of the PWM comparator consists of the sum of two components: the amplified control signal received from the 50 mΩ current sense resistor and the ramp generator voltage derived from the oscillator. The oscillator sets the latch, and the latch turns on the FET switch. Under normal operating conditions, the PWM comparator resets the latch and turns off the FET, thus terminating the pulse. Since the comparator input contains information about the output voltage and the control loop is arranged to form a negative feedback loop, the value of the peak inductor current will be adjusted to maintain regulation.

Every time the latch is reset, the FET is turned off and the current flow through the switch is terminated. The latch can be reset by other events as well. Over−current condition is monitored by the current limit comparator which resets the latch and turns off the switch instantaneously within each clock cycle.

Over−Voltage Protection

The voltage on the feedback pin is sensed by an OVP Comparator. When the feedback voltage is 15% higher than the nominal voltage, the OVP Comparator stops switching of the power transistor, thus preventing the output voltage from going higher.

APPLICATIONS INFORMATION

Setting the Output Voltage

The internal reference is 1.23 V (Typical). The output voltage is divided by a resistor divider, R1 and R2 to the FB pin. The output voltage is given by

$$V_{OUT} = V_{REF}\left(1 + \frac{R_1}{R_2}\right)$$

According to this equation, and assuming desired output voltage of 15 V, good choices for the feedback resistors are, R_1 = 150 kΩ and R_2 = 13.4 kΩ.

Inductor Selection

The inductor parameters directly related to device performances are saturation current and dc resistance. The FAN5331 operates with a typical inductor value of 10 μH. The lower the dc resistance, the higher the efficiency.

Usually a trade−off between inductor size, cost and overall efficiency is needed to make the optimum choice.

The inductor saturation current should be rated around 1 A, which is the threshold of the internal current limit circuit. This limit is reached only during the start−up and with heavy load condition; when this event occurs the converter can shift over in discontinuous conduction mode due to the automatic turn−off of the switching transistor, resulting in higher ripple and reduced efficiency.

Some recommended inductors are suggested in the table below:

Table 1. RECOMMENDED INDUCTORS

Inductor Value	Vendor	Part Number	Comment
10 μH	Panasonic	ELL6GM100M	Lower Profile (1.6 mm)
10 μH	Murata	LQS66SN100M03L	Highest Efficiency
10 μH	Coilcraft	DO1605T−103Mx	Small Size

Capacitors Selection

For best performance, low ESR input and output capacitors are required. Ceramic capacitors in the range 4.7 μF to 10 μF, placed as close to the IC pins, are recommended for the lower input and output ripple. The output capacitor voltage rating should be according to the V_{OUT} setting.

A feed forward capacitor C_F, is required for stability. The recommended value (R_1 x C_F) is around 18 μS. Some capacitors are suggested in the table below.

Table 2. RECOMMENDED CAPACITORS

Capacitor Value	Vendor	Part Number
4.7 μF	Panasonic	ECJ3YB1C475K
4.7 μF	Murata	GRM31CR61C475

Diode Selection

The external diode used for rectification is usually a Schottky diode. Its average forward current and reverse voltage maximum ratings should exceed the load current and the voltage at the output of the converter respectively. A barrier Schottky diode such as BAT54 is preferred, due to its lower reverse current over the temperature range.

Care should be taken to avoid any short circuit of V_{OUT} to GND, even with the IC disabled, since the diode can be instantly damaged by the excessive current.

Thermal Shutdown

When the die temperature exceeds 150°C, a reset occurs and will remain in effect until the die cools to 130°C, at that time the circuit will be allowed to restart.

PCB Layout Recommendations

The inherently high peak currents and switching frequency of power supplies require careful PCB layout design. Therefore, use wide traces for high current paths and place the input capacitor, the inductor, and the output capacitor as close as possible to the integrated circuit terminals. The resistor divider that sets the output voltage should be routed away from the inductor to avoid RF coupling. A four layer PCB with at least one ground plane connected to the pin 2 of the IC is recommended. This ground plane acts as an electromagnetic shield to reduce EMI and parasitic coupling between components.

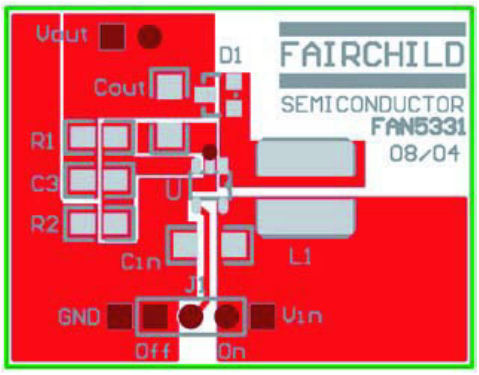


Figure 14. Recommended Layout

APPLICATION EXAMPLES

LED Driver

One or more serial LED strings can be driven with a constant current, set by the series resistor, given by

$$I_{LED} = \frac{1.23V}{R1}$$

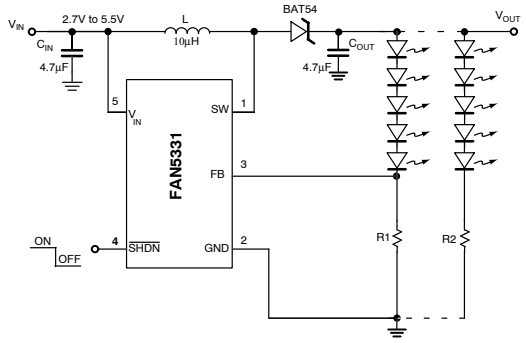


Figure 15. Low Noise Boost LED Driver

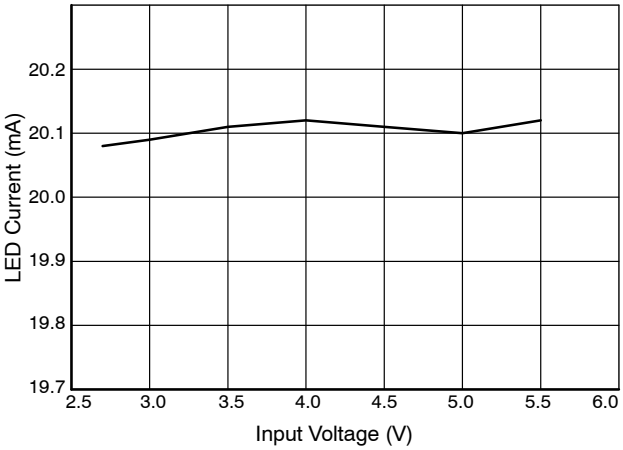


Figure 16. LED Current vs Input Voltage (String Connected to FB Pin)

The feedback loop tightly regulates the current in the branch connected to FB pin, while the current in the other branch depends on the sum of the LED's forward voltages, V_{OUT} and the ballast resistor. The input and the output ripple is less than 3 m V_{RMS}, for load currents up to 40 mA.

A Zener diode (V_Z = 22 V) connected between V_{OUT} and GND can prevent the FAN5331 from being damaged by over−voltage, if the load is accidently disconnected during operation.

Dual Boost Converter

A negative voltage can be provided by adding an external charge pump (C1, C2, D2, and D3).

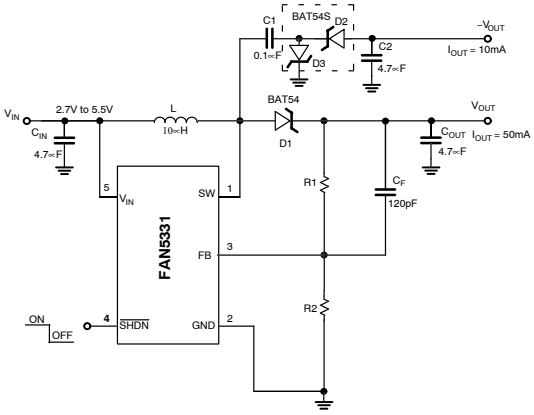


Figure 17. Dual (±) Boost Converter

While the feedback loop tightly regulates V_{OUT}, the negative out− put voltage ($-V_{OUT}$) can supply a light load with a negative voltage. Nevertheless, the negative voltage depends on the changes of the load current in both $-V_{OUT}$ and $+V_{OUT}$, as shown in the graph below.

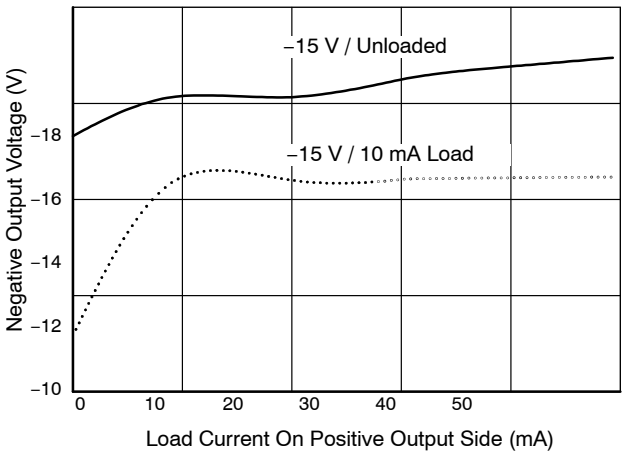


Figure 18. Negative Output Voltage vs Load Current

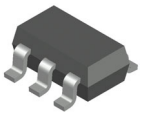
ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)†
FAN5331SX	SOT−23, 5 Lead (Pb−Free/Halogen Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

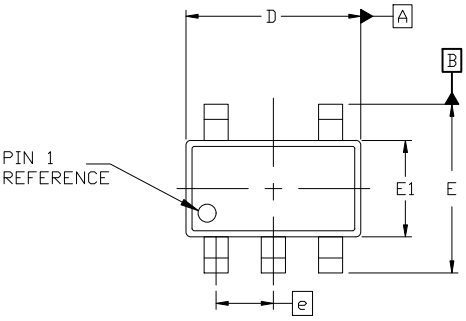
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

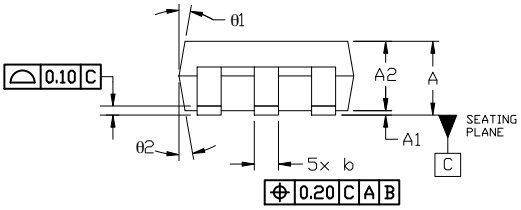


SOT−23, 5 Lead
CASE 527AH
ISSUE A

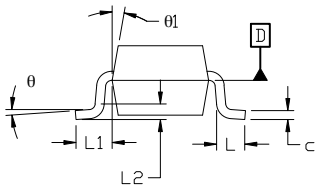
DATE 09 JUN 2021



TOP VIEW



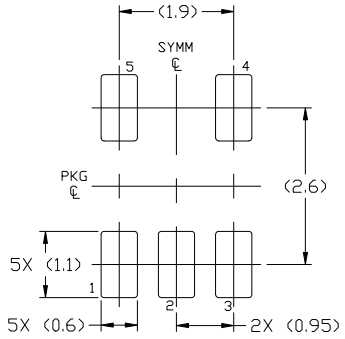
SIDE VIEW



END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 19894
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM D.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07mm.

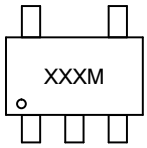
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.90	—	1.45
A1	0.00	—	0.15
A2	0.90	1.15	1.30
b	0.30	—	0.50
c	0.08	—	0.22
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 BSC		
L	0.30	0.45	0.60
L1	0.60 REF		
L2	0.25 REF		
θ	0°	4°	8°
θ1	0°	10°	15°
θ2	0°	10°	15°



RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**SOT−23, 5 LEAD**	**PAGE 1 OF 1**

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