

# High-Current, Half-Bridge, Gate-Driver IC FAN73912



SOIC-16W  
 CASE 751BH

## Description

The FAN73912 is a monolithic half bridge gate-drive IC designed for high-voltage and high-speed driving for MOSFETs and IGBTs that operate up to +1200 V.

The advanced input filter of HIN provides protection against short-pulsed input signals caused by noise.

An advanced level-shift circuit offers high-side gate driver operation up to  $V_S = -9.8$  V (typical) for  $V_{BS} = 15$  V. The UVLO circuit prevents malfunction when VCC and VBS are lower than the specified threshold voltage.

Output drivers typically source and sink 2 A and 3 A, respectively.

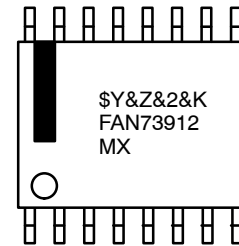
## Features

- Floating Channel for Bootstrap Operation to +1200 V
- Typically 2 A/ 3 A Sourcing/Sinking Current Driving Capability for Both Channels
- Gate Driver Supply (VCC) Range from 12 V to 20 V
- Separate Logic Supply (VDD) Range from 3 V to 20 V
- Extended Allowable Negative VS Swing to -9.8 V for Signal Propagation at VCC = VBS = 15 V
- Built-in Cycle-by-Cycle Edge-Triggered Shutdown Logic
- Built-in Shoot-Through Protection Logic
- Common-Mode dv/dt Noise Canceling Circuit
- UVLO Functions for Both Channels
- Built-in Advanced Input Filter
- Matched Propagation Delay Below 50 ns
- Outputs in-Phase with Input Signal
- Logic and Power Ground +/- 10 V Offset
- This Device is Pb-Free and Halogen Free

## Typical Application

- Electrical Contactor
- UPS
- Solar Inverter
- Ballast
- General-Purpose Half-Bridge Topology

## MARKING DIAGRAM



- \$Y = onsemi Logo
- &Z = Assembly Plant Code
- &2 = 2-Digit Date Code
- &K = Lot Code
- FAN73912MX = Specific Device Code

## ORDERING INFORMATION

Device	Package	Shipping†
FAN73912MX (Note 1)	Wide-16 SOIC	1,000/ Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

1. This device passed wave-soldering test by JESD22A-111

# FAN73912

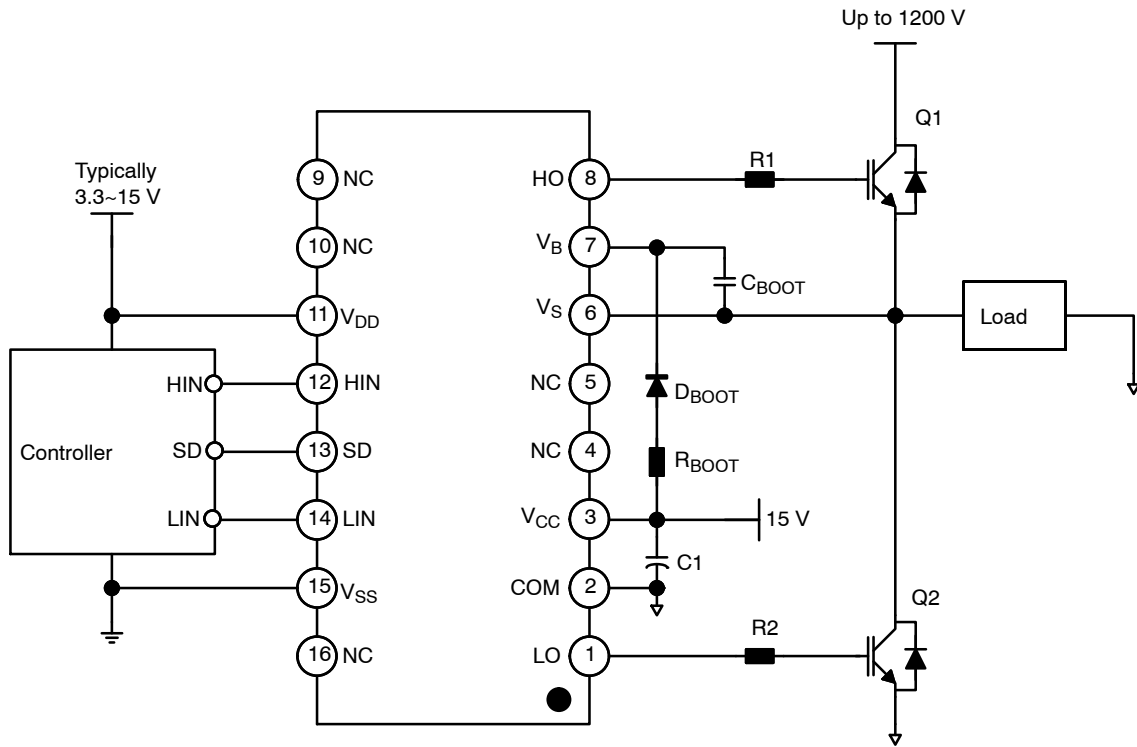


Figure 1. Application Schematic – Adjustable Option

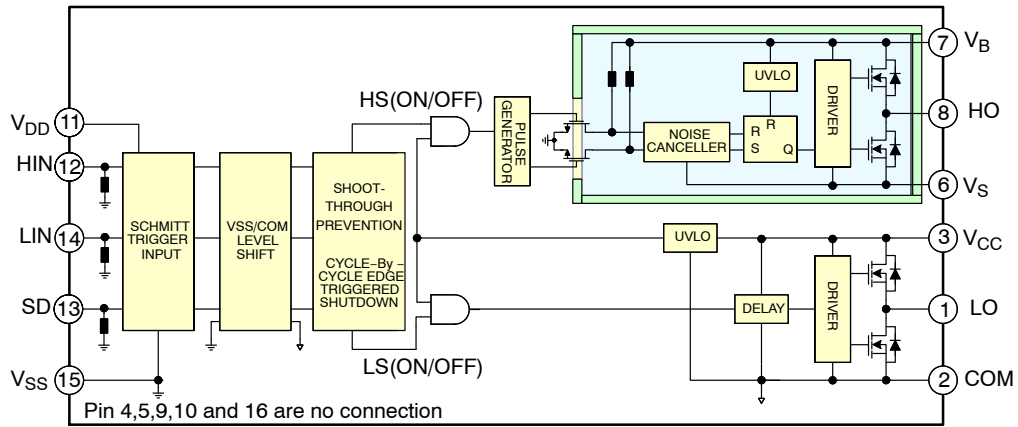
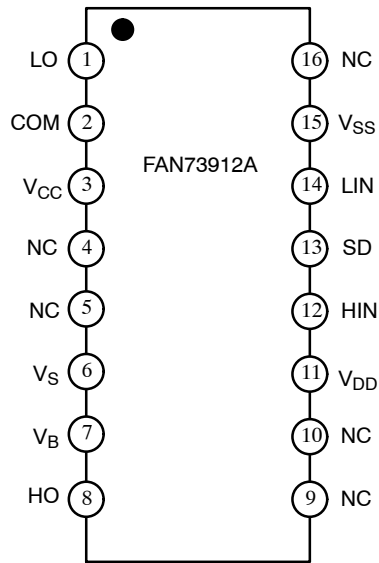


Figure 2. Simplified Block Diagram

## FAN73912



**Figure 3. Pin Connections – Wide 16-SOIC  
(Top View)**

**Table 1. PIN FUNCTION DESCRIPTION**

Pin No.	Symbol	Description
1	LO	Low-Side Driver Output
2	COM	Low-Side Driver Return
3	VCC	Low-Side Supply Voltage
4	NC	No Connection
5	NC	No Connection
6	V <sub>S</sub>	High-Voltage Floating Supply Return
7	V <sub>B</sub>	High-Side Floating Supply
8	HO	High-Side Driver Output
9	NC	No Connection
10	NC	No Connection
11	V <sub>DD</sub>	Logic Supply Voltage
12	HIN	Logic Input for High-Side Gate Driver Output
13	SD	Logic Input for Shutdown
14	LIN	Logic Input for Low-Side Gate Driver Output
15	V <sub>SS</sub>	Logic Ground
16	NC	No Connection

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**Table 2. MAXIMUM RATINGS** ( $T_J = 25^\circ\text{C}$ , unless otherwise specified. All voltage parameters are referenced to COM unless otherwise stated in the table.)

Symbol	Parameter	Min	Max	Unit
$V_B$	High-Side Floating Supply Voltage	-0.3	1225.0	V
$V_S$	High-Side Floating Offset Voltage	$V_B - 25$	$V_B + 0.3$	V
$V_{HO}$	High-Side Floating Output Voltage	$V_S - 0.3$	$V_B + 0.3$	V
$V_{CC}$	Low-Side Supply Voltage	-0.3	25	V
$V_{LO}$	Low-Side Floating Output Voltage	-0.3	$V_{CC} + 0.3$	V
$V_{DD}$	Logic Supply Voltage	$V_{SS} - 0.3$ -0.3	$V_{SS} + 25$ 25	V
$V_{SS}$	Logic GND	$V_{DD} - 25$	$V_{DD} + 0.3$	V
$V_{IN}$	Logic Input Voltage (HIN, LIN and SD)	$V_{SS} + V_{DD} - 25.3$ -0.3	$V_{DD} + 0.3$ 25	V
$dV_S/dt$	Allowable Offset Voltage Slew Rate	-	$\pm 50$	V/ns
$P_D$ (Note 2, 3, 4)	Power Dissipation	-	1.3	W
$\theta_{JA}$	Thermal Resistance	-	95	$^\circ\text{C}/\text{W}$
$T_J$	Junction Temperature	-	150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature	-55	150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Mounted on 76.2 x 114.3 x 1.6 mm PCB (FR-4 glass epoxy material).
- Refer to the following standards:  
 JESD51-2: Integral circuit's thermal test method environmental conditions, natural convection;  
 JESD51-3: Low effective thermal conductivity test board for leaded surface-mount packages.
- Do not exceed maximum power dissipation ( $P_D$ ) under any circumstances.

**Table 3. RECOMMENDED OPERATING CONDITIONS** (All voltage parameters are referenced to COM unless otherwise stated in the table)

Symbol	Parameter	Min	Max	Unit
$V_B$	High-Side Floating Supply Voltage	$V_S + 12$	$V_S + 20$	V
$V_S$	High-Side Floating Supply Offset Voltage (Note 6)	$8 - V_{CC}$	1200	V
$V_{HO}$	High-Side (HO) Output Voltage	$V_S$	$V_B$	V
$V_{CC}$	Low-Side Supply Voltage	12	20	V
$V_{LO}$	Low-Side (LO) Output Voltage	0	$V_{CC}$	V
$V_{DD}$	Logic Supply Voltage	$V_{SS} + 3$ 0	$V_{SS} + 20$ 20	V
$V_{SS}$	Logic Ground (Note 5)	-10	10	V
$V_{IN}$	Logic Input Voltage (HIN, LIN, SD)	$V_{SS} + V_{DD} - 20$ 0	$V_{DD}$ 20	V
$T_J$	Junction Temperature	-40	+125	$^\circ\text{C}$

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

- When  $V_{DD} < 10\text{ V}$ , the minimum  $V_{SS}$  offset is limited to  $-V_{DD}$ .
- Referenced to  $T_J = 25^\circ\text{C}$ .

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**Table 4. STATIC ELECTRICAL CHARACTERISTICS** ( $V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ,  $V_{DD}$ ) = 15.0 V,  $T_J$  = 25°C, unless otherwise specified. The  $V_{IH}$ ,  $V_{IL}$  and  $I_{IN}$  parameters are referenced to  $V_{SS}$  and are applicable to respective input leads: HIN, LIN and SD. The  $V_O$  and  $I_O$  parameters are referenced to  $V_S$  and COM and are applicable to the respective output leads: HO and LO. The  $V_{DDUV}$  parameters are referenced to COM. The  $V_{BSUV}$  parameters are referenced to  $V_{S1, 2, 3}$ .)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>LOW-SIDE POWER SUPPLY SECTION</b>						
$I_{QCC}$	Quiescent $V_{CC}$ Supply Current	$V_{IN} = 0\text{ V or }V_{DD}$	–	170	300	$\mu\text{A}$
$I_{QDD}$	Quiescent $V_{DD}$ Supply Current	$V_{IN} = 0\text{ V or }V_{DD}$	–	–	10	$\mu\text{A}$
$I_{PCC}$	Operating $V_{CC}$ Supply Current	$f_{IN} = 20\text{ kHz, rms }V_{IN} = 15\text{ V}_{PP}$	–	650	950	$\mu\text{A}$
$I_{PDD}$	Operating $V_{DD}$ Supply Current	$f_{IN} = 20\text{ kHz, rms }V_{IN} = 15\text{ V}_{PP}$	–	2	–	$\mu\text{A}$
$I_{SD}$	Shutdown Supply Current	$S_D = V_{DD}$	–	30	50	$\mu\text{A}$
$V_{CCUV+}$	$V_{CC}$ Supply Under-Voltage Positive-Going Threshold Voltage	$V_{CC} = \text{Sweep}$	9.7	11.0	12	V
$V_{CCUV-}$	$V_{CC}$ Supply Under-Voltage Negative-Going Threshold Voltage	$V_{CC} = \text{Sweep}$	9.2	10.5	11.4	V
$V_{CCUVH}$	$V_{CC}$ Supply Under-Voltage Lockout Hysteresis Voltage	$V_{CC} = \text{Sweep}$	–	0.5	–	V
<b>BOOTSTRAPPED SUPPLY SECTION</b>						
$I_{QBS}$	Quiescent $V_{BS}$ Supply Current	$V_{IN} = 0\text{ V or }V_{DD}$	–	50	100	$\mu\text{A}$
$I_{PBS}$	Operating $V_{BS}$ Supply Current	$f_{IN} = 20\text{ kHz, rms value}$	–	550	850	$\mu\text{A}$
$V_{BSUV+}$	$V_{BS}$ Supply Under-Voltage Positive-Going Threshold Voltage	$V_{BS} = \text{Sweep}$	9.7	11.0	12.0	V
$V_{BSUV-}$	$V_{BS}$ Supply Under-Voltage Negative-Going Threshold Voltage	$V_{BS} = \text{Sweep}$	9.2	10.5	11.4	V
$V_{BSUVH}$	$V_{BS}$ Supply Under-Voltage Lockout Hysteresis Voltage	$V_{BS} = \text{Sweep}$	–	0.5	–	V
$I_{LK}$	Offset Supply Leakage Current	$V_B = V_S = 1200\text{ V } (T_J = 25^\circ\text{C})$	–	–	50	$\mu\text{A}$
		$V_B = V_S = 1200\text{ V } (T_J = 125^\circ\text{C})$ (Note 7)	–	–	100	
		$V_B = V_S = 1100\text{ V } (T_J = -40^\circ\text{C})$ (Note 7)	–	–	100	
<b>INPUT LOGIC SECTION (HIN, LIN AND AD)</b>						
$V_{IH}$	Logic "1" Input Voltage	$V_{DD} = 3\text{ V}$	2.4	–	–	V
		$V_{DD} = 15\text{ V}$	9.5	–	–	
$V_{IL}$	Logic "0" Input Voltage	$V_{DD} = 3\text{ V}$	–	–	0.8	V
		$V_{DD} = 15\text{ V}$	–	–	6.0	
$I_{IN+}$	Logic "1" Input bias Current	$V_{IN} = 15\text{ V}$	–	30	50	$\mu\text{A}$
$I_{IN-}$	Logic "0" Input bias Current	$V_{IN} = 0\text{ V}$	–	–	1	$\mu\text{A}$
$R_{IN}$	Logic Input Pull-down Resistance		–	500	–	$\text{k}\Omega$
<b>GATE DRIVER OUTPUT SECTION</b>						
$V_{OH}$	High-Level Output Voltage, $V_{BIAS}-V_O$	$I_O = 0\text{ A}$	–	–	1.2	V
$V_{OL}$	Low-Level Output Voltage, $V_O$	$I_O = 0\text{ A}$	–	–	0.1	V
$I_{O+}$	Output HIGH Short-Circuit Pulse Current	$V_O = 0\text{ V, }V_{IN} = 5\text{ V with }PW \leq 10\ \mu\text{s}$	–	2.0	–	A
$I_{O-}$	Output LOW Short-Circuit Pulsed Current	$V_O = 15\text{ V, }V_{IN} = 0\text{ V with }PW \leq 10\ \mu\text{s}$	–	3.0	–	A
$V_S$	Allowable Negative $V_S$ Pin Voltage for HIN Signal Propagation to HO		–	–9.8	–7.0	V

7. These parameters are guaranteed by design.

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**Table 5. DYNAMIC ELECTRICAL CHARACTERISTICS** ( $V_{BIAS}(V_{CC}, V_{BS}, V_{DD}) = 15.0\text{ V}$ ,  $V_S = V_{SS} = \text{COM}$ ,  $C_L = 1000\text{ pF}$  and  $T_J = 25^\circ\text{C}$ , unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>LOW-SIDE POWER SUPPLY SECTION</b>						
$t_{ON}$	Turn-On Propagation Delay	$V_S = 0\text{ V}$	–	500	–	ns
$t_{OFF}$	Turn-Off Propagation Delay	$V_S = 0\text{ V}$	–	550	–	ns
$t_{FLTIN}$	Input Filtering Time (HIN, LIN) (Note 8)		80	150	220	ns
$t_{FLTSD}$	Input Filtering Time (SD)		–	30	–	ns
$t_{SD}$	Shutdown Propagation Delay Time		260	330	400	ns
$t_R$	Turn-On Rise Time		–	25	–	ns
$t_F$	Turn-Off Fall Time		–	15	–	ns
DT	Dead Time		200	330	450	ns
MDT	Dead Time Matching (Note 9)		–	–	50	ns
MT	Delay Matching, HO & LO Turn-On/OFF (Note 10)		–	–	50	ns
PM	Output Pulse-Width Matching (Note 11)	$PW_{IN} > 1\ \mu\text{s}$	–	50	100	ns

8. The minimum width of the input pulse should exceed 500 ns to ensure the filtering time of the input filter is exceeded.

9. MDT is defined as  $|DT_{HO\_LO} - DT_{LO\_HO}|$  referenced to Figure 40.

10. MT is defined as an absolute value of matching delay time between High-side and Low-Side.

11. PM is defined as an absolute value of matching pulse-width between Input and Output.

TYPICAL CHARACTERISTICS

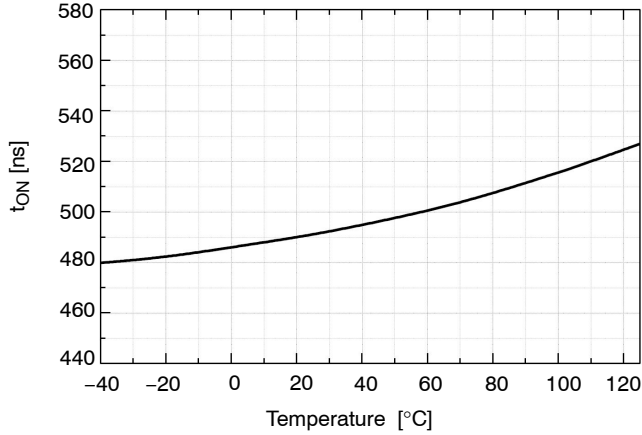


Figure 4. Turn-On Propagation Delay vs. Temperature

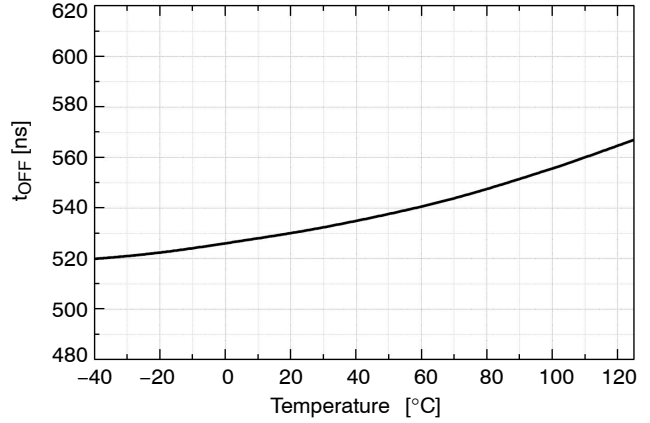


Figure 5. Turn-Off Propagation Delay vs. Temperature

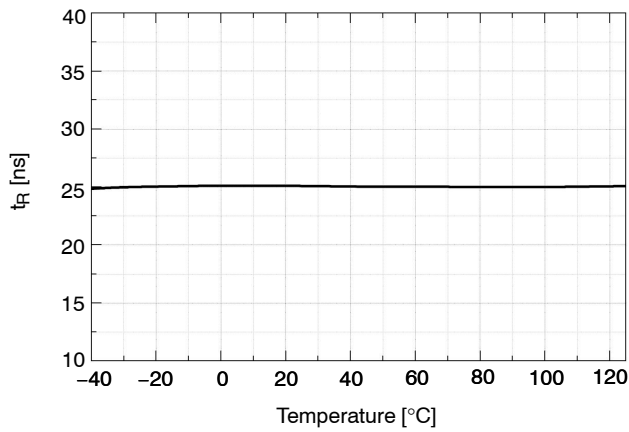


Figure 6. Turn-On Rise Time vs. Temperature

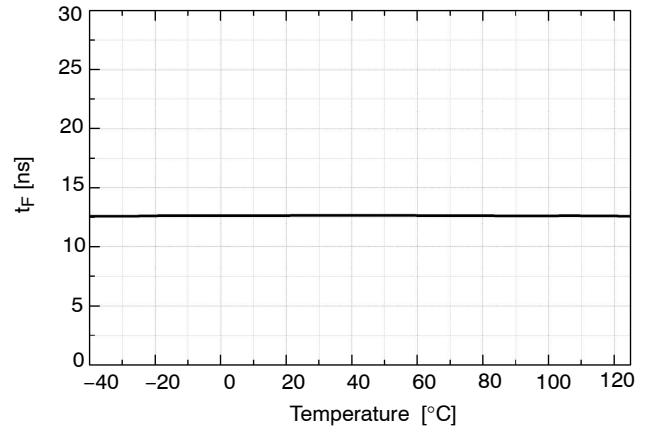


Figure 7. Turn-Off Fall Time vs. Temperature

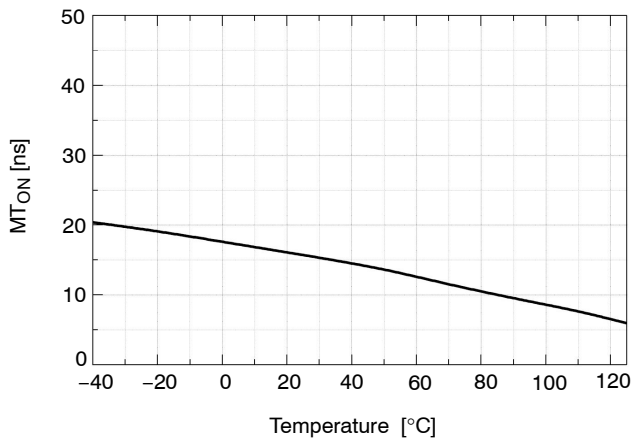


Figure 8. Turn-On Delay Matching vs. Temperature

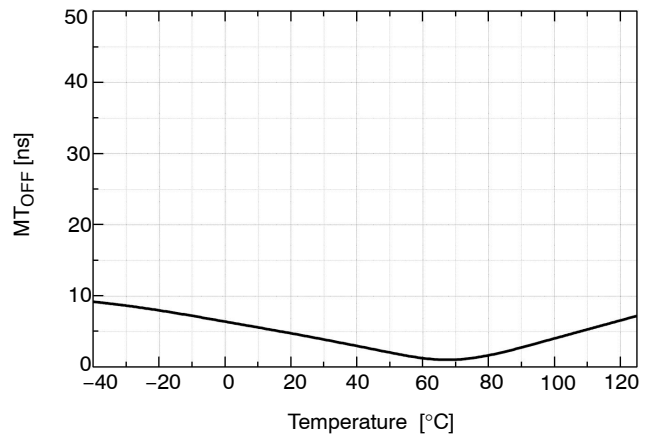


Figure 9. Turn-Off Delay Matching vs. Temperature

TYPICAL CHARACTERISTICS (continued)

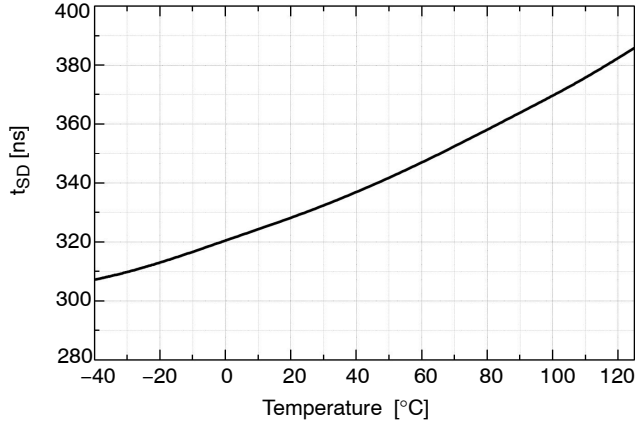


Figure 10. Shutdown Propagation Delay vs. Temperature

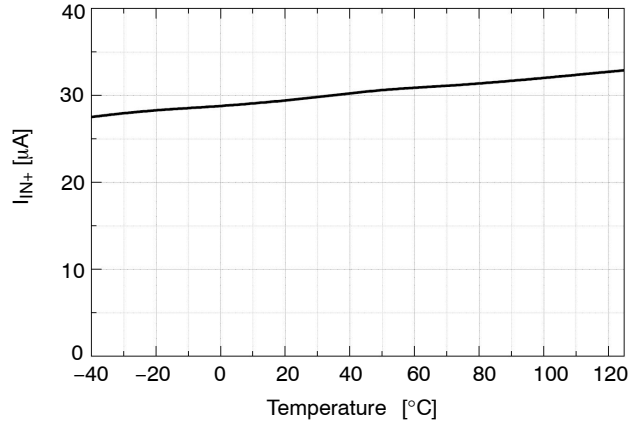


Figure 11. Logic Input High Bias Current vs. Temperature

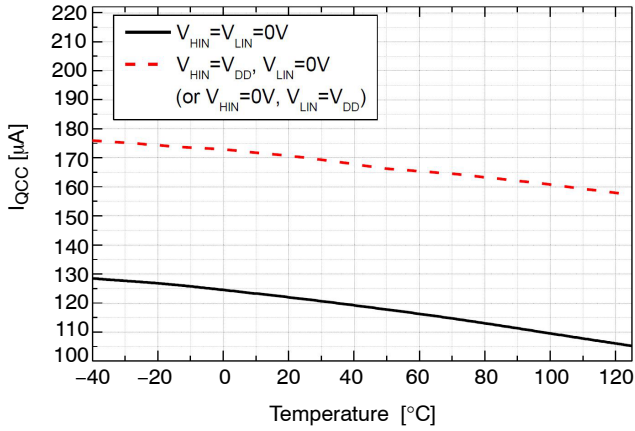


Figure 12. Quiescent V<sub>CC</sub> Supply Current vs. Temperature

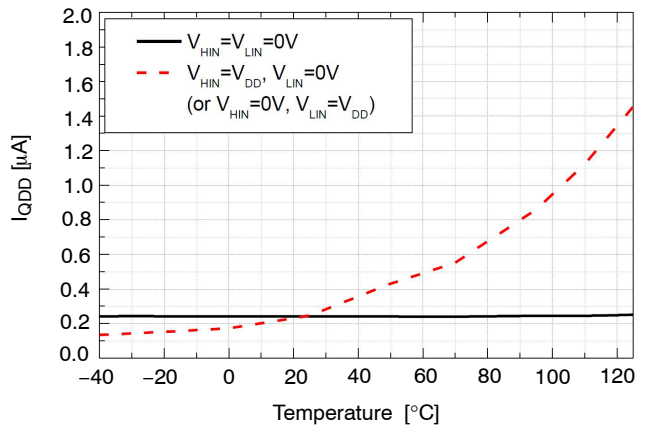


Figure 13. Quiescent V<sub>DD</sub> Supply Current vs. Temperature

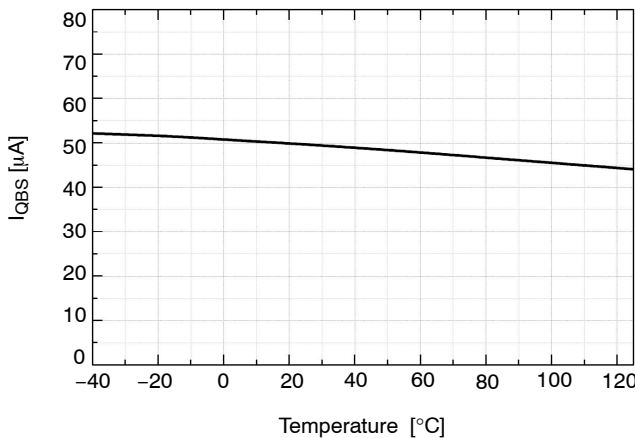


Figure 14. Quiescent V<sub>BS</sub> Supply Current vs. Temperature

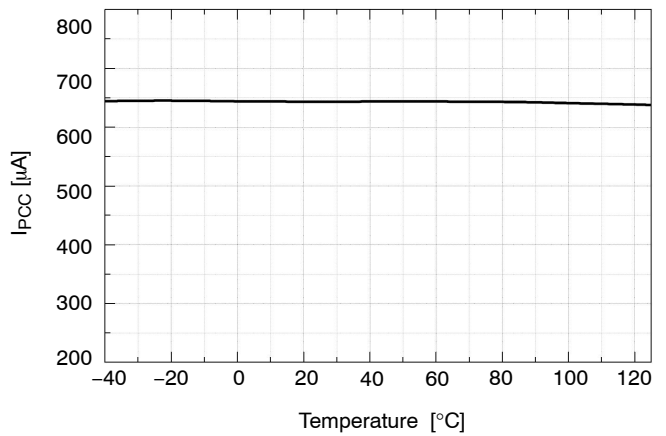


Figure 15. Operating V<sub>CC</sub> Supply Current vs. Temperature



TYPICAL CHARACTERISTICS (continued)

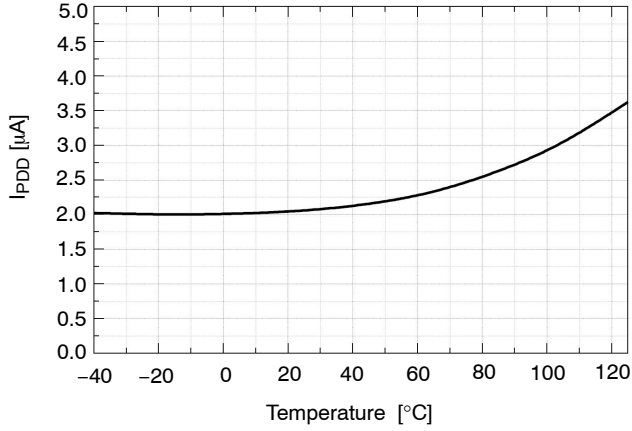


Figure 16. Operating V<sub>DD</sub> Supply Current vs. Temperature

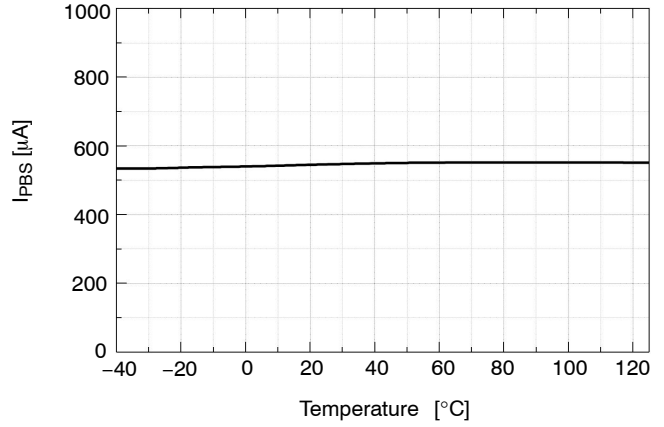


Figure 17. Operating V<sub>BS</sub> Supply Current vs. Temperature

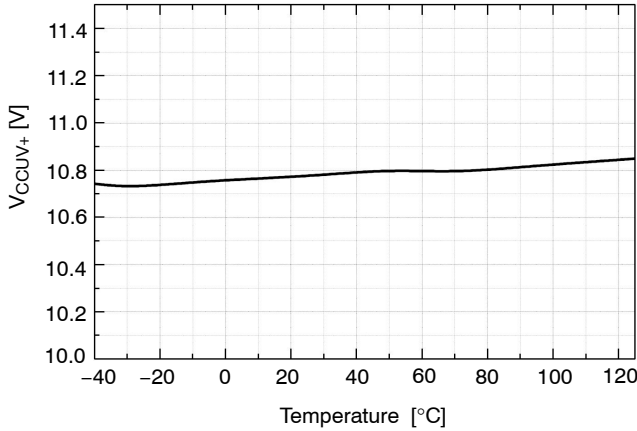


Figure 18. V<sub>CC</sub> UVLO+ vs. Temperature

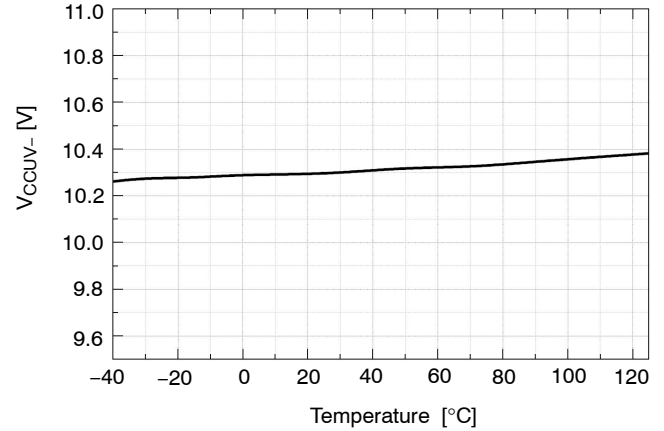


Figure 19. V<sub>CC</sub> UVLO- vs. Temperature

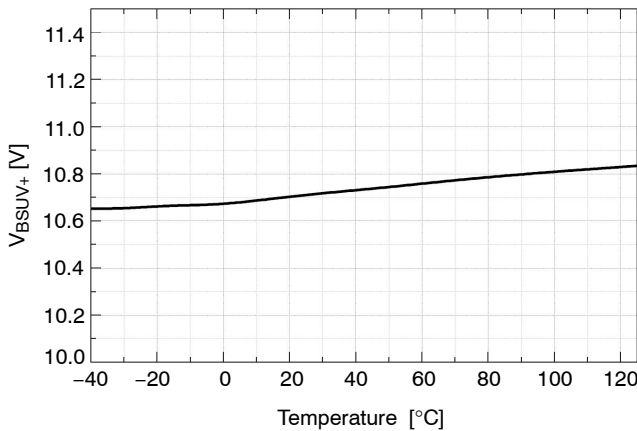


Figure 20. V<sub>BS</sub> UVLO+ vs. Temperature

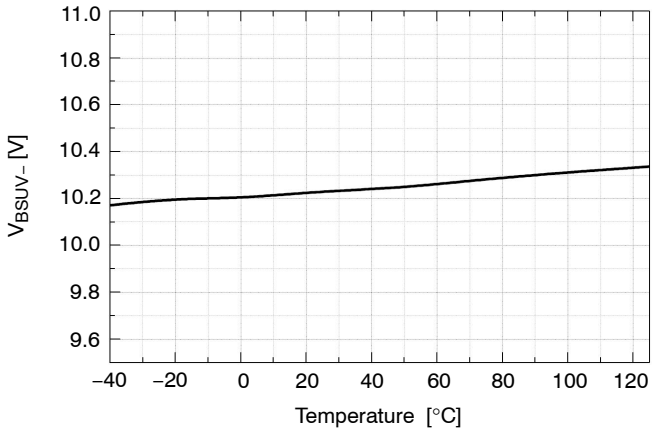


Figure 21. V<sub>BS</sub> UVLO- vs. Temperature

TYPICAL CHARACTERISTICS (continued)

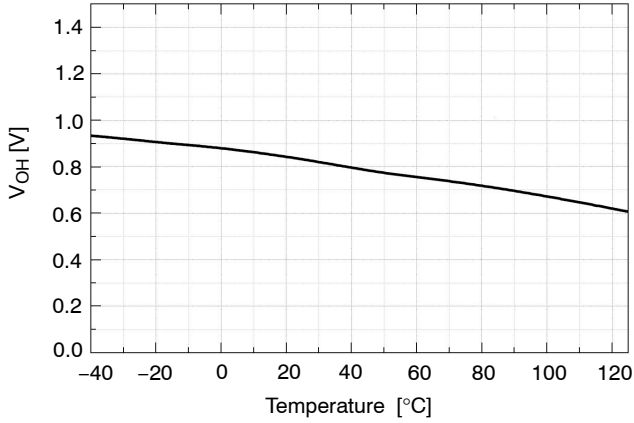


Figure 22. High-Level Output Voltage vs. Temperature

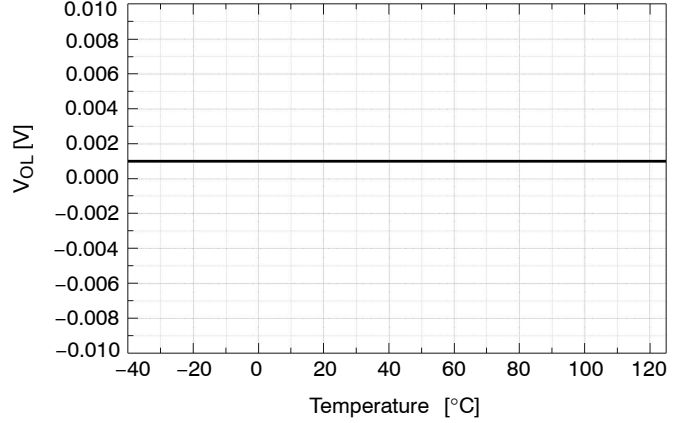


Figure 23. Low-Level Output Voltage vs. Temperature

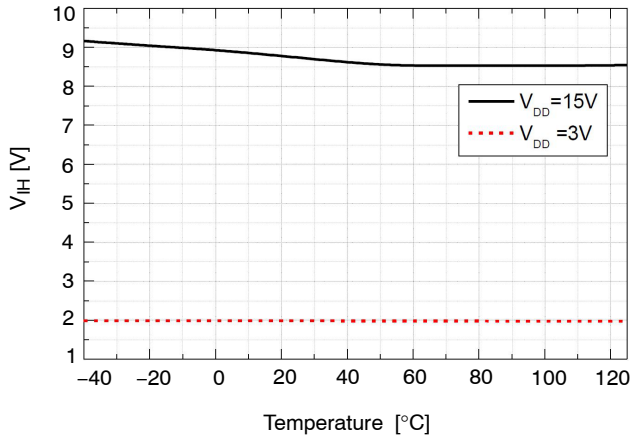


Figure 24. Logic High Input Voltage vs. Temperature

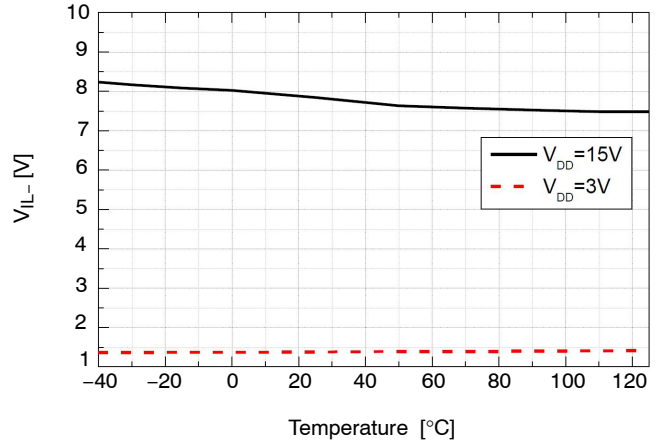


Figure 25. Logic Low Input Voltage vs. Temperature

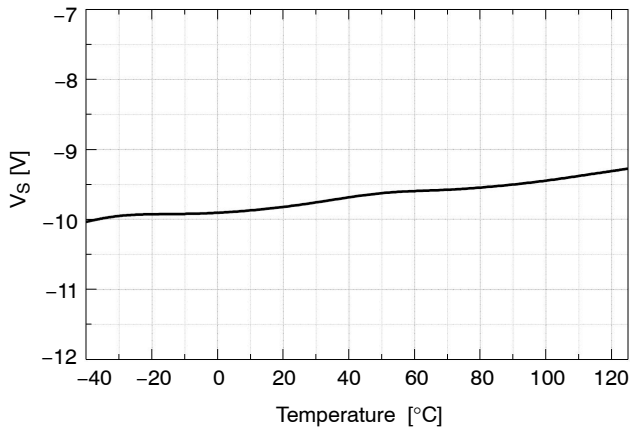


Figure 26. Allowable Negative  $V_S$  vs. Temperature

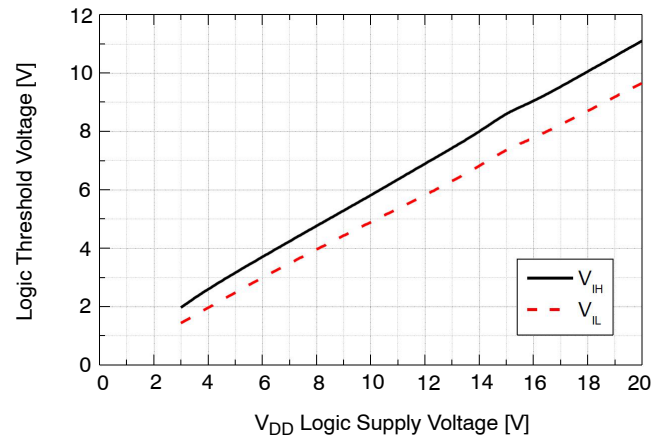
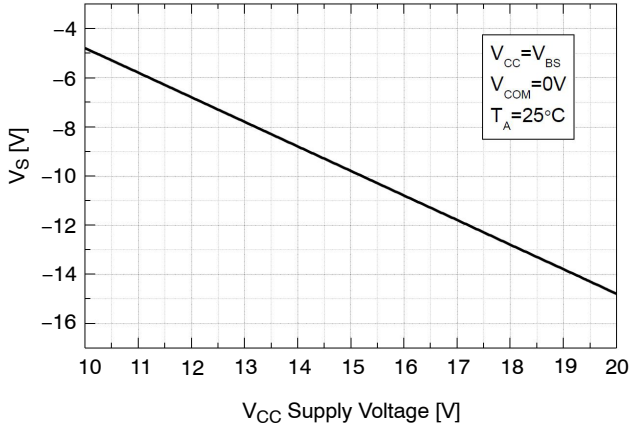
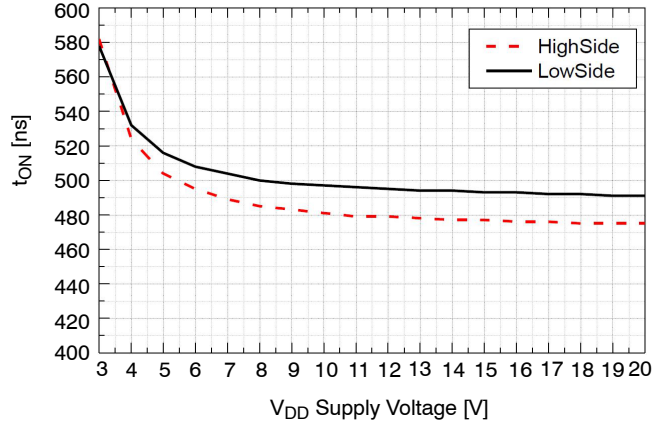


Figure 27. Input Logic (HIN&LIN) Threshold Voltage vs.  $V_{DD}$  Supply Voltage

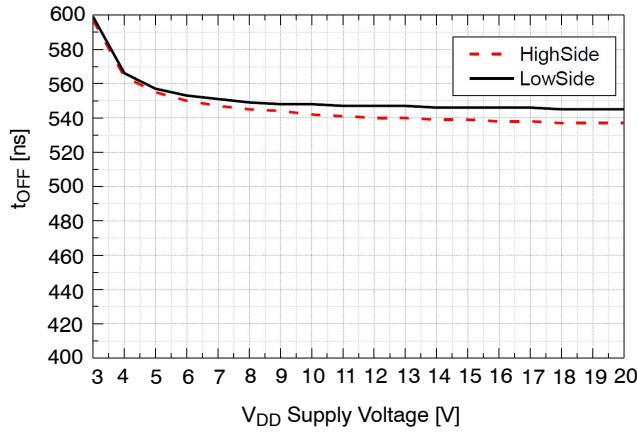
TYPICAL CHARACTERISTICS (continued)



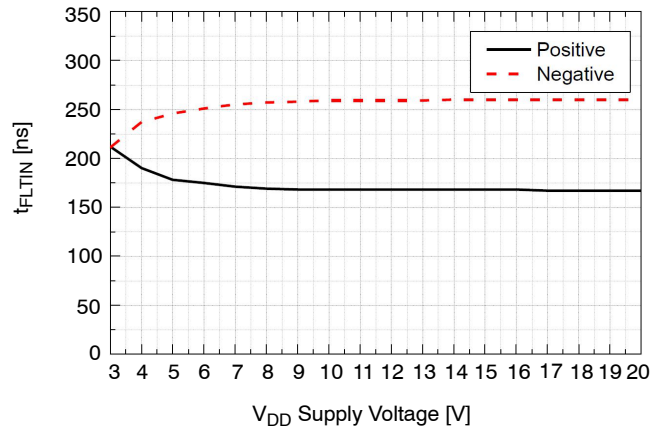
**Figure 28. Allowable Negative  $V_S$  Voltage for HIN Signal Propagation to High Side vs.  $V_{CC}$  Supply Voltage**



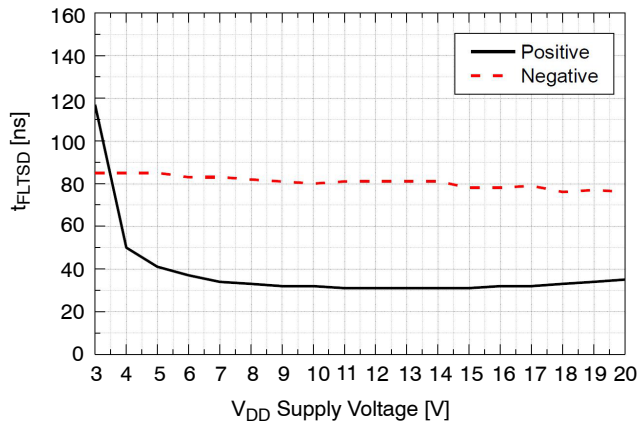
**Figure 29. Turn-On Propagation Delay vs.  $V_{DD}$  Supply Voltage**



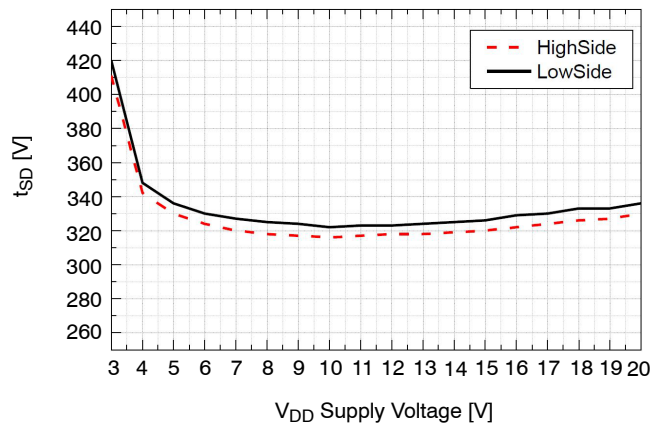
**Figure 30. Turn-Off Propagation Delay vs.  $V_{DD}$  Supply Voltage**



**Figure 31. Logic Input Filtering Time vs.  $V_{DD}$  Supply Voltage**



**Figure 32. Shutdown Input Filtering Time vs.  $V_{DD}$  Supply Voltage**



**Figure 33. Shutdown Propagation Delay vs.  $V_{DD}$  Supply Voltage**

TYPICAL CHARACTERISTICS (continued)

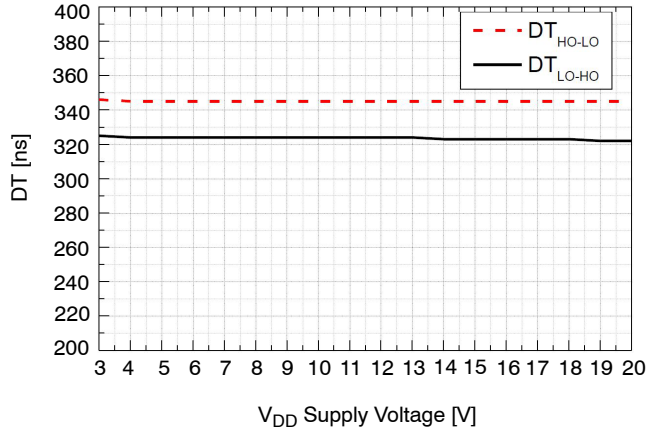


Figure 34. Dead Time vs. V<sub>DD</sub> Supply Voltage

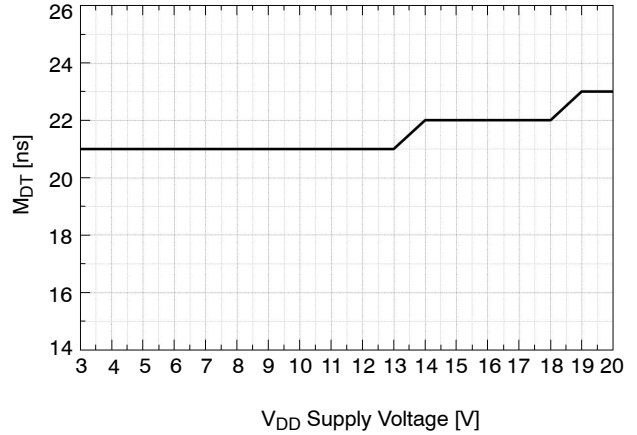


Figure 35. Dead-Time Matching vs. V<sub>DD</sub> Supply Voltage

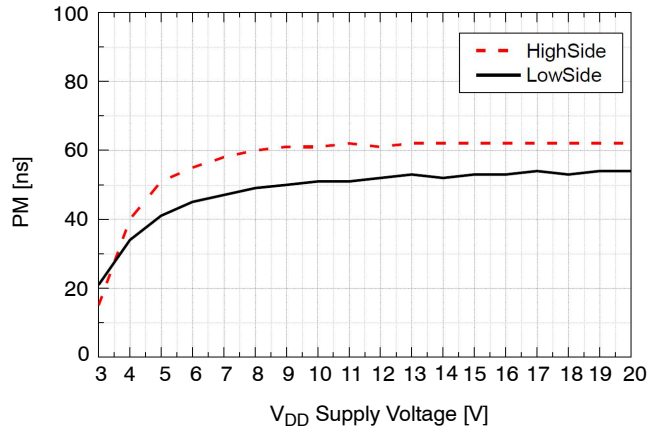


Figure 36. Output Pulse-Width Matching vs. V<sub>DD</sub> Supply Voltage

SWITCHING TIME DEFINITIONS

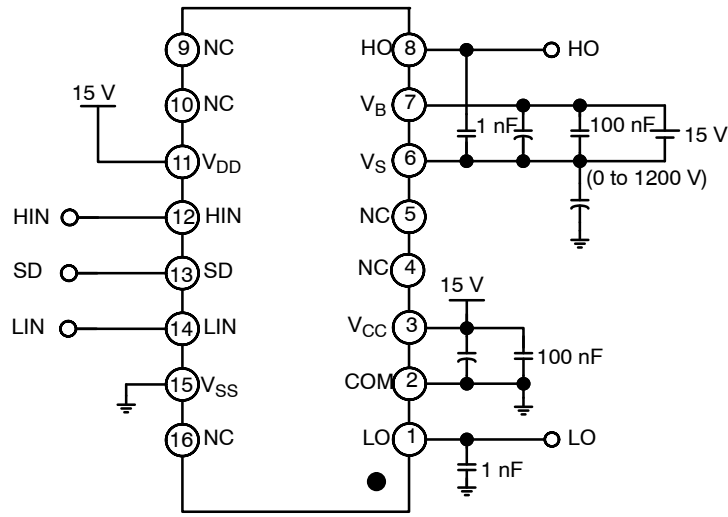


Figure 37. Switching Time Test Circuit

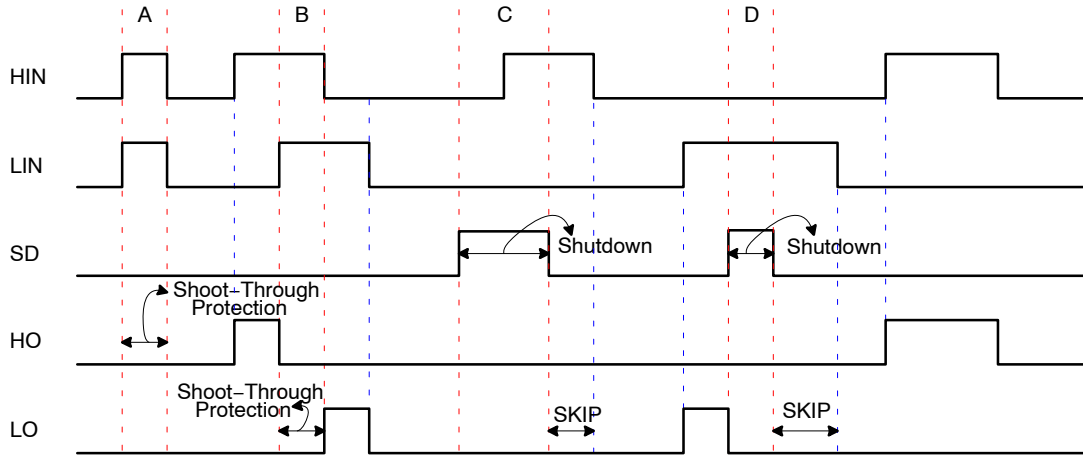


Figure 38. Input/Output Timing Diagram

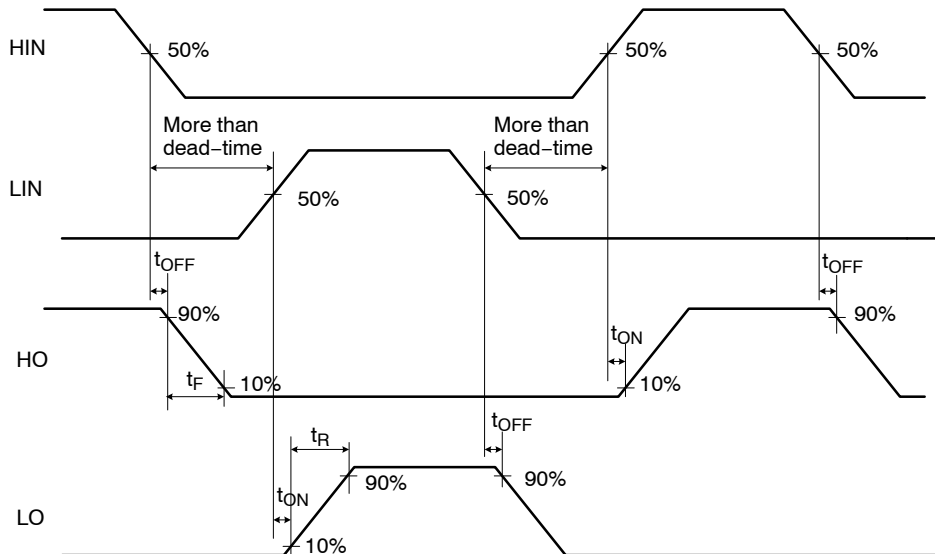


Figure 39. Switching Time Definition

SWITCHING TIME DEFINITIONS (continued)

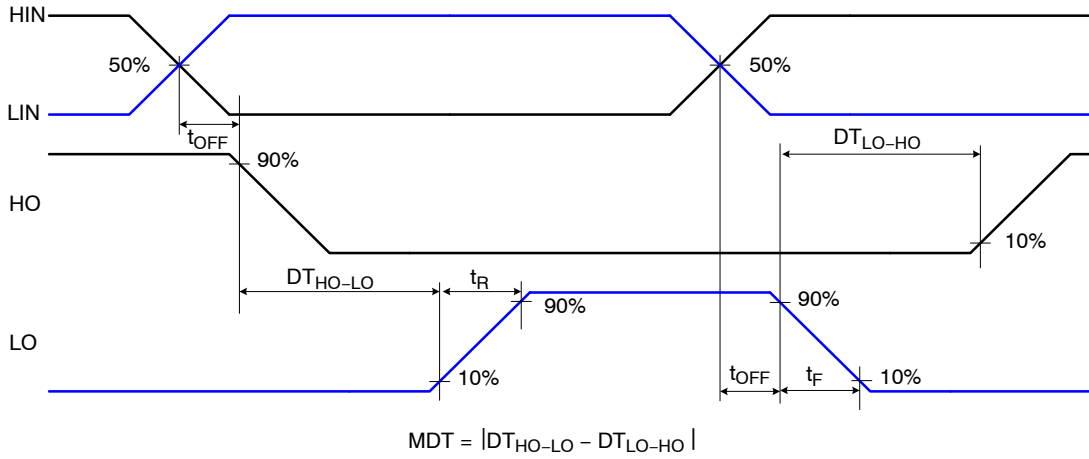


Figure 40. Internal Dead Time Definition

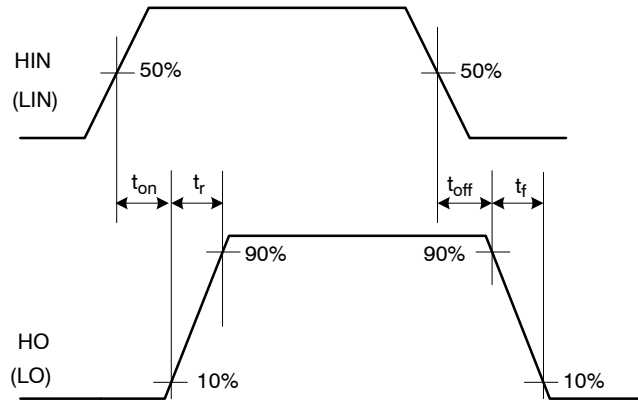


Figure 41. Switching Time Waveform Definitions

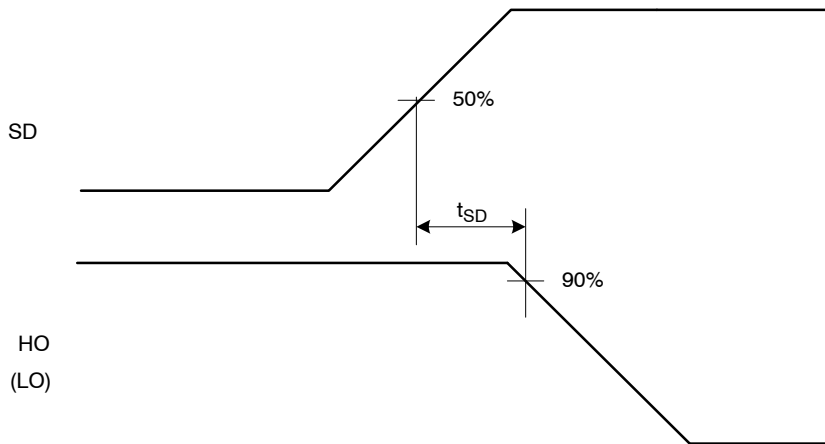


Figure 42. Switching Time Definitions

APPLICATIONS INFORMATION

**Dead Time**

Dead time is automatically inserted whenever the dead time of the external two input signals (between HIN and LIN signals) is shorter than internal fixed dead times (DT1 and DT2). Otherwise, external dead times larger than internal dead times are not modified by the gate driver and internal dead-time waveform definition is shown in Figure 43.

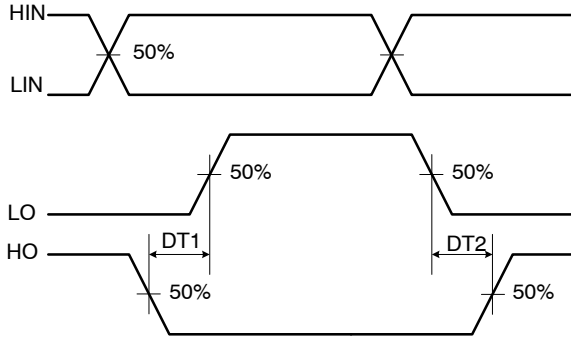


Figure 43. Internal Dead-Time Definitions

**Protection Function**

*Shoot-Through Protection*

The shoot-through protection circuitry prevents both high- and low-side switches from conducting at the same time, as shown in Figure 44.

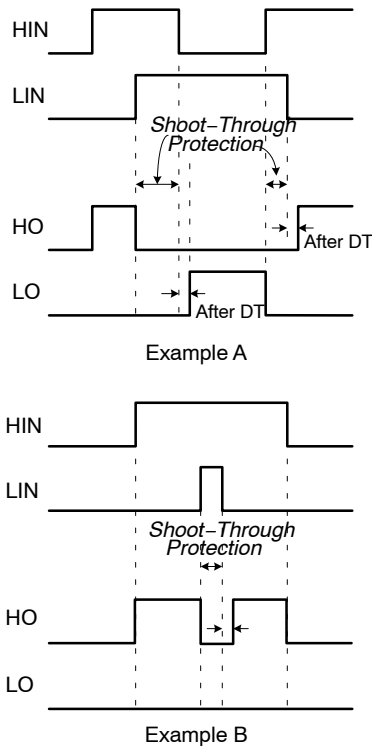


Figure 44. Shoot-Through Protection

**Shutdown Input**

When the SD pin is in LOW state, the gate driver operates normally. When a condition occurs that should shut down the gate driver, the SD pin should be HIGH. The Shutdown circuitry has an input filter; the minimum input duration is specified by  $t_{FLTIN}$  (typically 250 ns).

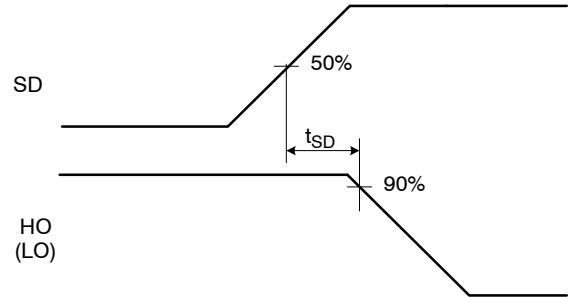


Figure 45. Output Shutdown Timing Waveform

**Noise Filter**

*Input Noise Filter*

Figure 46 shows the input noise filter method, which has symmetry duration between the input signal ( $t_{INPUT}$ ) and the output signal ( $t_{OUTPUT}$ ) and helps to reject noise spikes and short pulses. This input filter is applied to the HIN, LIN, and EN inputs. The upper pair of waveforms (Example A) shows an input signal duration ( $t_{INPUT}$ ) much longer than input filter time ( $t_{FLTIN}$ ); it is approximately the same duration between the input signal time ( $t_{INPUT}$ ) and the output signal time ( $t_{OUTPUT}$ ). The lower pair of waveforms (Example B) shows an input signal time ( $t_{INPUT}$ ) slightly longer than input filter time ( $t_{FLTIN}$ ); it is approximately the same duration between input signal time ( $t_{INPUT}$ ) and the output signal time ( $t_{OUTPUT}$ ).

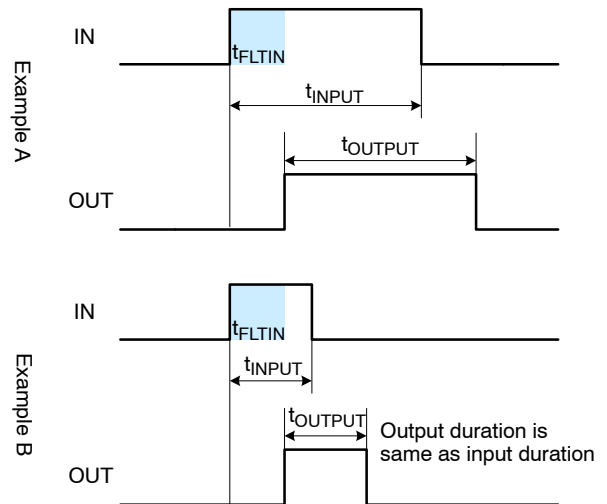
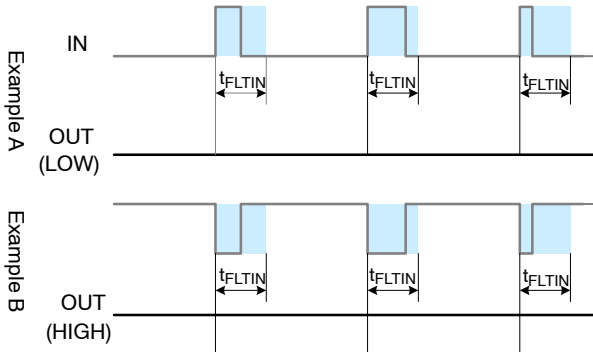


Figure 46. Input Noise Filter Definition

**Short-Pulsed Input Noise Rejection Method**

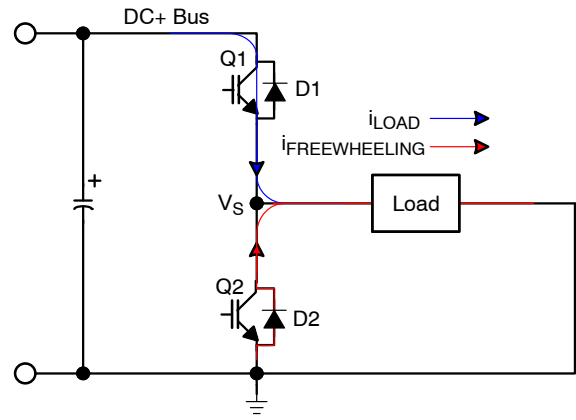
The input filter circuitry provides protection against short-pulsed input signals (HIN, LIN, and SD) on the input signal lines by applied noise signal. If the input signal duration is less than input filter time ( $t_{FLTIN}$ ), the output does not change states. Example A and B of the Figure 47 show the input and output waveforms with short-pulsed noise spikes with a duration less than input filter time; the output does not change states.



**Figure 47. Noise Rejecting Input Filter Definition**

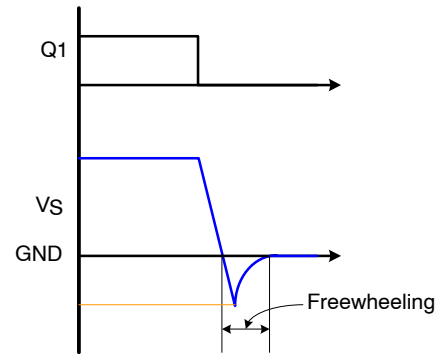
**Negative VS Transient**

The bootstrap circuit has the advantage of being simple and low cost, but has some limitations. The biggest difficulty with this circuit is the negative voltage present at the emitter of the high-side switching device when high-side switch is turned-off in half-bridge application. If the high-side switch, Q1, turns-off while the load current is flowing to an inductive load, a current commutation occurs from high-side switch, Q1, to the diode, D2, in parallel with the low-side switch of the same inverter leg. Then the negative voltage present at the emitter of the high-side switching device, just before the freewheeling diode, D2, starts clamping, causes load current to suddenly flow to the low-side freewheeling diode, D2, as shown in Figure 48.



**Figure 48. Half-Bridge Application Circuits**

This negative voltage can be trouble for the gate driver’s output stage, there is the possibility to develop an overvoltage condition of the bootstrap capacitor, input signal missing and latch-up problems because it directly affects the source VS pin of the gate driver, shown in Figure 49. This undershoot voltage is called “negative VS transient”.



**Figure 49. VS Waveforms during Q1 Turn-Off**



Figure 50 and Figure 51 show the commutation of the load current between high-side switch, Q1, and low-side freewheeling diode, D3, in same inverter leg. The parasitic inductances in the inverter circuit from the die wire bonding to the PCB tracks are jumped together in  $L_C$  and  $L_E$  for each IGBT. When the high-side switch, Q1, and low-side switch, Q4, are turned on, the  $V_{S1}$  node is below DC+ voltage by the voltage drops associated with the power switch and the parasitic inductances of the circuit due to load current is flows from Q1 and Q4, as shown in Figure 50. When the high-side switch, Q1, is turned off and Q4, remained turned on, the load current, to flows the low-side freewheeling diode, D3, due to the inductive load connected to  $V_{S1}$  as shown in Figure 51. Q1 Turn-Off and D3 Conducting. The current flows from ground (which is connected to the COM pin of the gate driver) to the load and the negative voltage present at the emitter of the high-side switching device. In this case, the COM pin of the gate driver is at a higher potential than the  $V_S$  pin due to the voltage drops associated with freewheeling diode, D3, and parasitic elements,  $L_{C3}$  and  $L_{E3}$ .

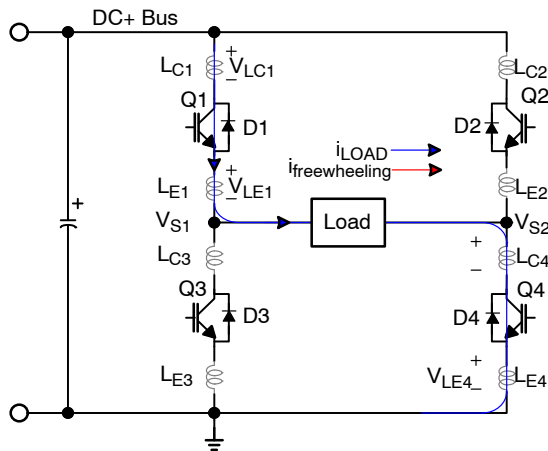


Figure 50. Q1 and Q4 Turn-On

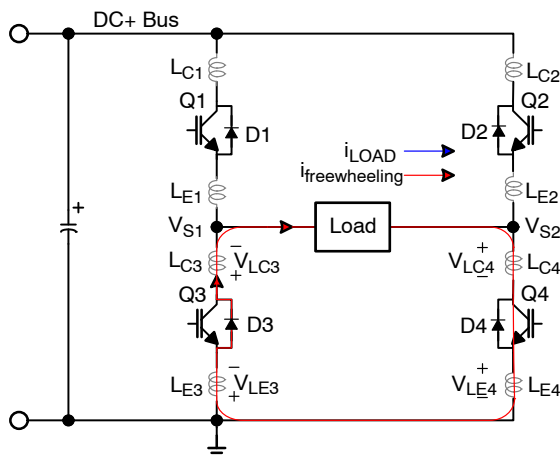


Figure 51. Q1 Turn-Off and D3 Conducting

The FAN73912 has a typical negative  $V_S$  transient characteristics, as shown in Figure 52.

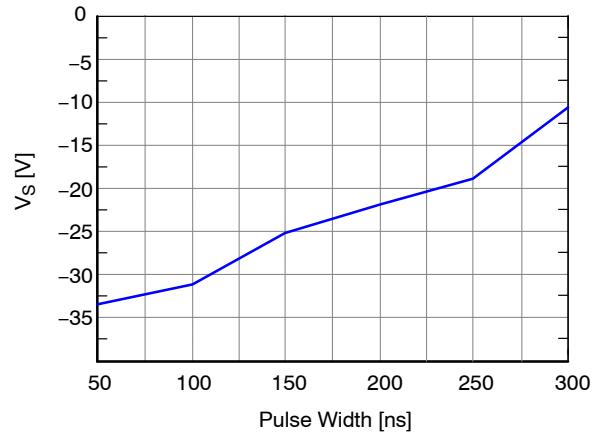


Figure 52. Negative  $V_S$  Transient Characteristic

Even though the FAN73912 has been shown able to handle these negative  $V_S$  transient conditions, it is strongly recommended that the circuit designer limit the negative  $V_S$  transient as much as possible by careful PCB layout to minimize the value of parasitic elements and component use. The amplitude of negative  $V_S$  voltage is proportional to the parasitic inductances and the turn-off speed,  $di/dt$ , of the switching device.

### General Guidelines

#### Printed Circuit Board Layout

The layout recommended for minimized parasitic elements is as follows:

- Direct tracks between switches with no loops or deviation.
- Avoid interconnect links. These can add significant inductance.
- Reduce the effect of lead-inductance by lowering package height above the PCB.
- Consider co-locating both power switches to reduce track length.
- To minimize noise coupling, the ground plane should not be placed under or near the high-voltage floating side.
- To reduce the EM coupling and improve the power switch turn-on/off performance, the gate drive loops must be reduced as much as possible.

#### Placement of Components

The recommended placement and selection of component as follows:

- Place a bypass capacitor between the  $V_{CC}$  and  $V_{SS}$  pins. A ceramic 1  $\mu$ F capacitor is suitable for most applications. This component should be placed as close as possible to the pins to reduce parasitic elements.

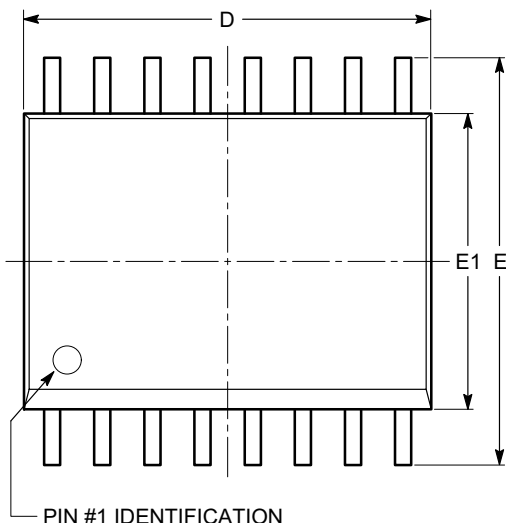
## FAN73912

- The bypass capacitor from  $V_{CC}$  to  $V_{SS}$  supports both the low-side driver and bootstrap capacitor recharge. A value at least ten times higher than the bootstrap capacitor is recommended.
- The bootstrap resistor,  $R_{BOOT}$ , must be considered in sizing the bootstrap resistance and the current developed during initial bootstrap charge. If the resistor is needed in series with the bootstrap diode, verify that  $V_B$  does not fall below COM (ground). Recommended use is typically  $5 \sim 10 \Omega$  that increase the  $V_{BS}$  time constant. If the voltage drop of bootstrap resistor and diode is too high or the circuit topology does not allow a sufficient charging time, a fast recovery or ultra-fast recovery diode can be used.
- The bootstrap capacitor,  $C_{BOOT}$ , uses a low-ESR capacitor, such as ceramic capacitor. It is strongly recommended that the placement of components is as follows:
  - Place components tied to the floating voltage pins ( $V_B$  and  $V_S$ ) near the respective high-voltage portions of the device and the FAN73912. Not Connected (NC) pins in this package maximize the distance between the high-voltage and low-voltage pins (see Figure 3).
  - Place and route for bypass capacitors and gate resistors as close as possible to gate drive IC.
  - Locate the bootstrap diode,  $D_{BOOT}$ , as close as possible to bootstrap capacitor,  $C_{BOOT}$ .
  - The bootstrap diode must use a lower forward voltage drop and minimal switching time as soon as possible for fast recovery or ultra-fast diode.



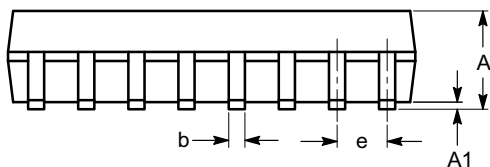
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**CASE 751BH-01**  
**ISSUE A**

DATE 18 MAR 2009

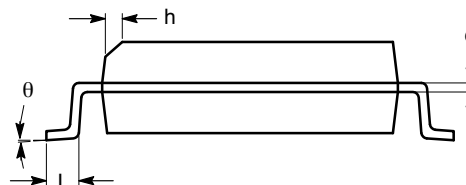


**TOP VIEW**

SYMBOL	MIN	NOM	MAX
A	2.36	2.49	2.64
A1	0.10		0.30
b	0.33	0.41	0.51
c	0.18	0.23	0.28
D	10.08	10.31	10.49
E	10.01	10.31	10.64
E1	7.39	7.49	7.59
e	1.27 BSC		
h	0.25		0.75
L	0.38	0.81	1.27
$\theta$	0°		8°



**SIDE VIEW**



**END VIEW**

**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-013.

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