MOSFET – N-Channel, SUPERFET® II, FRFET®

650 V, 24 A, 150 mΩ

FCPF150N65F

V_{DS}	$R_{DS(ON)}$ MAX	I_D MAX
650 V	150 mΩ @ 10 V	24 A*

*Drain current limited by maximum junction temperature.

Description

SUPERFET II MOSFET is **onsemi**'s brand−new high voltage super−junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on−resistance and lower gate charge performance. SUPERFET II FRFET MOSFET combines a faster and more rugged intrinsic body diode performance with fast switching, aimed at achieving better reliability and efficiency especially in resonant switching applications. SUPERFET II FRFET is very suitable for the switching power applications such as server/telecom power, Solar inverter, FPD TV power, computing power, lighting and industrial power applications.
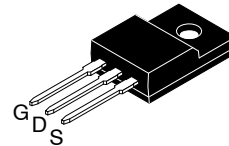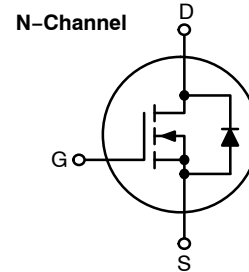
Features

- 700 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 133 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 72 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 361 pF)
- 100% Avalanche Tested
- RoHS Compliant

Applications

- Telecom / Server Power Supplies
- Solar Inverters
- Computing Power Supplies
- FPD TV Power / Lighting

N−Channel

TO−220 Fullpack, 3−Lead / TO−220F−3SG CASE 221AT

MARKING DIAGRAM

FCPF15
0N65F
AYWWZZ

FCPF150N65F = Device Code
A = Assembly Location
YWW = Date Code (Year & Week)
ZZ = Assembly Lot

ORDERING INFORMATION

Device	Package	Shipping
FCPF150N65F	TO−220F	1000 Units / Tube

January, 2024 – Rev. 2

FCPF150N65F

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage	−DC	±20	V
		−AC (f > 1 Hz)	±30	
I_D	Drain Current	− Continuous (T_C = 25°C)	24*	A
		− Continuous (T_C = 100°C)	14.9*	
I_{DM}	Drain Current	− Pulsed (Note 1)	72*	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		663	mJ
I_{AR}	Avalanche Current (Note 1)		4.7	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		2.98	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		50	
P_D	Power Dissipation	(T_C = 25°C)	39	W
		−Derate above 25°C	0.31	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*Drain current limited by maximum junction temperature.
1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. I_{AS} = 4.7 A, R_G = 25 Ω, starting T_J = 25°C.
3. $I_{SD} \leq$ 12 A, di/dt $\leq$ 200 A/μs, $V_{DD} \leq$ 380 V, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	3.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 10 mA, T_J = 25°C	650	–	–	V
		V_{GS} = 0 V, I_D = 10 mA, T_J = 150°C	700	–	–	
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, referenced to 25°C	–	0.72	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V	–	–	10	μA
		V_{DS} = 520 V, V_{GS} = 0 V, T_C = 125°C	–	86	–	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 2.4 mA	3	–	5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 12 A	–	133	150	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 12 A	–	22	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 100 V, V_{GS} = 0 V, f = 1 MHz	–	2810	3737	pF
C_{oss}	Output Capacitance		–	91	121	pF
C_{rss}	Reverse Transfer Capacitance		–	0.77	–	pF
C_{oss}	Output Capacitance	V_{DS} = 380 V, V_{GS} = 0 V, f = 1 MHz	–	54	–	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	361	–	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS} = 380 V, I_D = 12 A, V_{GS} = 10 V (Note 4)	–	72	94	nC
Q_{gs}	Gate to Source Gate Charge		–	15	–	nC
Q_{gd}	Gate to Drain "Miller" Charge		–	31	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	0.69	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 380 V, I_D = 12 A, V_{GS} = 10 V, R_G = 4.7 Ω (Note 4)	–	28	66	ns
t_r	Turn–On Rise Time		–	15	40	ns
$t_{d(off)}$	Turn–Off Delay Time		–	73	156	ns
t_f	Turn–Off Fall Time		–	6	22	ns
DRAIN–SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Drain to Source Diode Forward Current		–	–	24	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	72	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 12 A	–	–	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 12 A, dI_F/dt = 100 A/μs	–	123	–	ns
Q_{rr}	Reverse Recovery Charge		–	597	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
4. Essentially independent of operating temperature.
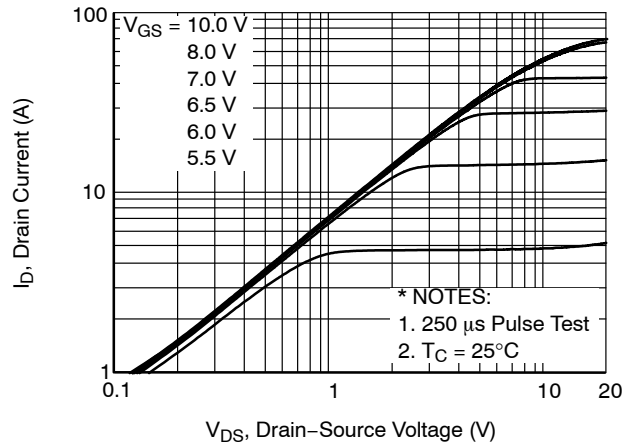
TYPICAL PERFORMANCE CHARACTERISTICS
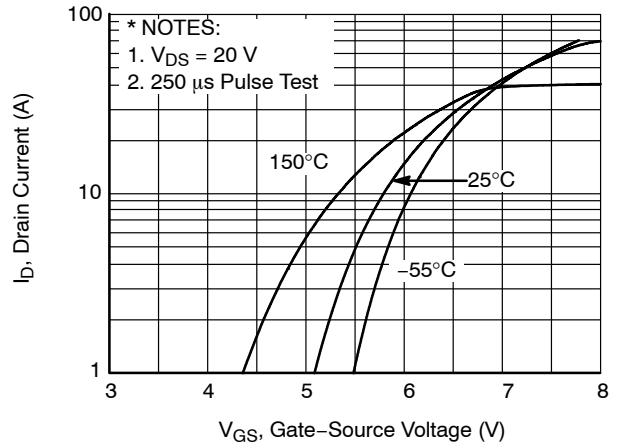
Figure 1. On−Region Characteristics

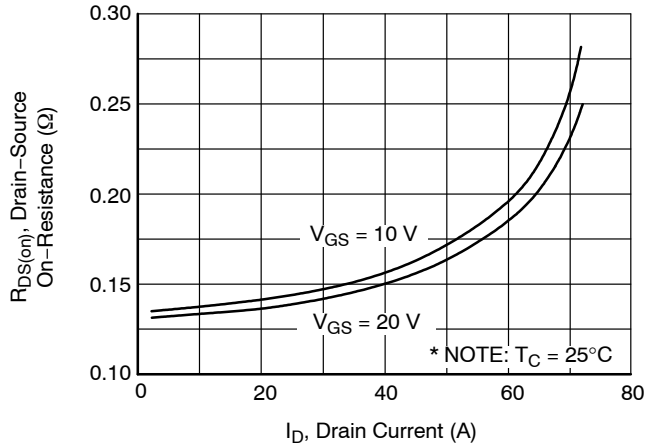Figure 2. Transfer Characteristics

Figure 3. On−Resistance Variation vs. Drain
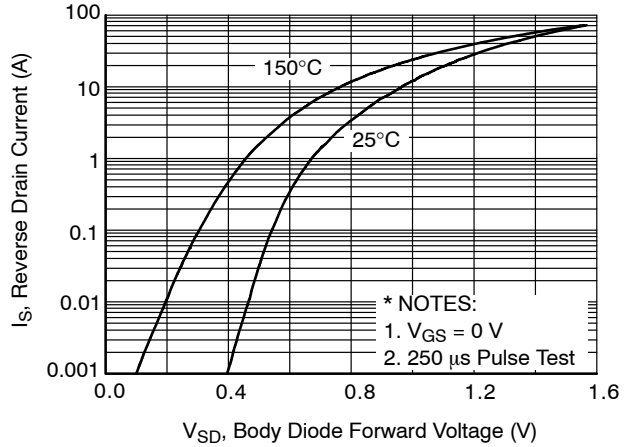Current and Gate Voltage

Figure 4. Body Diode Forward Voltage
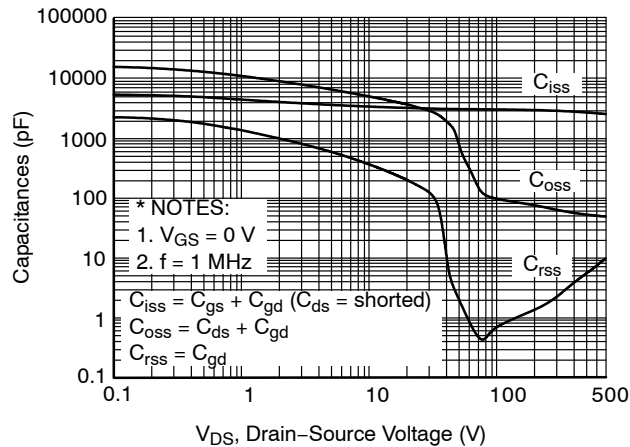Variation vs. Source Current and Temperature
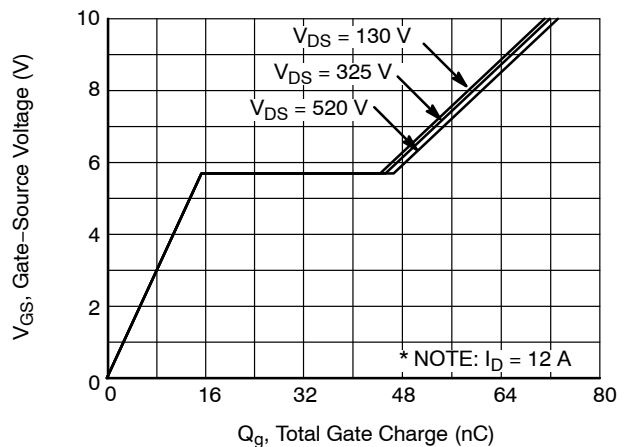
Figure 5. Capacitance Characteristics

Figure 6. Gate Charge Characteristics

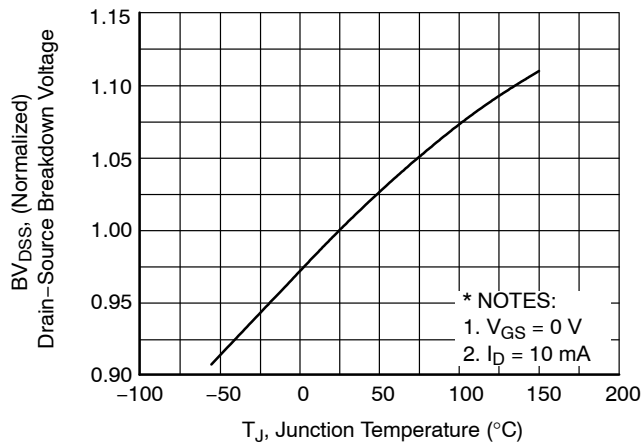**TYPICAL PERFORMANCE CHARACTERISTICS** (continued)
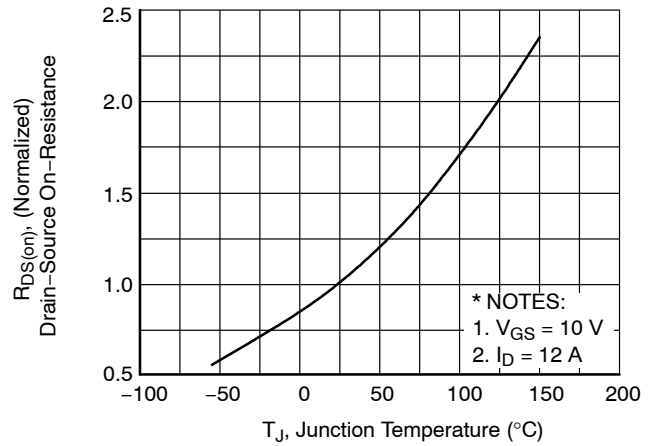
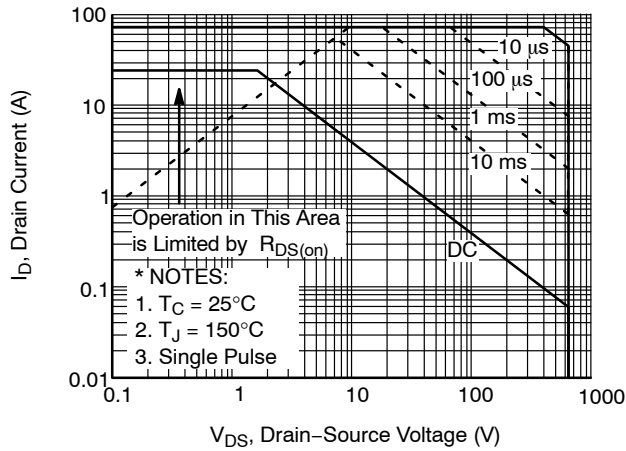Figure 7. Breakdown Voltage Variation
vs. Temperature

Figure 8. On−Resistance Variation
vs. Temperature

Figure 9. Maximum Safe Operating Area
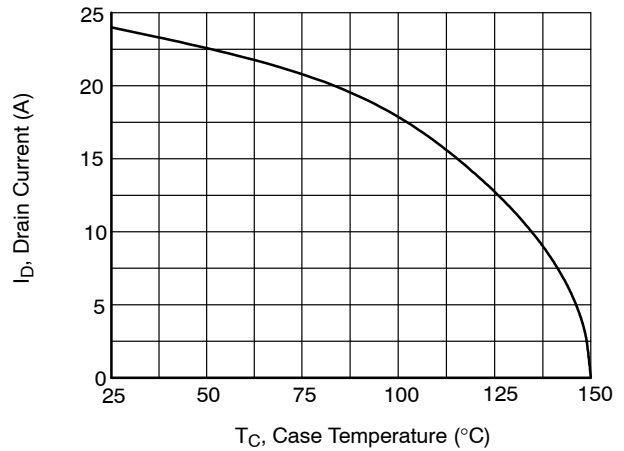
Figure 10. Maximum Drain Current
vs. Case Temperature
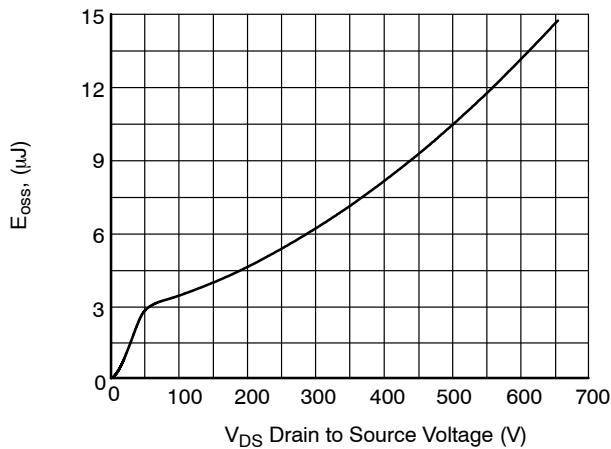
Figure 11. E$_{OSS}$ vs. Drain to Source Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (continued)
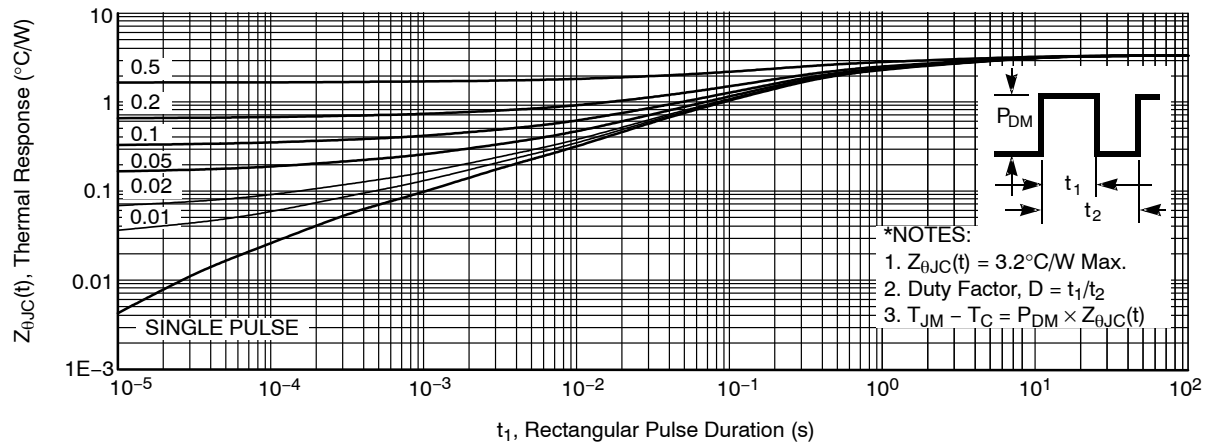
Figure 12. Transient Thermal Response Curve
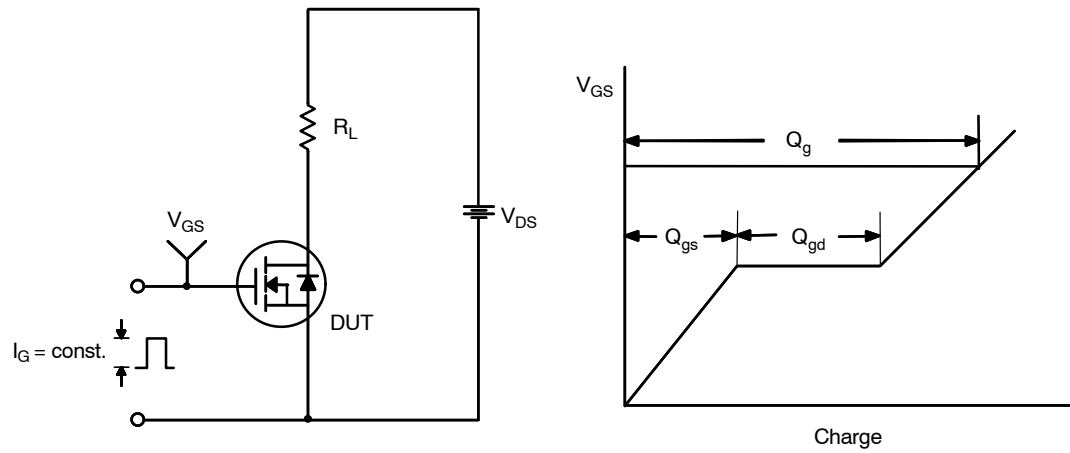
Figure 13. Gate Charge Test Circuit & Waveform
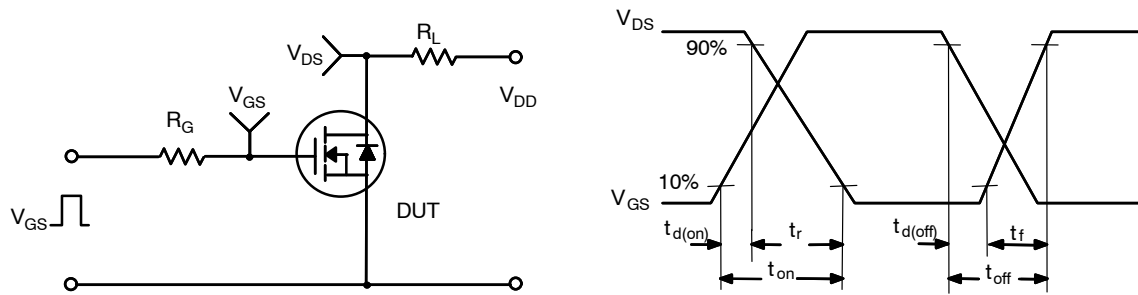
Figure 14. Resistive Switching Test Circuit & Waveforms

$$E_{AS} = \frac{1}{2} LI_{AS}^{2}$$
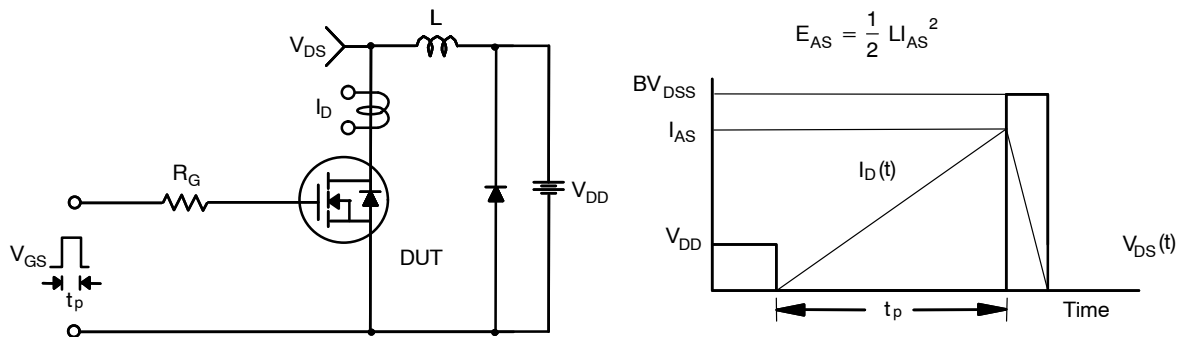
Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

The following labels appear in the figure:

DUT

V_{DS}

I_{SD}

L

Driver

R_G

Same Type as DUT

V_{DD}

V_{GS}

- dv/dt controlled by R_G
- I_{SD} controlled by pulse period

V_{GS} (Driver)

$D = \dfrac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$

10 V

I_{SD} (DUT)

I_{FM} , Body Diode Forward Current

di/dt

I_{RM}

Body Diode Reverse Current

V_{DS} (DUT)

Body Diode Recovery dv/dt

V_{SD}

V_{DD}

Body Diode Forward Voltage Drop
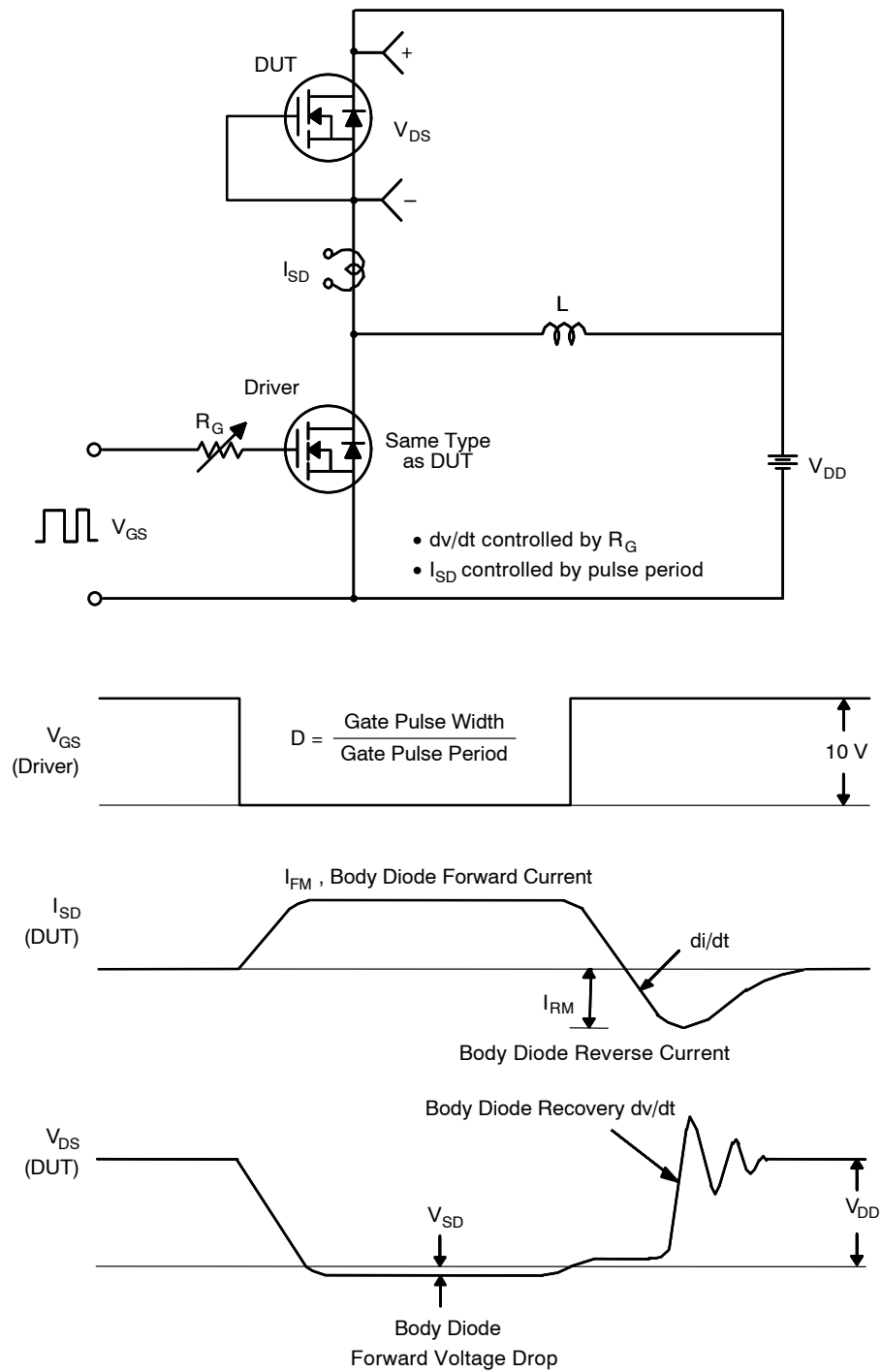
Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

TO−220 Fullpack, 3−Lead / TO−220F−3SG
CASE 221AT
ISSUE B

DATE 19 JAN 2021

Scale 1:1

DIM	MILLIMITERS		
	MIN	NOM	MAX
A	4.50	4.70	4.90
A1	2.56	2.76	2.96
A2	2.34	2.54	2.74
b	0.70	0.80	0.90
b2	~	~	1.47
c	0.45	0.50	0.60
D	15.67	15.87	16.07
D1	15.60	15.80	16.00
E	9.96	10.16	10.36
e	2.34	2.54	2.74
F	~	0.84	~
H1	6.48	6.68	6.88
L	12.78	12.98	13.18
L1	3.03	3.23	3.43
Ø P	2.98	3.18	3.38
Ø P1	~	1.00	~
Q	3.20	3.30	3.40

OPTION1

DETAIL-A

NOTES:
A. DIMENSION AND TOLERANCE AS ASME Y14.5-2009
B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUCSIONS.
C. OPTION 1 - WITH SUPPORT PIN HOLE
    OPTION 2 - NO SUPPORT PIN HOLE

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical–documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

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