MOSFET – Power, N-Channel, UltraFET

55 V, 75 A, 7 mΩ

FDH5500-F085

Features

- Typ $R_{DS(on)}$ = 5.2 mΩ at V_{GS} = 10 V, I_D = 75 A
- Typ $Q_{g(10)}$ = 118 nC at V_{GS} = 10 V
- Simulation Models
  –Temperature Compensated PSPICE™ and Saber® Models
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- AEC–Q101 Qualified and PPAP Capable
- This Device is Pb–Free and is RoHS Compliant

Applications

- DC Linear Mode Control
- Solenoid and Motor Control
- Switching Regulators
- Automotive Systems

ON Semiconductor®

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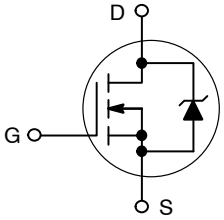
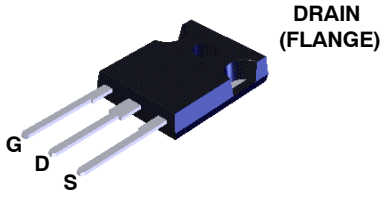
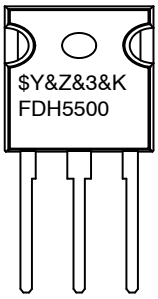
V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
55 V	7 mΩ	75 A





JEDEC TO–247
CASE 340CK

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot
FDH5500	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

MOSFET MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage (Note 1)		55	V
V_{DGR}	Gate to Gate Voltage (R_{GS} = 20 kΩ) (Note 1)		55	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Drain Current Continuous (T_C < 135°C, V_{GS} = 10 V)		75	A
	Pulsed		Figure 4	
E_{AS}	Single Pulse Avalanche Energy (Note 2)		864	mJ
P_D	Power Dissipation	(T_C = 25°C)	375	W
		− Derate Above 25°C	2.5	W/°C
T_J, T_{STG}	Operating and Storage Temperature		−55 to +175	°C
T_L	Max. Lead Temp. for Soldering (at 1.6 mm from case for 10 sec)		300	°C
T_{pkg}	Max. Package Temp. for Soldering (Package Body for 10 sec)		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Starting T_J = 25°C to 175°C.
2. Starting TJ = 25°C, L = 0.48 mH, I_{AS} = 60 A

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance Junction to Case	0.4	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO−247, 1in^2 copper pad area	30	°C/W

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDH5500	FDH5500−F085	TO−247	Tube	N/A	30 Units

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	55			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 50 V, V_{GS} = 0 V, V_{DS} = 45 V			1	μA
		V_{DS} = 50 V, V_{GS} = 0 V, V_{DS} = 45 V, T_C = 150°C			250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V			±100	nA
ON CHARACTERISTICS						
$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.0	2.9	4.0	V
$R_{DS(ON)}$	Drain to Source On Resistance	I_D = 75 A, V_{GS} = 10 V		5.2	7	mΩ
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz		3565		pF
C_{OSS}	Output Capacitance			1310		pF
C_{RSS}	Reverse Transfer Capacitance			395		pF
$Q_{g(TOT)}$	Total Gate Charge at 20 V	V_{GS} = 0 V to 20 V; V_{DD} = 30 V, I_D = 75 A, R_L = 0.4 Ω, I_g = 1.0 mA		206	268	nC
$Q_{g(10)}$	Total Gate Charge 10 V	V_{GS} = 0 V to 10 V; V_{DD} = 30 V, I_D = 75 A, R_L = 0.4 Ω, I_g = 1.0 mA		118	153	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0 V to 2 V; V_{DD} = 30 V, I_D = 75 A, R_L = 0.4 Ω, I_g = 1.0 mA		6.2	8.1	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 30 V, I_D = 75 A, R_L = 0.4 Ω, I_g = 1.0 mA		17.8		nC
Q_{gd}	Gate to Drain “Miller” Charge			51		nC
SWITCHING CHARACTERISTICS						
t_{on}	Turn-On Time	V_{DD} = 30 V, I_D = 75 A, R_L = 0.4 Ω, V_{GS} = 10 V, R_{GS} = 2.5 Ω			185	ns
$t_{d(on)}$	Turn-On Delay Time			13.7		ns
t_r	Rise Time			102		ns
$t_{d(off)}$	Turn-Off Delay Time			34		ns
t_f	Fall Time			22		ns
t_{off}	Turn-Off Time				91	ns
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 75 A		1	1.25	V
t_{rr}	Reverse Recovery Time	I_F = 75 A, dI_{SD}/dt = 100 A/μs		60	78	ns
Q_{rr}	Reverse Recovery Charge			77	100	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

(T_C = 25°C unless otherwise noted)

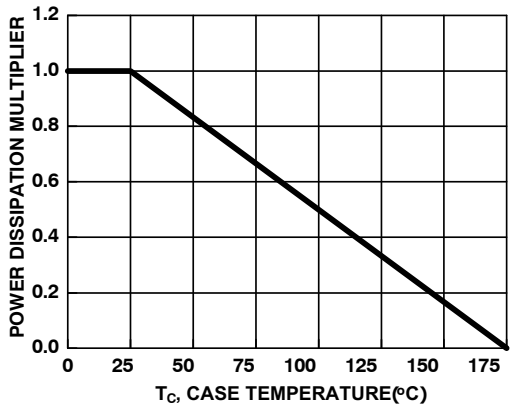


Figure 1. Normalized Power Dissipation vs. Case Temperature

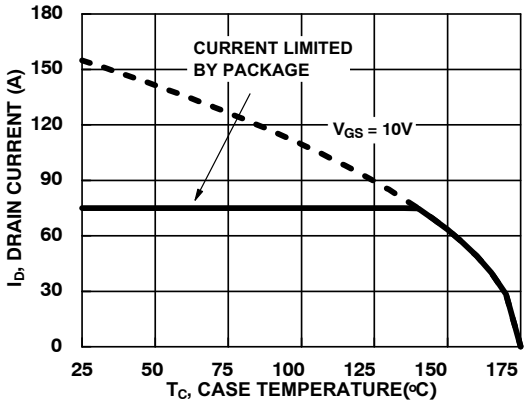


Figure 2. Maximum Continuous Drain Current vs Case Temperature

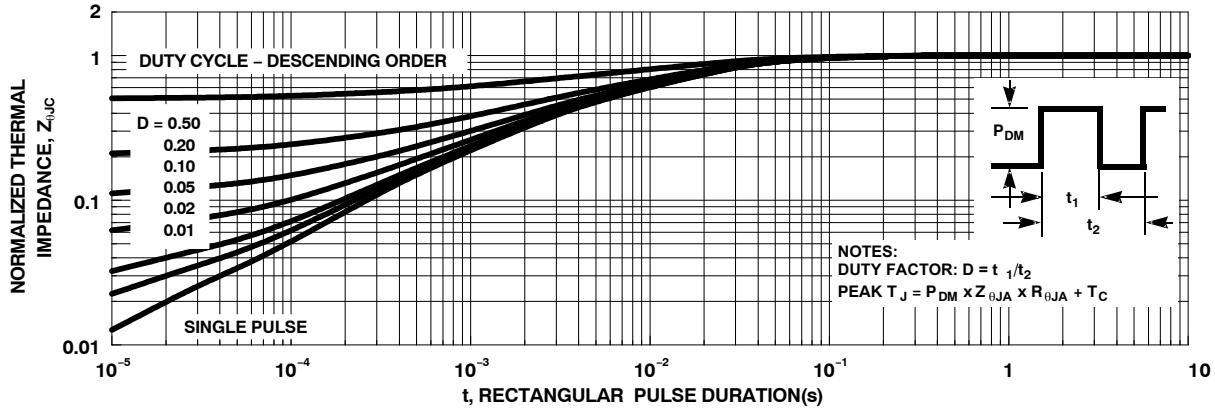


Figure 3. Normalized Maximum Transient Thermal Impedance

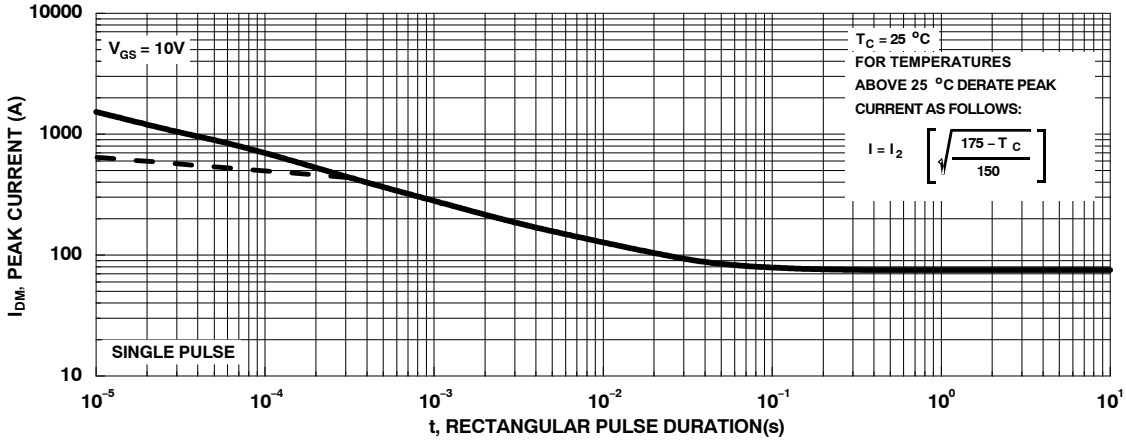


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (Continued)

(T_C = 25°C unless otherwise noted)

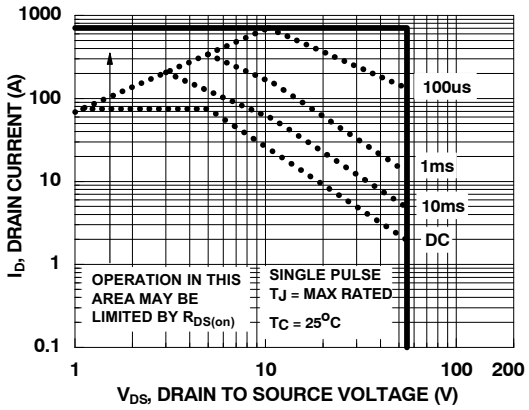


Figure 5. Forward Bias Safe Operating Area

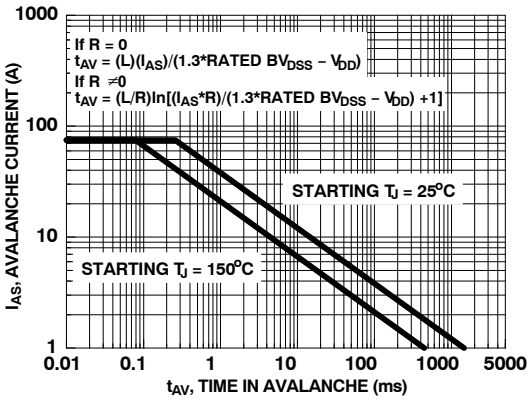


Figure 6. Unclamped Inductive Switching Capability

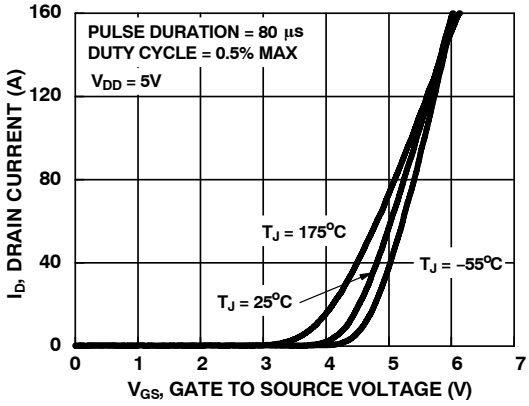


Figure 7. Transfer Characteristics

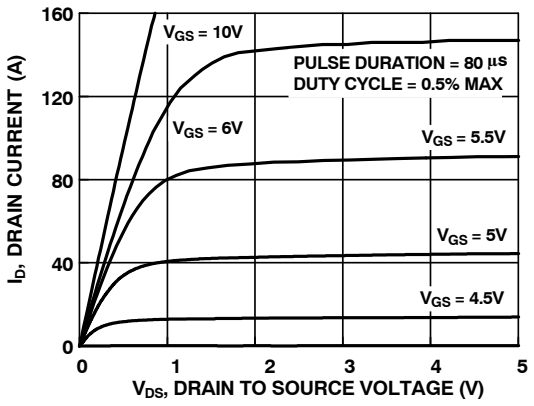


Figure 8. Saturation Characteristics

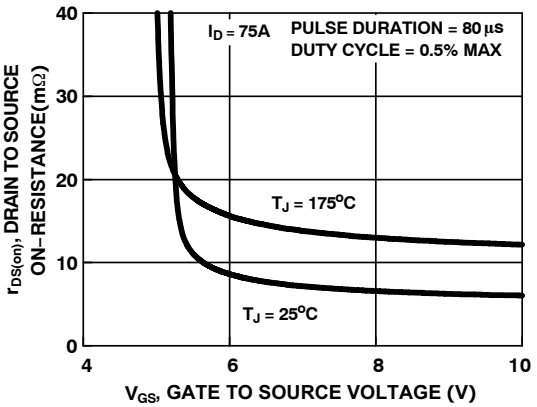


Figure 9. Drain to Source On Resistance Variation vs Gate to Source Voltage

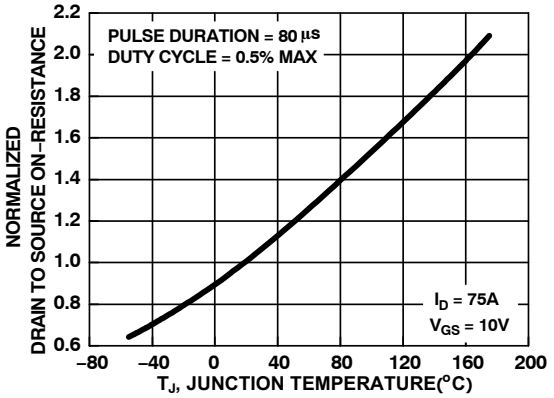
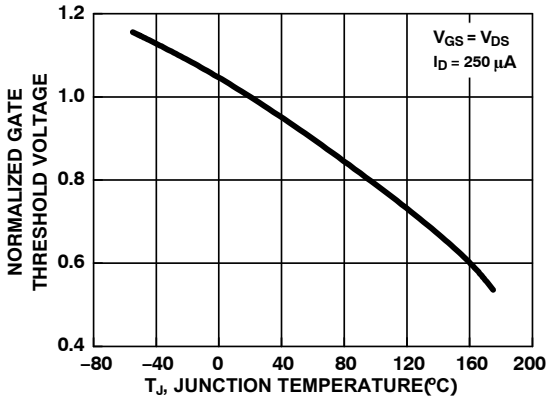


Figure 10. Normalized Drain to Source On Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS (Continued)

(T_C = 25°C unless otherwise noted)



μs

Figure 11. Normalized Gate Threshold Voltage vs. Junction Temperature

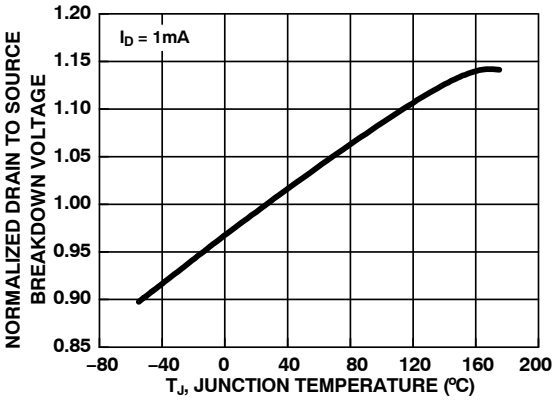


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

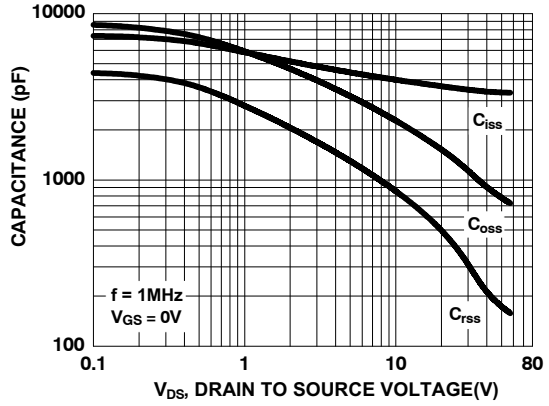


Figure 13. Capacitance vs. Drain to Source Voltage

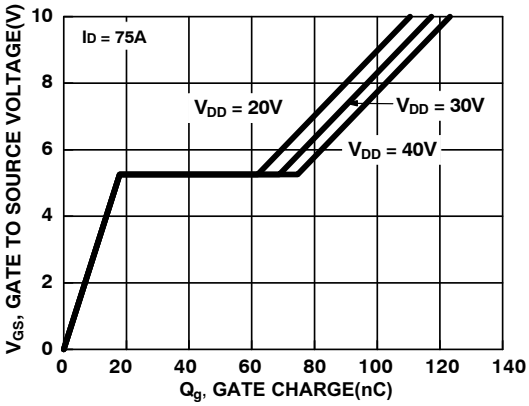


Figure 14. Gate Charge vs. Gate to Source Voltage

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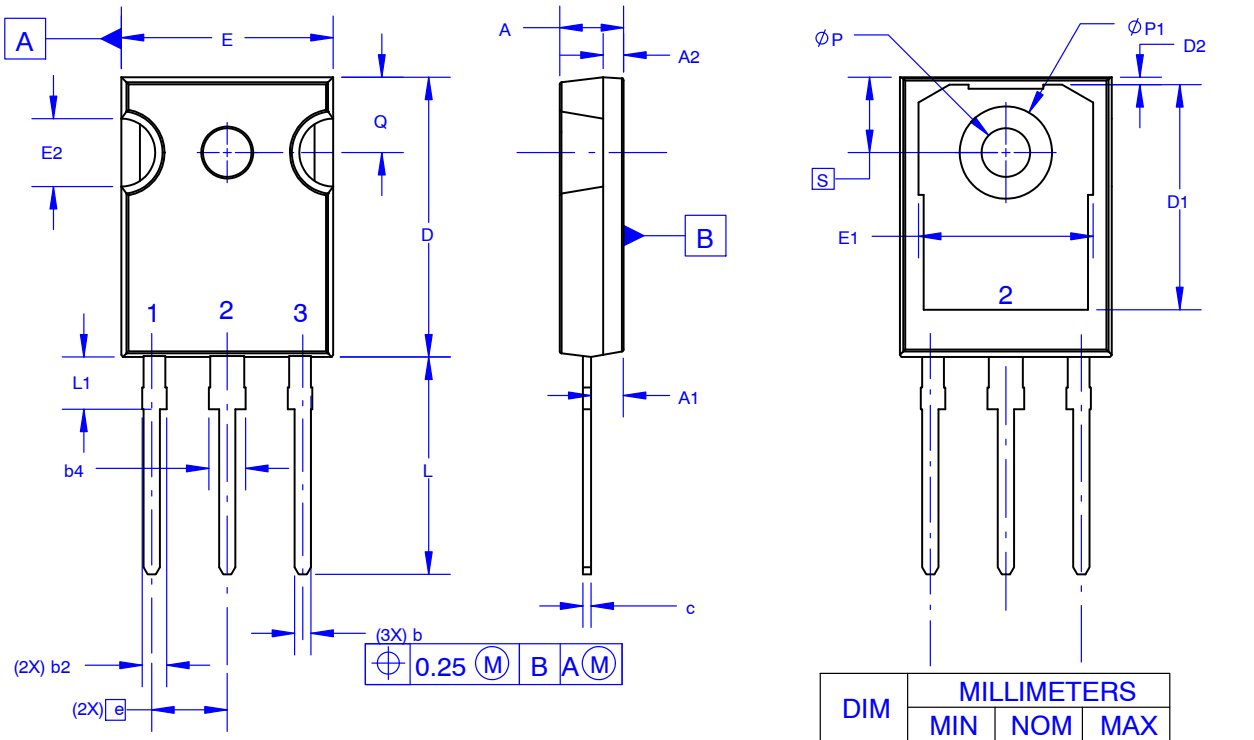
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

TO−247−3LD SHORT LEAD
CASE 340CK
ISSUE A

DATE 31 JAN 2019

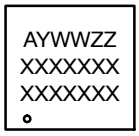


DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D	20.32	20.57	20.82
D1	13.08	~	~
D2	0.51	0.93	1.35
E	15.37	15.62	15.87
E1	12.81	~	~
E2	4.96	5.08	5.20
e	~	5.56	~
L	15.75	16.00	16.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
ØP1	6.60	6.80	7.00
Q	5.34	5.46	5.58
S	5.34	5.46	5.58

NOTES: UNLESS OTHERWISE SPECIFIED.

A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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