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FAIRCHILD SEMICONDUCTOR®

November 2009

# FSA110 — 具有负信号处理能力及内置下拉电阻的音频和高速 (480Mbps) USB 信号线与开关

## 特性

- 对于高速USB具有6pF典型开关断开电容
- 对于音频信号具有2.5Ω典型导通电阻
- 音频通道具有负电压信号处理能力
- 可自动检测USB
- 在D+/R, D-/L 端口有断电保护
- 流通引脚无需PCB过孔
- 在非选择通道上内置下拉电阻有效去除音频噪音

## 应用

- 手机, PDA, 数字相机和笔记本
- LCD显示屏, TV, 和机顶盒

## 概述

FSA110是双刀单掷开关，在USB应用中它兼有一条低音频失真路径和低断开电容特征。这种结构对于在单一连接器上共享USB2.0 高速信号和音频信号的线与电路是理想的选择。内部优化的结构设计允许音频输入低于地电平这样在媒体播放器或便携产品设计中USB接口可以被音频输出和USB信号复用。

FSA110被配置成默认的USB状态，用户可以根据音频设计需要来控制开关的闭合，音频通道默认关闭并可以通过控制/OE管脚来实现音频通道的激活。 FSA110内部有断电保护功能，适用于当供电电源在0V时有效隔离外部信号。

## 重要注解：

欲知其它详情，请联系analogswitch@fairchildsemi.com.

## 订货信息

| 订货号码 | 表面标记 | Eco Status | 封装描述 |
|---|---|---|---|
| FSA110K8X | A110 | Green | 8-引脚 US8, JEDEC MO-187, Variation CA, 3.0mm宽的封装 |
| FSA110UMX | GZ | Green | 10-引脚，方型, 超薄模塑无脚封装, 1.4 x 1.8mm |

*For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html*

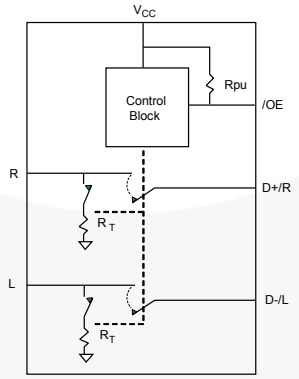



**图1：模拟表达符号**

## 管脚分配图

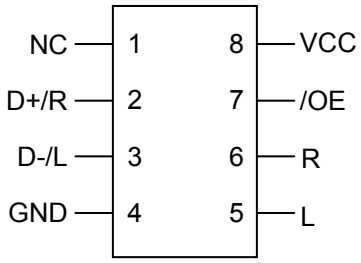



**图2：8管脚的US8**

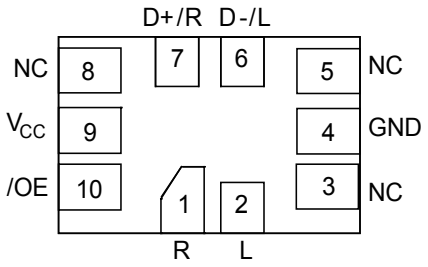



**图3：10管脚的UMLP**

## 管脚描述

| 名称 | 描述 |
|---|---|
| $V_{CC}$ | 供电电源. |
| /OE | 输出使能，管脚默认为高平，在上电时允许使用者关闭音频通道，音频通道仅在/OE被低平驱动时才连通，开关默认为USB 模式. |
| R, L | 音频左，右输入源. |
| D+/R, D-/L | USB和音频共同连接端. |

## 真值表

| $V_{CC}$ /O | E(1) | 音频模式 USB | 模式 |
|---|---|---|---|
| 低平 | | 断开 | 导通 |
| 高平 | 低平 | 导通 | 断开 |
| - | 高平 | 断开 | 导通 |

**注解**:

1．具有内部上拉电阻至 $V_{CC}$ 的/OE提供了一个默认的USB状态， /OE 必须被低电平驱动时才能导通音频路径。

## 功能描述

FSA110兼有USB和音频的开关，它能够让USB连接器和立体声音频CODEC的输出共享D+/D-线。/OE管脚有内部的上拉电阻，这种电阻起于默认的USB模式结构。这种结构在系统上电时给音频通道提供了内置的静音和不管是否有$V_{CC}$供电默认的USB模式能够允许系统传送USB 数据。当USB开关被连接时这种结构还允许使用者优先USB默认状态和在USB路径上输送模拟音频。在这种结构中不再需要自动的USB检测器。音频开关通道能够处理负电压信号，消除了对大的耦合电容的需要和大大地减小了潜在的爆破音。在开关处在USB模式时音频R, L端口的终端电阻被启动，这样能够减小在音频路径上的爆破音。

## 应用框图

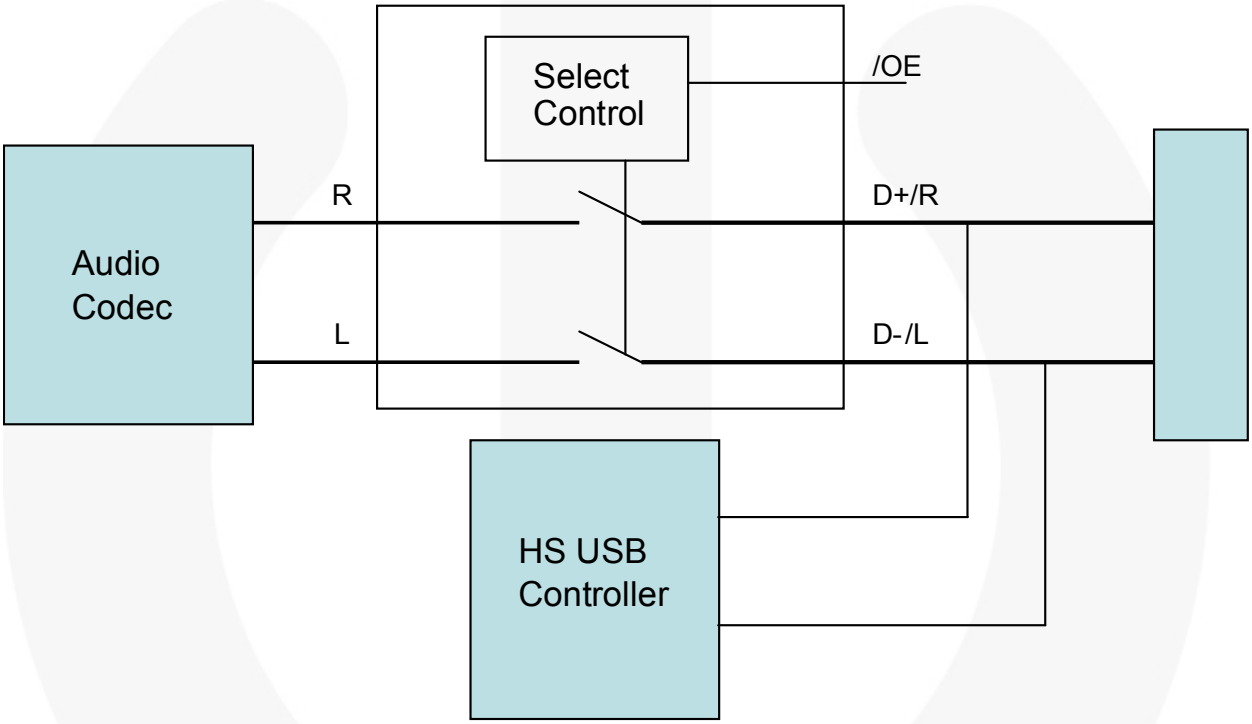



**图4. 典型的应用框图**

## 最大绝对额定值

超出绝对最大额定值会破坏设备，设备会不工作或者说不建议设备在和超过建议的工作条件下被操作。另外，过长的暴露在超过建议工作条件下会影响设备的可靠性， 这种最大绝对额定值仅仅是极端额定值。

| 表达符号 | 参数 | | 最小 | 最大 | 单位 |
|---|---|---|---|---|---|
| $V_{CC}$ | 供电电压 | | -0.5 | 4.6 | V |
| /OE | 输出使能控制信号 | | -0.5 | 4.6 | V |
| $V_{SW}$ | 开关 I/O电压(2) | USB 路径 | -1.0 | 4.6 | V |
| | | 音频路径 | $V_{CC}$–4.6 | 4.6 | V |
| $I_{IK}$ | 输入钳位二极管电流 | | | - 50 | mA |
| $I_{SW}$ | 开关 I/O 电流(续) | 音频 | | 100 | mA |
| $I_{SWPEAK}$ | 峰值开关电流(脉冲持续时间, <10% 占空系数) | 音频 | | 150 | mA |
| $T_{STG}$ | 保存温度范围 | | -65 | +150 | °C |
| $T_J$ | 最高结点温度 | | | +150 | °C |
| $T_L$ | 导线温度(焊接, 10秒) | | | +260 | °C |
| ESD | 人体电流模式(JEDEC: JESD22-A114) | I/O 至地 | 12 | | kV |
| | | 所有管脚 | 2 | | |
| | | $V_{CC}$至地 | 12 | | |
| | 充放电模式 (JEDEC-JESD-C101) | | 2 | | |

**注解**:

**2.** 如输入及输出二极管电流额定值均达到时则可能会超出输入及输出负额定值。

## 推荐工作条件

推荐工作条件表中定义的是实际元件工作的条件。推荐工作条件指定用于保证实现数据表规范的最佳性能， Fairchild 建议不得超出以上值或设计至最大绝对额定值。

| 表达符号 | 参数 | | 最小 | 最大 | 单位 |
|---|---|---|---|---|---|
| $V_{CC}$ | 供电电压 | | 2.7 | 4.3 | V |
| /OE | 输出使能控制信号 | | 3.0 | 4.3 | V |
| $V_{SW}$ | 开关输入/输出电压 | USB路径使能 | 0 | 4.3 | V |
| | | 音频路径使能 | $V_{CC}$ -4.3 | 4.3 | V |
| $T_A$ | 操作温度 | | -40 | +85 | °C |

## DC电气特性

如未另外说明均为25ºC下的标准值

| 表达符号 | 参数 | $V_{CC}$ (V) | 条件 | $T_A$ = -40 至 +85°C | | | 单位 |
|---|---|---|---|---|---|---|---|
| | | | | 最小 | 典型(6) | 最大 | |
| **共同管脚** | | | | | | | |
| $V_{IK}$ | 钳位二极管电压 | 3.0 | $I_{IK}$ = -18mA | | | -1.2 | V |
| $V_{IH}$ | 控制输入电压高电平 | 2.7 至 4.3 | | 1.7 | | | |
| $V_{IL}$ | 控制输入电压低电平 | 2.7 至 4.3 | | | | 0.6 | |
| | | | $V_{IN}$ = 4.3V | 1 | | -1 | |
| $I_{OFF}$ | 断开漏电流 (共同端口仅为D+/R, D-/L) | 0 | 共同端(D+/R, D-/L)<br>$V_{SW}$ = 4.3V或悬浮 | -10 | | 10 | µA |
| $I_{NC(ON)}$ | D+/R 或 D-/L端口导通漏电流 | 4.3 | D+/R, D-/L = 0.3V,<br>4.0V D+, D-, R, L =悬浮<br>Figure 10 | -250 | 1 | 250 | nA |
| $R_{Pu}$ | /OE端内部上拉电阻 | 4.3 | | | 3 | | MΩ |
| $R_T$ | 音频路径终端电阻 | 4.3 | $V_{IN}$=0.3V 或 4.0V | | 100 | | Ω |
| **音频开关路径** | | | | | | | |
| $V_{Audio}$ | 音频模拟信号范围 | 2.7 至 4.3 | | $V_{CC}$-4.3V | | $V_{CC}$ | V |
| $R_{ONAudio}$ | 音频开关导通电阻(3) | 2.7 | $V_{L/R}$ = -1.5V, 0V,1.5V<br>$I_{ON}$ = 60mA | | 1.5 | 3.0 | Ω |
| $\Delta R_{ONAudio}$ | 音频$\Delta R_{ON}$(4) | 2.7 | $V_{L/R}$ = 0.7V $I_{ON}$ = 60mA | | 0.4 | | Ω |
| $R_{FLAT(Audio)}$ | 音频$R_{ON}$平坦度(5) | 2.7 | $V_{SW}$=-1.5V 至1.5V $I_{ON}$ = 60mA | | 0.4 | 0.8 | Ω |
| **供电电源** | | | | | | | |
| $I_{CC}$ | 静态工作电流 | 4.3 | /OE = 低平或$V_{CC}$, $I_{OUT}$ = 0 | | 1.5 | 15.0 | µA |

**注解：**

3. 导通电阻由开关指定电流下A、B管脚之间的电压降决定。

4. $\Delta R_{ON}=R_{ON\,max} - R_{ON\,min}$在相同$V_{CC}$、温度及电压下测得， 最差条件下的信号路径－音频或USB通道均被表征。

5. 平坦度定义为各种条件指定范围内ON电阻最大值与最小值之间的差值。

6. 由特性保证而非产品试验。

## AC电气特性

如未另外说明均为25ºC下的标准值.

| 表达符号 | 参数 | $V_{CC}$ (V) | 条件 | $T_A$ = - 40 to +85°C | | | 单位 |
|---|---|---|---|---|---|---|---|
| | | | | 最小 | 典型.(7) | 最大 | |
| $t_{ON}$ | 开启时间, /OE至输出 | 2.7 至 4.3 | $V_{D+/R, D-/L}$ = 1.0V<br>$R_L$ = 50Ω, $C_L$ = 50Pf<br>Figures 11, 12, 13 | | 2 | | µs |
| $t_{OFF}$ | 关闭时间, /OE至输出 | 2.7 至 4.3 | $V_{D+/R, D-/L}$ = 1.0V<br>$R_L$ = 50Ω, $C_L$ = 50pF<br>Figures 11, 12, 13 | | 2 | | µs |
| Xtalk | 非相邻通道串扰 (音频模式) | 3.3 至 4.3 | f = 20kHz, $R_T$ = 32Ω,<br>$C_L$ = 0pF<br>Figure 18 | | -75 | | dB |
| THD | 总谐波失真 (音频模式) | 3.0 至 4.3 | f = 20Hz to 20 kHz<br>$R_L$ = 32Ω, $V_{IN}$ = $2V_{pp}$<br>Figure 16 | | 0.05 | | % |
| SNR | 信号噪声比 (音频模式) | 3.3 至 4.3 | f = 20kHz to 20kHz,<br>$R_L$ = 32Ω, $V_{IN}$ = $2V_{PP}$<br>Figure 16 | | 80 | | dB |

**注解**:
7．由特性保证而非产品试验。

## 电容

如未另外说明均为25ºC下的标准值

| 表达符号 | 参数 | $V_{CC}$ (V) | 条件 | $T_A$ = - 40 至 +85°C | | | 单位 |
|---|---|---|---|---|---|---|---|
| | | | | 最小 | 典型(8) | 最大 | |
| $C_{IN}$ | 控制端输入电容 | 3.0 至 4.3 | $V_{BIAS}$ = 0.2V | | 2.5 | | pF |
| $C_{OFF}$ | 开关断开电容 | 3.0 至 4.3 | f = 240MHz<br>Figure 14 | | 6.0 | | pF |

**注解**:
8．由特性保证而非产品试验。

## 典型特性

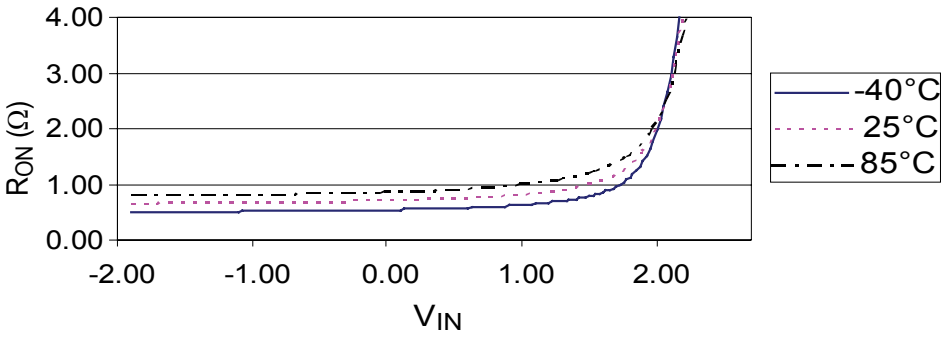



图5.$R_{ON}$ 音频, $V_{CC}$=2.7V

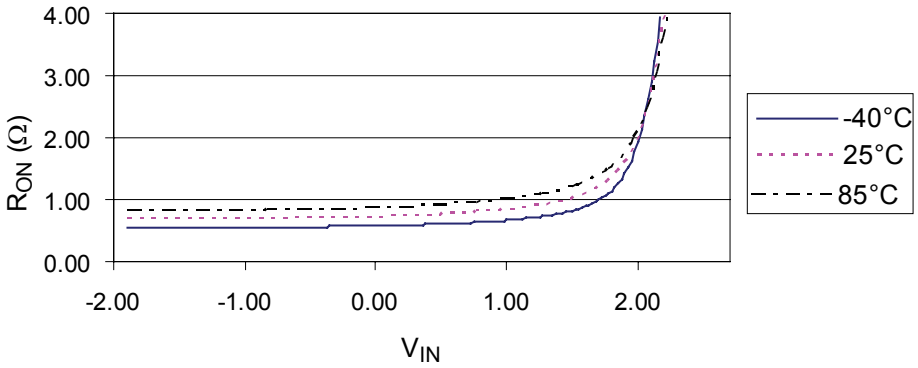



图6.$R_{ON}$ 音频, $V_{CC}$=2.7V

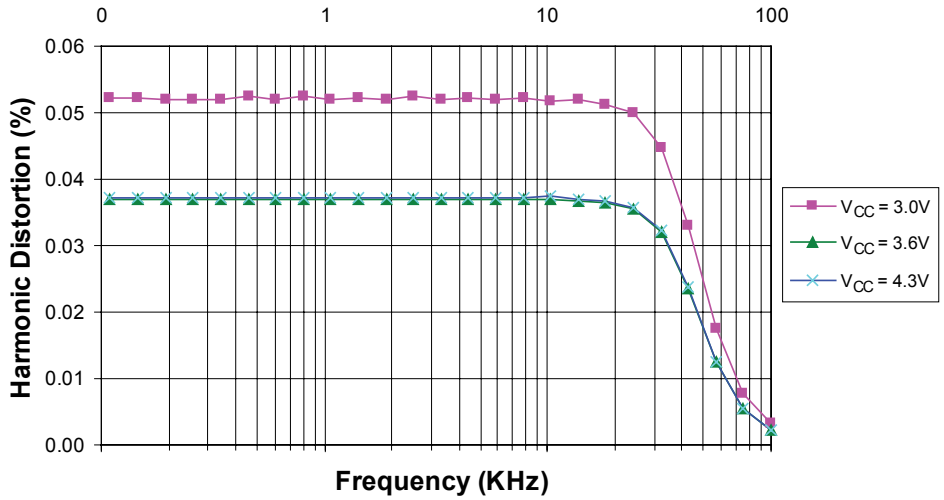



图7.总谐波失真

## 测试图

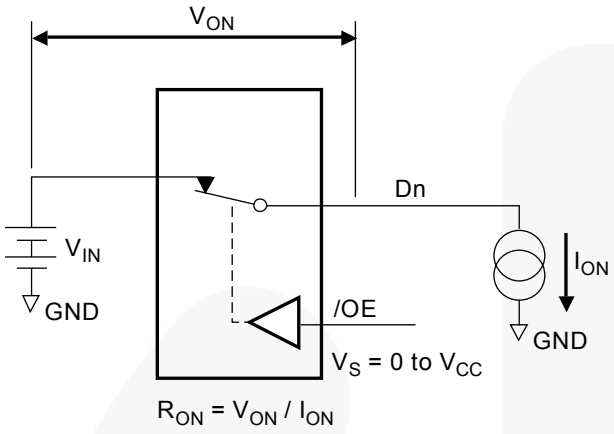



图8.导通电阻

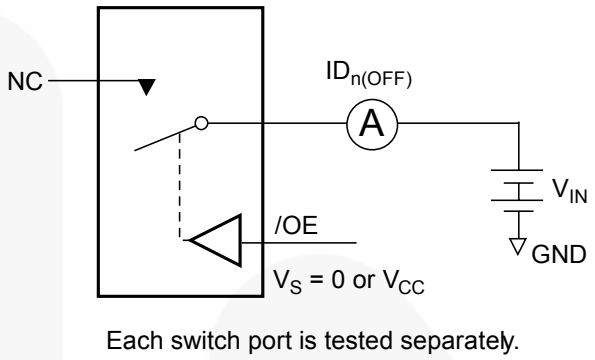



图9.断开漏电流

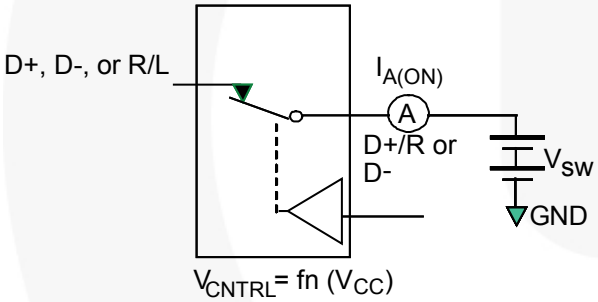



图10. 导通漏电流

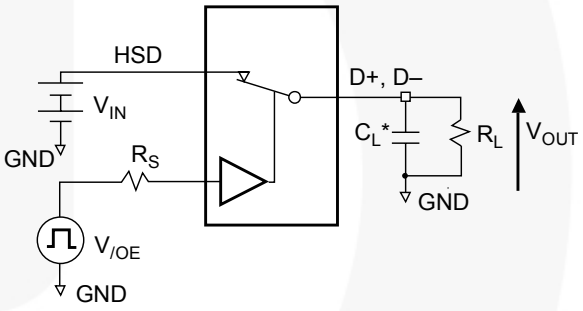



图11.AC测试电路负载

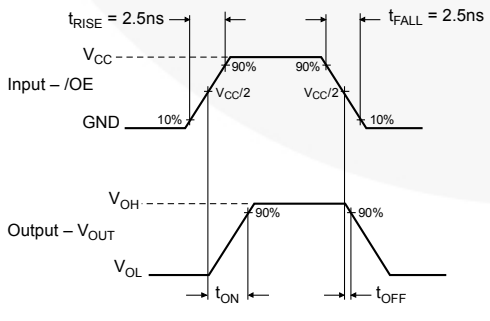



图12.开启/ 关闭波形

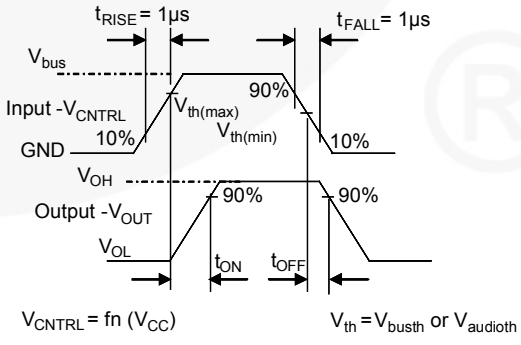



图13.开启/ 关闭波形

## 测试图(续)

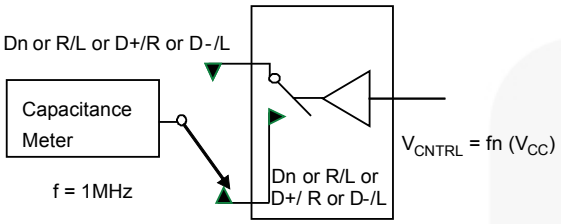



图14.通道断开电容

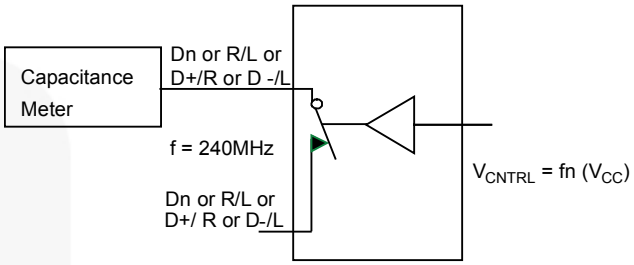



图15.通道导通电容

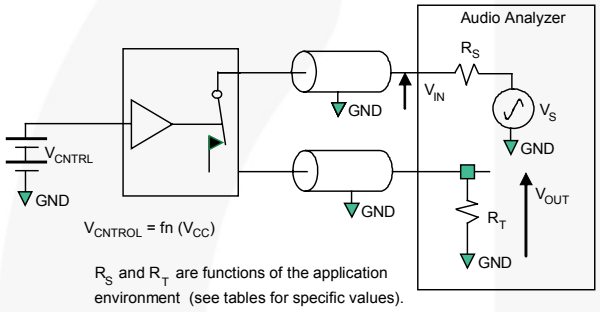



图16.总谐波失真

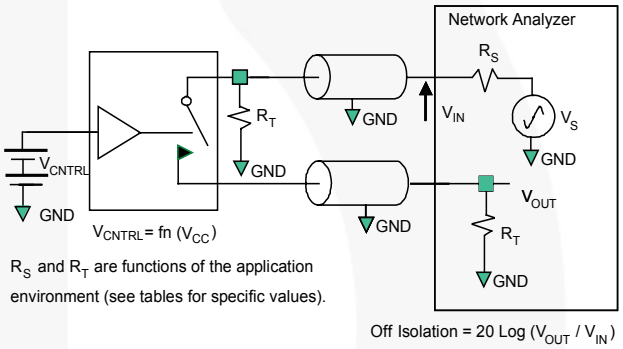



图17.通道隔离度

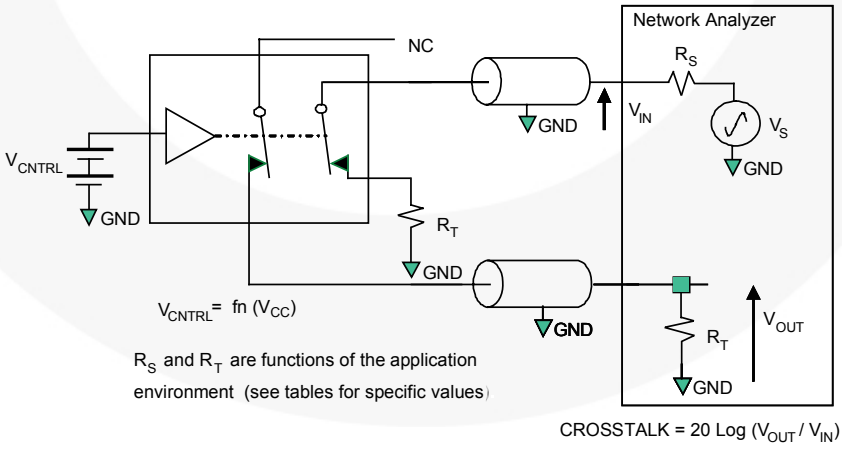
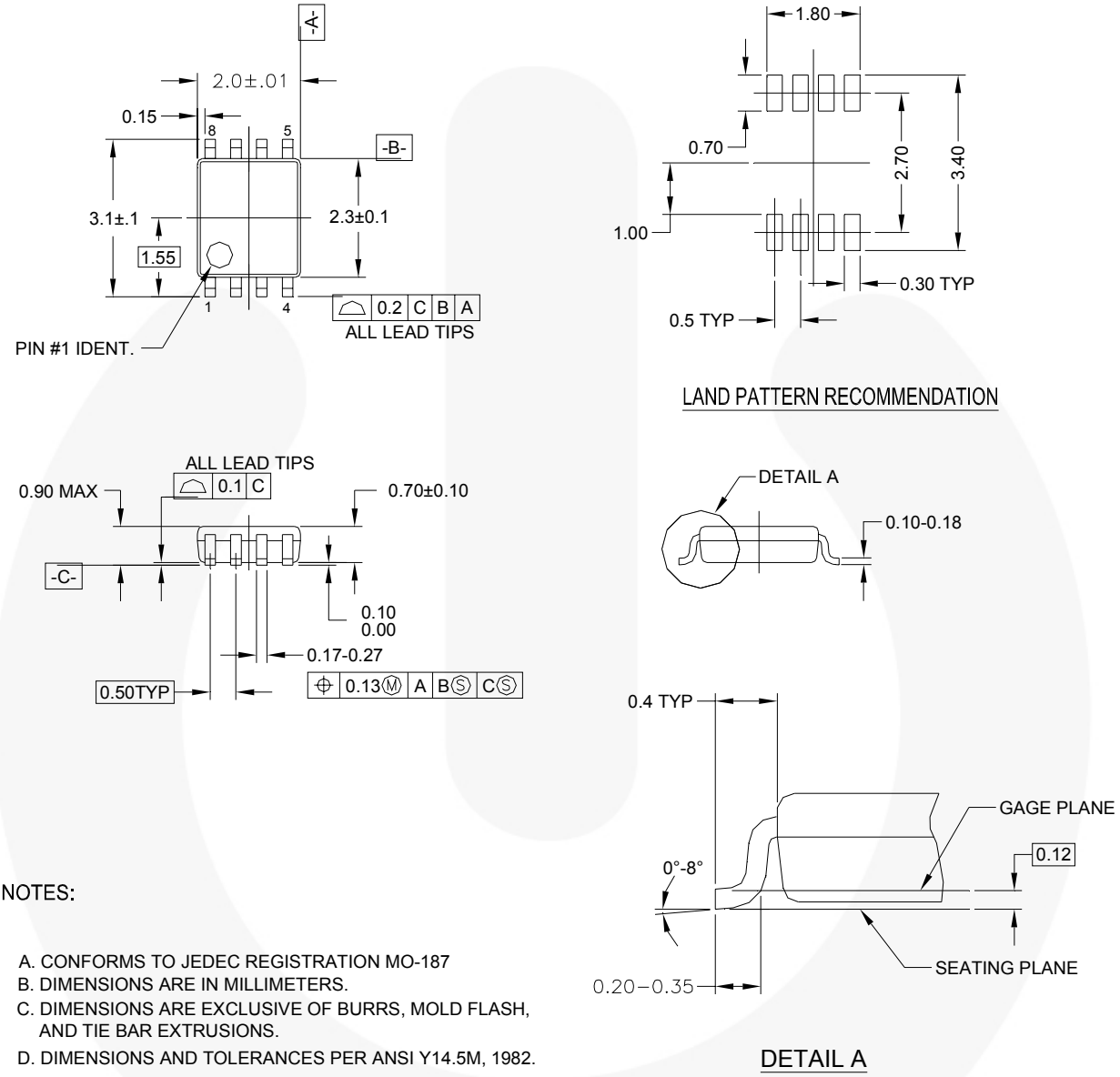



图18.非相邻通道之间的串扰

## 物理尺寸




NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-187
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MAB08AREVC

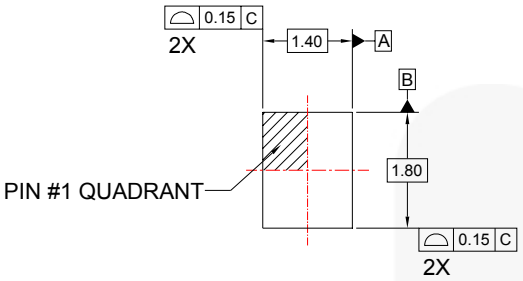
**图19. 8-引脚 US8, JEDEC MO-187, Variation CA, 3.0mm宽的封装**

*Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.*

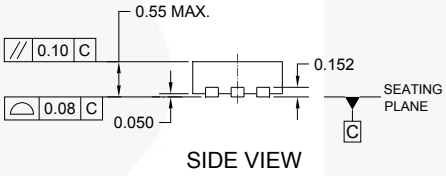
*Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:*

*http://www.fairchildsemi.com/packaging/.*

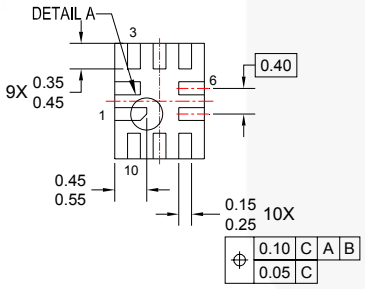
## 物理尺寸



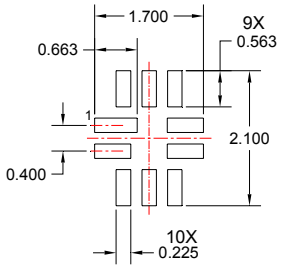

TOP VIEW



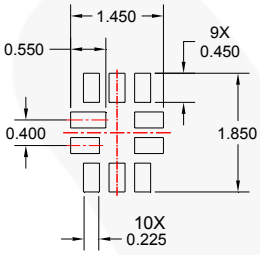

SIDE VIEW



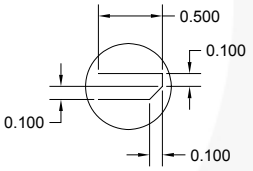

BOTTOM VIEW




RECOMMENDED LAND PATTERN




OPTIONAL MINIMIAL TOE LAND PATTERN




DETAIL A
PIN #1 TERMINAL
SCALE: 2X

NOTES:

A. DIMENSIONS ARE IN MILLIMETERS.

B. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

C. DRAWING FILENAME: UMLP10Arev2

**图20。10引脚的方型, 超薄模塑无脚封装(MLP)**

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