Green Mode Power Switch

FSL137H

Description

The highly integrated FSL137H consists of an integrated current mode Pulse Width Modulator (PWM) and an avalanche-rugged 700 V SENSEFET[®]. It is specifically designed for high-performance offline Switch Mode Power Supplies (SMPS) with minimal external components.

The integrated PWM controller features include a proprietary green-mode function that provides off-time modulation to linearly decrease the switching frequency at light-load conditions to minimize standby power consumption. To avoid acoustic noise problems, the minimum PWM frequency is set above 18 kHz. The green-mode function enables the power supply to meet international power conservation requirements. With the internal high-voltage startup circuitry, the power loss due to bleeding resistors is also eliminated. To further reduce power consumption, the PWM controller is manufactured using the BiCMOS process, which allows an operating current of only 3.5 mA.

The FSL137H built–in synchronized slope compensation achieves stable peak–current–mode control. The proprietary external line compensation ensures constant output power limit over a wide AC input voltage range, from 90 V_{AC} to 264 V_{AC} .

The FSL137H provides many protection functions. In addition to cycle–by–cycle current limiting, the internal open–loop protection circuit ensures safety when an open–loop or output short–circuit failure occurs. PWM output is disabled until V_{DD} drops below the UVLO lower limit, when the controller starts up again. As long as V_{DD} exceeds ~28 V, the internal OVP circuit is triggered.

Compared to a discrete MOSFET and controller or RCC switching converter solution, the FSL137H reduces total component count, design size, and weight while increasing efficiency, productivity, and system reliability. These devices provide a basic platform well suited for design of cost-effective flyback converters.

Features

- Built-in 5 ms Soft-Start Function
- Internal Avalanche Rugged 700 V SENSEFET
- Low Audio Noise
- High-Voltage Startup
- Fixed PWM Frequency at 100 kHz
- Linearly Decreasing PWM Frequency to 18 kHz
- Peak-Current-Mode Control
- Cycle-by-Cycle Current Limiting
- Leading–Edge Blanking (LEB)
- Synchronized Slope Compensation
- Internal Open-loop Protection (OLP)
- V_{DD} Under-Voltage Lockout (UVLO)
- V_{DD} Over–Voltage Protection (OVP)
- Constant Power Limit (Full AC Input Range)
- Internal OTP Sensor with Hysteresis



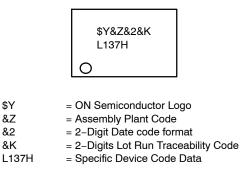
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MARKING DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Applications

General-purpose switch-mode power supplies and flyback power converters, including:

- SMPS for VCR, STB, DVD & VCD Player, Printer, Facsimile, & Scaner
- Adapter for Camcorder

Table 1. ORDERING INFORMATION

Part Number	Operating Temperature Range	SENSEFET	Package	Packing Method
FSL137HNY	–40°C to 105°C	3.0 A 700 V	8-Lead, Dual In-line Package (DIP)	Tube

APPLICATION DIAGRAM

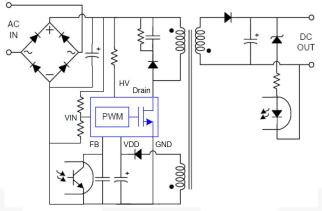


Figure 1. Typical Flyback Application

Table 2. OUTPUT POWER TABLE (Note 1)

	230 V _{AC} ± 15% (Note 2)		85–265 V _{AC}	
Product	Adapter (Note 3)	Open Frame (Note 4)	Adapter (Note 3)	Open Frame (Note 4)
FSL137H	17.5 W	25 W	13 W	19 W

1. The maximum output power can be limited by junction temperature.

2. 230 V_{AC} or 100/115 V_{AC} with doublers.

3. Typical continuous power in a non-ventilated enclosed adapter with sufficient drain pattern as a heat sink, at $T_A = 50^{\circ}C$ ambient. 4. Maximum practical continuous power in an open-frame design with sufficient drain pattern as a heat sink, at $T_A = 50^{\circ}C$ ambient.

INTERNAL BLOCK DIAGRAM

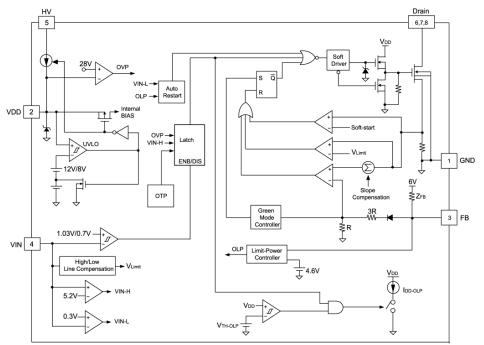


Figure 2. Internal Block Diagram

PIN CONFIGURATION

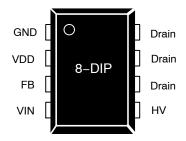


Figure 3. Pin Configuration

Table 3. PIN DEFINITIONS

Pin No.	Name	Description				
1	GND	Ground. SENSEFET source terminal on primary side and internal controller ground.				
2	VDD	wer Supply. The internal protection circuit disables PWM output as long as V _{DD} exceeds the OVP trigger point.				
3	FB	Feedback . The signal from the external compensation circuit is fed into this pin. The PWM duty cycle is determined in response to the signal on this pin and the internal current-sense signal.				
4	VIN	Line-Voltage Detection. The line-voltage detection is used for brownout protection with hysteresis and constant output power limit over universal AC input range. This pin has additional protections that are pull-HIGH latch and pull-low auto recovery, depending on the application.				
5	HV	Startup. For startup, this pin is pulled HIGH to the line input or bulk capacitor via resistors.				
6, 7, 8	Drain	SENSEFET Drain. High-voltage power SENSEFET drain connection.				

Table 4. ABSOLUTE MAXIMUM RATINGS

Symbol	Paramete	er	Min	Max	Unit
V _{DRAIN}	Drain Pin Voltage (Note 5, 6)			700	V
I _{DM}	Drain Current Pulsed (Note 7)			12	А
E _{AS}	Single Pulsed Avalanche Energy (Note 8)			230	mJ
V _{VDD}	DC Supply Voltage			30	V
V _{FB}	FB Pin Input Voltage		-0.3	7.0	V
V _{VIN}	VIN Pin Input Voltage		-0.3	7.0	V
V _{HV}	HV Pin Input Voltage			700	V
PD	Power Dissipation ($T_A < 50^{\circ}C$)			1.5	W
θ_{JA}	Junction-to-Air Thermal Resistance			80	°C/W
Ψ_{JT}	Junction-to-Top Thermal Resistance (Note 9)			35	°C/W
TJ	Operating Junction Temperature			+150	°C
T _{STG}	Storage Temperature Range		-55	150	°C
ΤL	Lead Temperature (Wave Soldering or IR, 10 Seconds)			+260	°C
ESD	Electrostatic Discharge Capability,	Human Body Model: JESD22-A114		4.5	kV
	All Pins Except HV Pin (Note 10)	Charged Device Model: JESD22-C101		1.5	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

All voltage values, except differential voltages, are given with respect to the network ground terminal.
 Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

7. Non-repetitive rating: Pulse width is limited by maximum junction temperature. 8. L = 51 mH, starting $T_J = 25^{\circ}C$. 9. Measured on the package top surface. 10. All pins including HV pin: HBM = 1 kV, CDM = 1.25 kV

Table 5. RECOMMENDED OPERATING CONDITIONS

Symbol Parameter		Min	Max	Unit	
T _A	Operating Ambient Temperature	-40	+105	°C	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 6. ELECTRICAL CHARACTERISTICS (V_{DD} = 15 V, T_A = 25° C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Тур	Max	Unit
SENSEFET	SECTION (Note 11)			•		
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V	700			V
I _{DSS}	Zero-Gate-Voltage Drain Current	V _{DS} = 700 V, V _{GS} = 0 V		0.5	50.0	μA
		V_{DS} = 560 V, V_{GS} = 0 V, T_{A} = 125°C		1	200	
R _{DS(ON)}	Drain-Source On-State Resistance (Note 12)	V _{GS} = 10 V, I _D = 0.5 A		4.00	4.75	Ω
C _{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 25 V, f = 1MHz		315	410	pF
C _{OSS}	Output Capacitance	V_{GS} = 0 V, V_{DS} = 25 V, f = 1MHz		47	61	pF
C _{RSS}	Reverse Transfer Capacitance	V_{GS} = 0 V, V_{DS} = 25 V, f = 1MHz		9	14	pF
t _{d(on)}	Turn-on Delay Time	V _{DS} = 350 V, I _D = 1.0 A		11.2	33.0	ns
t _r	Rise Time	V _{DS} = 350 V, I _D = 1.0 A		34	78	ns
t _{d(off)}	Turn-off Delay Time	V _{DS} = 350 V, I _D = 1.0 A		28.2	67.0	ns
t _f	Fall Time	V _{DS} = 350 V, I _D = 1.0 A		32	74	ns
V _{DD} SECTIO	N	· ·				
V _{OP}	Continuously Operating Voltage				22	V
V _{DD-ON}	Start Threshold Voltage		11	12	13	V
V _{DD-OFF}	Minimum Operating Voltage		7	8	9	V
I _{DD-ST}	Startup Current	V _{DD-ON} – 0.16 V			30	μA
I _{DD-OP}	Operating Supply Current	V _{DD} = 15 V, V _{FB} = 3 V	3.0	3.5	4.0	mA
I _{DD-BM}	Green-Mode Operating Supply Current	$V_{FB} = V_{FB-G}$		2		mA
I _{DD-OLP}	Internal Sink Current	V _{TH-OLP} + 0.1 V	30	60	90	μA
V _{TH-OLP}	I _{DD-OLP} Off Voltage		5	6	7	V
V _{DD-OVP}	V _{DD} Over-Voltage Protection		27	28	29	V
t _{D-VDDOVP}	V _{DD} Over-Voltage Protection Debounce Time		75	130	200	μs
HV SECTION	· N	•	•			
I _{HV}	Maximum Current Drawn from HV Pin	HV 120 V_{DC} , V_{DD} = 0 V with 10 μ F	1.5	3.5	5.0	mA
I _{HV-LC}	Leakage Current After Startup	HV 700 V, V _{DD} = V _{DD-OFF} + 1 V		1	20	μA
	R SECTION	•			-	
fosc	Frequency in Nominal Mode	Center Frequency	94	100	106	kHz
fosc-G	Green-Mode Frequency		14	18	22	kHz
D _{MAX}	Maximum Duty Cycle			85	1	%
f _{DV}	Frequency Variation vs. V _{DD} Deviation	V _{DD} = 9 V to 22 V		1	5	%
f _{DT}	Frequency Variation vs. Temperature Deviation (Note 11)	$T_A = -40 \text{ to } +105^{\circ}\text{C}$			5	%

Symbol	Parameter	Test Condition	Min	Тур	Max	Unit
V _{IN} SECTIOI	N		-	-	-	
V _{IN-ON}	PWM Turn-on Threshold Voltage		0.98	1.03	1.08	V
V _{IN-RL}	Release Latch Voltage		0.65	0.70	0.75	V
V _{IN-H}	Pull HIGH Latch Trigger Level		4.9	5.2	5.5	V
t _{IN-H}	Pull HIGH Latch Debounce Time			100		μs
V _{IN-L}	Pull LOW Auto Recovery Trigger Level		0.2	0.3	0.4	V
EEDBACK	INPUT SECTION		-		-	
Av	FB Voltage to Current-Sense Attenuation			1⁄4		V/V
Z_{FB}	Input Impedance			9.5		kΩ
$V_{\text{FB-OPEN}}$	Output High Voltage		5			V
V_{FB-OLP}	FB Open-Loop Trigger Level		4.4	4.6	4.8	V
t _{D-OLP}	Delay Time of FB Pin Open-loop Protection		50	56	59	ms
V_{FB-N}	Green-Mode Entry FB Voltage		2.3	2.5	2.7	V
V_{FB-G}	Green-Mode Ending FB Voltage			V _{FB-N} - 0.1		V
V _{FB-ZDC}	Zero Duty Cycle FB Voltage		1.9	2.1	2.3	V

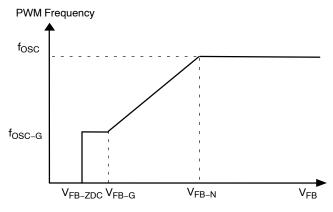


Figure 4. V_{FB} vs. PWM Frequency

Symbol	Parameter	Test Condition	Min	Тур	Max	Unit
CURRENT-	SENSE SECTION				-	
$I_{LIM at} V_{IN}$ = 1.2 V	Peak Current Limit	V _{IN} = 1.2 V	0.74	0.84	0.94	A
$I_{LIM at} V_{IN}$ = 3.6 V	Peak Current Limit	V _{IN} = 3.6 V	0.64	0.74	0.84	A
t _{SS}	Period during Soft Startup Time (Note 11)		4.5	5.0	5.5	ms
VER-TEM	PERATURE PROTECTION SECTION (OTP)					
			1	T		- I

T _{OTP}	Protection Junction Temperature (Notes 11, 13)		142	°C	
	(

11. These parameters, although guaranteed, are not 100% tested in production. 12. Pulse test: pulse width \leq 300 μ s, duty \leq 2%. 13. When activated, the output is disabled and the latch is turned off.

TYPICAL CHARACTERISTICS

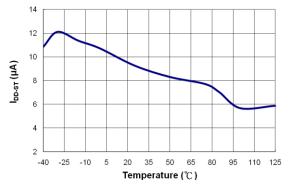


Figure 5. I_{DD-ST} vs. Temperature

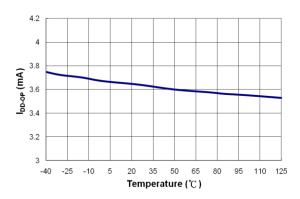


Figure 6. I_{DD-OP} vs. Temperature

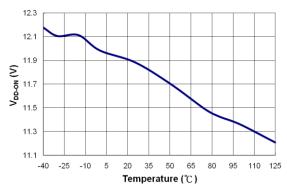


Figure 7. V_{DD-ON} vs. Temperature

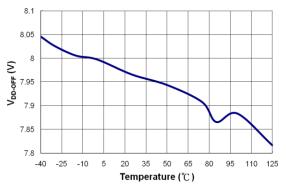


Figure 8. V_{DD-OFF} vs. Temperature

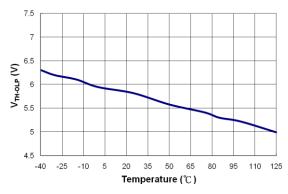


Figure 9. V_{TH-OLP} vs. Temperature

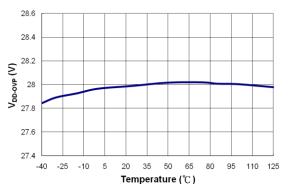


Figure 10. V_{DD-OVP} vs. Temperature

TYPICAL CHARACTERISTICS (continued)

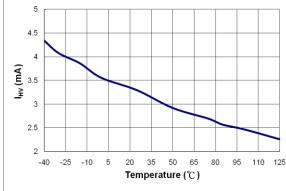


Figure 11. I_{HV} vs. Temperature

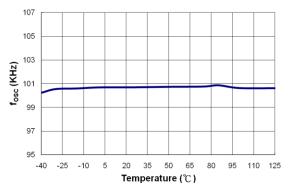


Figure 12. f_{OSC} vs. Temperature

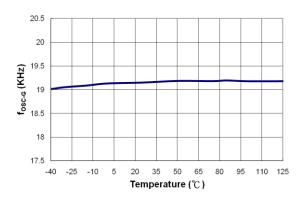


Figure 13. f_{OSC-G} vs. Temperature

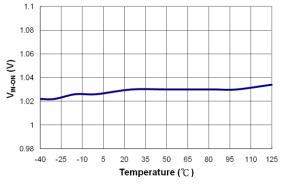


Figure 14. V_{IN-ON} vs. Temperature

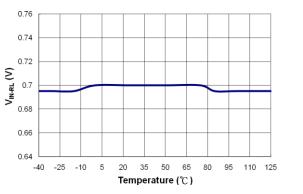


Figure 15. V_{IN-RL} vs. Temperature

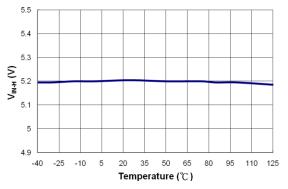


Figure 16. V_{IN-H} vs. Temperature

TYPICAL CHARACTERISTICS (continued)

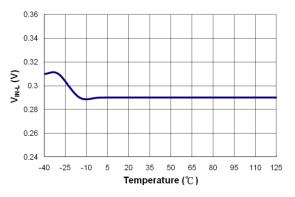


Figure 17. VIN-L vs. Temperature

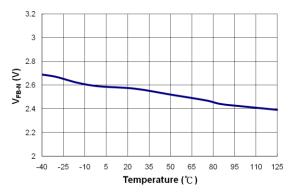


Figure 18. V_{FB-N} vs. Temperature

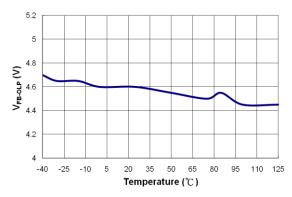


Figure 19. V_{FB-OLP} vs. Temperature

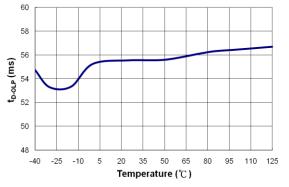


Figure 20. t_{D-OLP} vs. Temperature

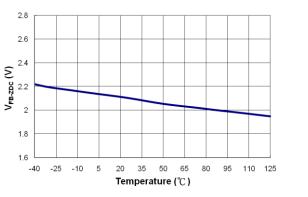


Figure 21. V_{FB-ZDC} vs. Temperature

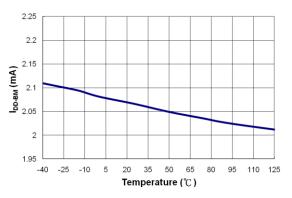


Figure 22. I_{DD-BM} vs. Temperature

FUNCTIONAL DESCRIPTION

Startup Operation

For startup, the HV pin is connected to the line input or bulk capacitor through the external resistor, R_{HV} , as shown in Figure 23. Typical startup current drawn from the HV pin is 3.5 mA and it charges the V_{DD} capacitor through the resistor R_{HV} . The startup current turns off when the V_{DD} capacitor voltage reaches V_{DD-ON} . The V_{DD} capacitor maintains V_{DD} until the auxiliary winding of the transformer provides the operating current.

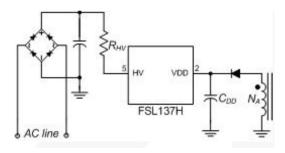


Figure 23. Startup Circuit

Slope Compensation

FSL137H is designed for flyback power converters. The peak–current–mode control is used to optimize system performance. Slope compensation is added to stabilize tcurrent loop. FSL137H inserts a synchronized, positively sloped ramp at each switching cycle.

Soft-Start

The FSL137H has internal soft-start circuit that slowly increases the SENSEFET current after startup. The typical soft-start time is 5 ms during which the V_{Limit} level is increased in six steps to smoothly establish the required output voltage, as shown in Figure 24. It also helps to prevent transformer saturation and reduce the stress on the secondary diode during startup.

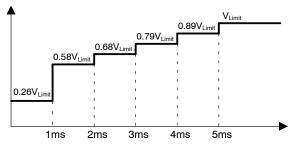


Figure 24. Soft-Start Function

Green-Mode Operation

The FSL137H uses feedback voltage (V_{FB}) as an indicator of the output load and modulates the PWM

frequency, as shown in Figure 25, such that the switching frequency decreases as load decreases. In heavy load conditions, the switching frequency is 100 kHz. Once V_{FB} decreases below V_{FB-N} (2.5 V), the PWM frequency starts to linearly decrease from 100 kHz to 18 kHz to reduce the switching losses. As V_{FB} decreases below V_{FB-G} (2.4 V), the switching frequency is fixed at 18 kHz and FSL137H enters into "deep" green mode to reduce the standby power consumption. As VFB decreases below V_{FB-ZDC} (2.1 V), FSL137H enters into burst-mode operation. When VFB drops below VFB-ZDC, FSL137H stops switching and the output voltage starts to drop, which causes the feedback voltage to rise. Once VFB rises above V_{FB-ZDC}, switching resumes. Burst mode alternately enables and disables switching, thereby reducing switching loss to improve power saving, as shown in Figure 26.

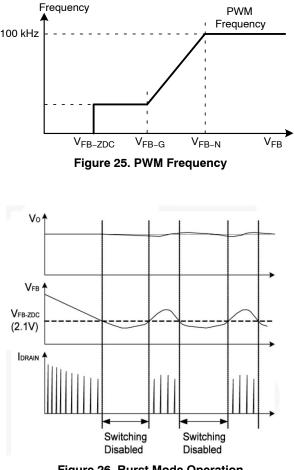
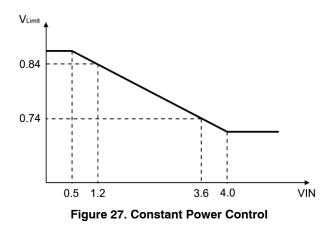


Figure 26. Burst Mode Operation

Constant Power Control

To limit the output power of the converter constantly, high/low line compensation is included. Sensing the converter input voltage through the VIN pin, the high/low line compensation function generates a relative peak-current-limit threshold voltage for constant power control, as shown in Figure 27.

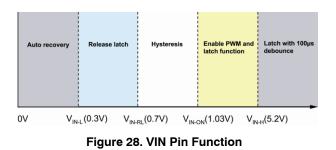


Protections

The FSL137H provides full protection functions to prevent the power supply and the load from being damaged. The protection features include:

Latch/Auto Recovery Function

The FSL137H provides additional protections by the VIN pin, such as pull–HIGH latch and pull–LOW auto recovery that depend on the application. As shown in Figure 28, when V_{IN} is higher than 5.2 V, FSL137H is latched until the V_{DD} is discharged. FSL137H is in auto recovery when V_{IN} is lower than 0.3 V.



Open-Loop/Overload Protection (OLP)

When the upper branch of the voltage divider for the shunt regulator (KA431 shown) is broken, as shown in Figure 29,

or over current or output short occurs. There is no current flowing through the opto-coupler transistor, which pulls up the feedback voltage to 6 V. When the feedback voltage is above 4.6 V for longer than 56 ms, OLP is triggered. This protection is also triggered when the SMPS output drops below the nominal value longer than 56 ms due to the overload condition.

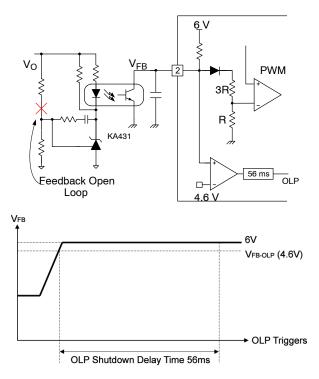


Figure 29. OLP Operation

VDD Over–Voltage Protection (OVP)

 V_{DD} over-voltage protection prevents IC damage caused by over voltage on the V_{DD} pin. The OVP is triggered when V_{DD} reaches 28 V. It has a debounce time (typically 130 µs) to prevent false trigger by switching noise.

Over-Temperature Protection (OTP)

The SENSEFET and the control IC are integrated, making it easier to detect the temperature of the SENSEFET. When the temperature exceeds approximately 142°C, thermal shutdown is activated.

TYPICAL APPLICATION CIRCUIT

Table 7.

Application	Devices	Input Voltage Range	Output
Adapter	FSL137H	90-264Vac	12 V/1 A (12 W)

Features

- High efficiency (>77.76% at full load) meeting Energy Star V2.0 regulation with enough margin
- Standby power < 100mW at no–load condition
- Provides full protection functions:

Table 8.

OVP	ОТР	OLP	VIN-H	VIN-L
Latch	Latch	Auto Restart	Latch	Auto Restart

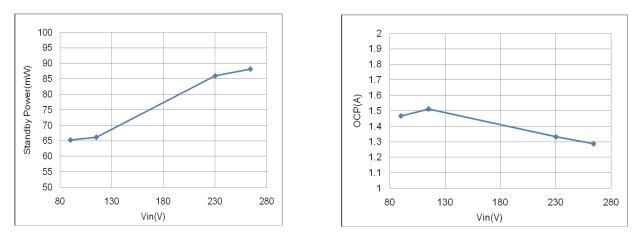


Figure 30. Measured Standby Power and OCP

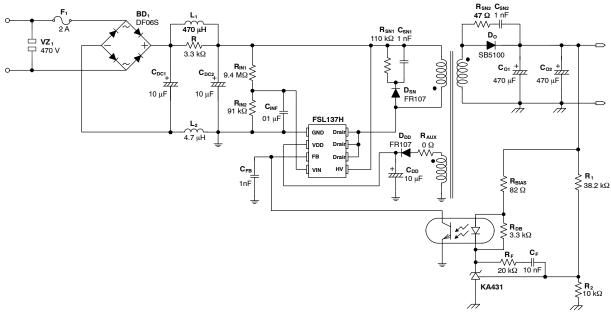


Figure 31. Schematic of Typical Application Circuit

TYPICAL APPLICATION CIRCUIT (continued)

Transformer Specification

- Core: EE16
- Bobbin: EE16

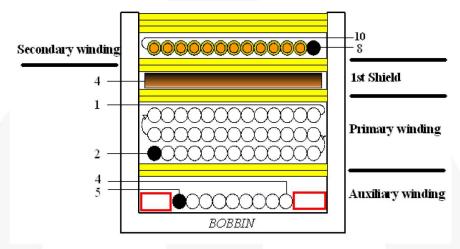


Figure 32. Transformer Diagram

Table 9.

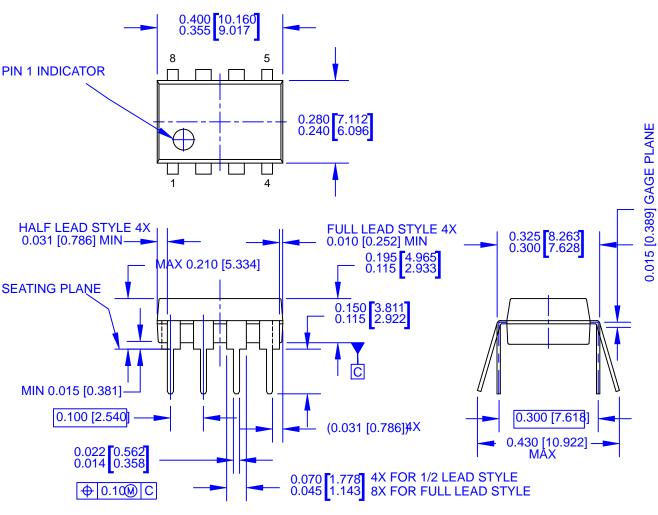
	Terminal			
NO.	S	F	Wire	Ts
W1	5	4	2UEW 0.3*1	13
W2	2	1	2UEW 0.26*1	75
W3	4	-	Copper Shield	1.2
W4	8	10	TEX-E 0.35*1	13
			Core Rounding Tape	3
Primary-Side Inductance	= 600 μH ±5%	•	•	•
Primary-Side Effective Le	akage < 20 μH ±5%			

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DATE 31 JUL 2016



NOTES:

A) THIS PACKAGE CONFORMS TOBEC MS-001 VARIATION BA WHICH DEFINES
2 VERSIONS OF THE PACKAGE TERMINAL STYLE WHICH ARE SHOWN HERE.
B) CONTROLING DIMS ARE IN INCHES

C) DIMENSIONS ARE EXCLUSIVE OF BURRSMOLD FLASH, AND TIE BAR EXTRUSIONS.

D) DIMENSION AND TOLERANCES PER ASME Y14.5M-2009

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