3.3 V/5 V ECL 2:1 Multiplexer

MC100EP58

Description

The MC100EP58 is a 2:1 multiplexer. The device is pin and functionally equivalent to the EL58 and LVEL58 devices.

The 100 Series contains temperature compensation.

Features

- 310 ps Typical Propagation Delay
- Maximum Frequency > 3 GHz Typical
- PECL Mode Operating Range:
  - V_{CC} = 3.0 V to 5.5 V with V_{EE} = 0 V
- NECL Mode Operating Range:
  - V_{CC} = 0 V with V_{EE} = −3.0 V to −5.5 V
- Open Input Default State
- Q Output Will Default LOW with Inputs Open or at V_{EE}
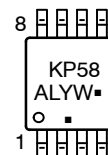- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

ON Semiconductor®

www.onsemi.com

8
1

TSSOP−8
DT SUFFIX
CASE 948R−02

MARKING DIAGRAM*

8
KP58
ALYW■

1

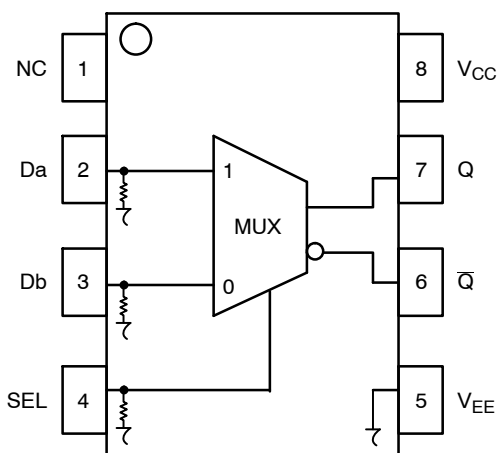| K | = MC100 |
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
■	= Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping
MC100EP58DTG	TSSOP−8 (Pb-Free)	100 Units / Tube

MC100EP58

Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

Table 1. PIN DESCRIPTION

PIN	FUNCTION
Da*, Db*	ECL Data Inputs
SEL*	ECL Select Inputs
Q, $\overline{Q}$	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

* Pins will default LOW when left open.

Table 2. TRUTH TABLE

SEL	Data
H L	a b

Table 3. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 kΩ
Internal Input Pullup Resistor	N/A

ESD Protection
  Human Body Model
  Machine Model
  Charged Device Model
	> 4 kV
	> 200 V
	> 2 kV

Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb-Free Pkg
TSSOP−8	Level 3
Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count	41 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		6	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		−6	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 −6	V
I_{out}	Output Current	Continuous Surge		50 100	mA
I_{BB}	V_{BB} Sink/Source			±0.5	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP−8	185 140	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP−8	41 to 44	°C/W
T_{sol}	Wave Solder (Pb-Free)	<2 to 3 sec @ 260°C		265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. JEDEC standard multilayer board − 2S2P (2 signal, 2 power)

Table 5. 100EP DC CHARACTERISTICS, PECL (V_{CC} = 3.3 V, V_{EE} = 0 V (Note 1))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	20	28	37	20	31	39	25	33	42	mA
V_{OH}	Output HIGH Voltage (Note 2)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 2)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2075		2420	2075		2420	2075		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1355		1675	1355		1675	1355		1675	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to −2.2 V.
2. All loading with 50 Ω to V_{CC} − 2.0 V.

Table 6. 100EP DC CHARACTERISTICS, PECL (V_{CC} = 5.0 V, V_{EE} = 0 V (Note 1))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	20	28	37	20	31	39	25	33	42	mA
V_{OH}	Output HIGH Voltage (Note 2)	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
V_{OL}	Output LOW Voltage (Note 2)	3055	3180	3305	3055	3180	3305	3055	3180	3305	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3775		4120	3775		4120	3775		4120	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3055		3375	3055		3375	3055		3375	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +2.0 V to −0.5 V.
2. All loading with 50 Ω to V_{CC} − 2.0 V.

Table 7. 100EP DC CHARACTERISTICS, NECL (V_{CC} = 0 V, V_{EE} = −5.5 V to −3.0 V (Note 1))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	20	28	37	20	31	39	25	33	42	mA
V_{OH}	Output HIGH Voltage (Note 2)	−1145	−1020	−895	−1145	−1020	−895	−1145	−1020	−895	mV
V_{OL}	Output LOW Voltage (Note 2)	−1945	−1820	−1695	−1945	−1820	−1695	−1945	−1820	−1695	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	−1225		−880	−1225		−880	−1225		−880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	−1945		−1625	−1945		−1625	−1945		−1625	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.
1. Input and output parameters vary 1:1 with V_{CC}.
2. All loading with 50 Ω to V_{CC} − 2.0 V.

Table 8. AC CHARACTERISTICS (V_{CC} = 0 V; V_{EE} = −3.0 V to −5.5 V or V_{CC} = 3.0 V to 5.5 V; V_{EE} = 0 V (Note 1))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency (See Figure 2. F_{max}/JITTER)		> 3			> 3			> 3		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential D to Q,$\overline{Q}$ SEL to Q,$\overline{Q}$	200	280	380	210	310	410	220	340	420	ps
t_{JITTER}	Cycle-to-Cycle Jitter (See Figure 2. F_{max}/JITTER)		0.2	< 2		0.2	< 2		0.2	< 2	ps
V_{PP}	Input Voltage Swing (Differential Configuration)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times Q, $\overline{Q}$ (20% − 80%)	70	120	170	80	130	180	100	150	200	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.
1. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} − 2.0 V.
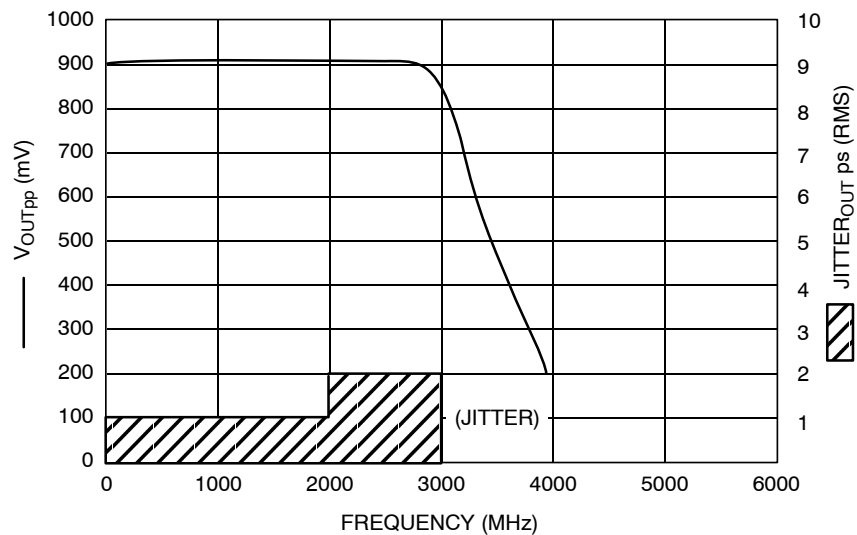
Figure 2. F$_{max}$/Jitter

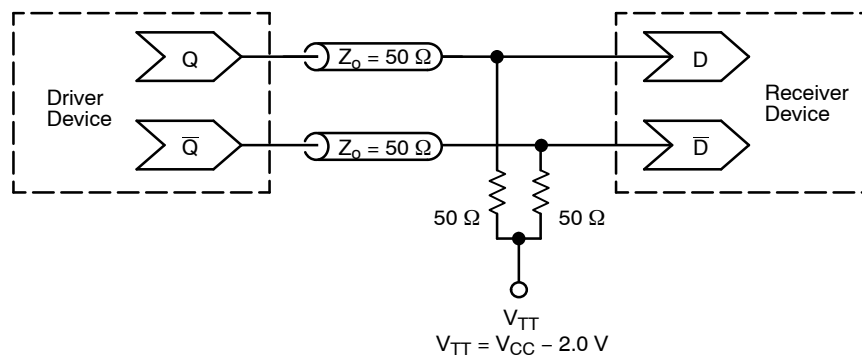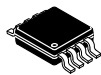**Figure 3. Typical Termination for Output Driver and Device Evaluation**
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

$V_{TT} = V_{CC} - 2.0\ V$

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

TSSOP 8
CASE 948R−02
ISSUE A

DATE 04/07/2000

SCALE 2:1

8x **K** REF

0.15 (0.006) T U Ⓢ

⊕ 0.10 (0.004) Ⓜ T U Ⓢ V Ⓢ

2X **L/2**

8 □ □ 5

B
−U−

PIN 1
IDENT

1 □ □ 4

0.15 (0.006) T U Ⓢ

A
−V−

0.25 (0.010)

M

F

DETAIL E

C

0.10 (0.004)

−T− SEATING
PLANE

D

G

DETAIL E

−W−
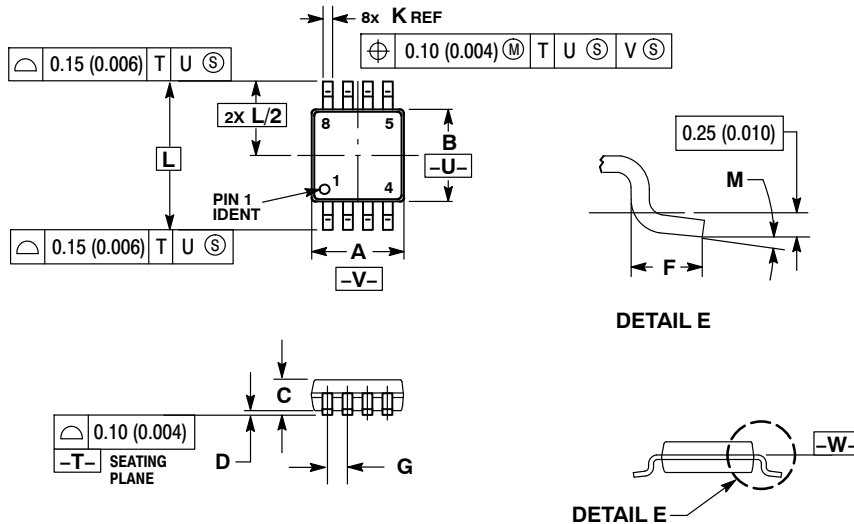
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0 °	6 °	0 °	6 °

DOCUMENT NUMBER:	98AON00236D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**TSSOP 8**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

◊