MC14503B

Hex Non-Inverting 3-State Buffer

The MC14503B is a hex non−inverting buffer with 3−state outputs, and a high current source and sink capability. The 3−state outputs make it useful in common bussing applications. Two disable controls are provided. A high level on the Disable A input causes the outputs of buffers 1 through 4 to go into a high impedance state and a high level on the Disable B input causes the outputs of buffers 5 and 6 to go into a high impedance state.

Features

- 3−State Outputs
- TTL Compatible – Will Drive One TTL Load Over Full Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Two Disable Controls for Added Versatility
- Pin for Pin Replacement for MM80C97 and 340097
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This Device is Pb−Free and is RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1)

Parameter	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	−0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	V_{in}, V_{out}	−0.5 to V_{DD} + 0.5	V
Input Current (DC or Transient) per Pin	I_{in}	±10	mA
Output Current (DC or Transient) per Pin	I_{out}	±25	mA
Power Dissipation, per Package (Note 2)	P_D	500	mW
Ambient Temperature Range	T_A	−55 to +125	°C
Storage Temperature Range		−65 to +150	°C
Lead Temperature (8–Second Soldering)		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
   "D/DW" Package: −7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.
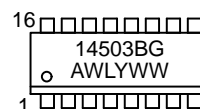
ON Semiconductor®

http://onsemi.com
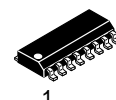
SOIC−16
D SUFFIX
CASE 751B

PIN ASSIGNMENT

DIS A	1●	16	V_{DD}
IN 1	2	15	DIS B
OUT 1	3	14	IN 6
IN 2	4	13	OUT 6
OUT 2	5	12	IN 5
IN 3	6	11	OUT 5
OUT 3	7	10	IN 4
V_{SS}	8	9	OUT 4

MARKING DIAGRAM

```
16 □□□□□□□□
    14503BG
o   AWLYWW
1  □□□□□□□□
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A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G	= Pb−Free Package

TRUTH TABLE

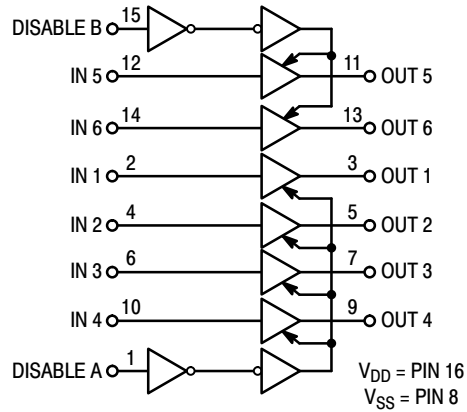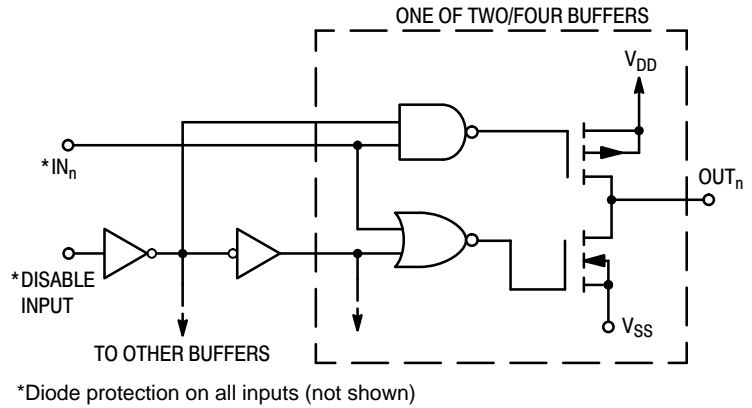| In_n	Appropriate Disable Input	Out_n
0	0	0
1	0	1
X	1	High Impedance

X = Don't Care

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MC14503B

LOGIC DIAGRAM

DISABLE B o—15
IN 5 o—12 — 11 o OUT 5
IN 6 o—14 — 13 o OUT 6
IN 1 o—2 — 3 o OUT 1
IN 2 o—4 — 5 o OUT 2
IN 3 o—6 — 7 o OUT 3
IN 4 o—10 — 9 o OUT 4
DISABLE A o—1

V_{DD} = PIN 16
V_{SS} = PIN 8

CIRCUIT DIAGRAM

ONE OF TWO/FOUR BUFFERS

*IN$_n$

*DISABLE INPUT

TO OTHER BUFFERS

V_{DD}

OUT$_n$

V_{SS}

*Diode protection on all inputs (not shown)

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	−55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (Note 3)	Max	Min	Max	
Output Voltage "0" Level V_{in} = 0		V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
			10	–	0.05	–	0	0.05	–	0.05	
			15	–	0.05	–	0	0.05	–	0.05	
"1" Level V_{in} = V_{DD}		V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
			10	9.95	–	9.95	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level (V_O = 3.6 or 1.4 Vdc) (V_O = 7.2 or 2.8 Vdc) (V_O = 11.5 or 3.5 Vdc)		V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
			10	–	3.0	–	4.50	3.0	–	3.0	
			15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level (V_O = 1.4 or 3.6 Vdc) (V_O = 2.8 or 7.2 Vdc) (V_O = 3.5 or 11.5 Vdc)		V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
			10	7.0	–	7.0	5.50	–	7.0	–	
			15	11	–	11	8.25	–	11	–	
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	4.5	−4.3	–	−3.6	−5.0	–	−2.5	–	mAdc
			5.0	−5.8	–	−4.8	−6.1	–	−3.0	–	
			5.0	−1.2	–	−1.02	−1.4	–	−0.7	–	
			10	−3.1	–	−2.6	−3.7	–	−1.8	–	
			15	−8.2	–	−6.8	−14.1	–	−4.8	–	
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	4.5	2.2	–	1.8	2.1	–	1.2	–	mAdc
			5.0	2.6	–	2.1	2.3	–	1.3	–	
			10	6.5	–	5.5	6.2	–	3.8	–	
			15	19.2	–	16.1	25	–	11.2	–	
Input Current		I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Capacitance, (V_{in} = 0)		C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current, (Per Package)		I_Q	5.0	–	1.0	–	0.002	1.0	–	30	µAdc
			10	–	2.0	–	0.004	2.0	–	60	
			15	–	4.0	–	0.006	4.0	–	120	
Total Supply Current (Note 4, 5) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs) (All outputs switching, 50% Duty Cycle)		I_T	5.0	I_T = (2.5 µA/kHz) f + I_{DD}							µAdc
			10	I_T = (6.0 µA/kHz) f + I_{DD}							
			15	I_T = (10 µA/kHz) f + I_{DD}							
3–State Output Leakage Current		I_{TL}	15	–	±0.1	–	±0.0001	±0.1	–	±3.0	µAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
4. The formulas given are for the typical characteristics only at 25°C.
5. To calculate total supply current at loads other than 50 pF: $I_T(C_L)$ = I_T(50 pF) + (C_L − 50) Vfk where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.006.

SWITCHING CHARACTERISTICS (Note 6) (C_L = 50 pF, $T_A = 25°C$)

Characteristic	Symbol	V_{DD} V_{CC}	All Types		Unit
			Typ (Note 7)	Max	
Output Rise Time t_{TLH} = (0.5 ns/pF) C_L + 20 ns t_{TLH} = (0.3 ns/pF) C_L + 8.0 ns t_{TLH} = (0.2 ns/pF) C_L + 8.0 ns	t_{TLH}	5.0 10 15	45 23 18	90 45 35	ns
Output Fall Time t_{THL} = (0.5 ns/pF) C_L + 20 ns t_{THL} = (0.3 ns/pF) C_L + 8.0 ns t_{THL} = (0.2 ns/pF) C_L + 8.0 ns	t_{THL}	5.0 10 15	45 23 18	90 45 35	ns
Turn–Off Delay Time, all Outputs t_{PLH} = (0.3 ns/pF) C_L + 60 ns t_{PLH} = (0.15 ns/pF) C_L + 27 ns t_{PLH} = (0.1 ns/pF) C_L + 20 ns	t_{PLH}	5.0 10 15	75 35 25	150 70 50	ns
Turn–On Delay Time, all Outputs t_{PHL} = (0.3 ns/pF) C_L + 60 ns t_{PHL} = (0.15 ns/pF) C_L + 27 ns t_{PHL} = (0.1 ns/pF) C_L + 20 ns	t_{PHL}	5.0 10 15	75 35 25	150 70 50	ns
3–State Propagation Delay Time Output "1" to High Impedance	t_{PHZ}	5.0 10 15	75 40 35	150 80 70	ns
Output "0" to High Impedance	t_{PLZ}	5.0 10 15	80 40 35	160 80 70	ns
High Impedance to "1" Level	t_{PZH}	5.0 10 15	65 25 20	130 50 40	ns
High Impedance to "0" Level	t_{PZL}	5.0 10 15	100 35 25	200 70 50	ns

6. The formulas given are for the typical characteristics only at 25°C.
7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
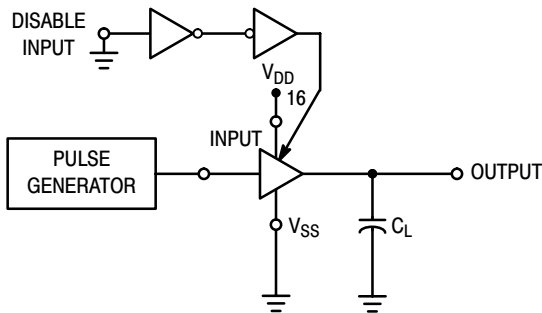
Figure 1. Switching Time Test Circuit and Waveforms
(t_{TLH}, t_{THL}, t_{PHL}, and t_{PLH})

MC14503B
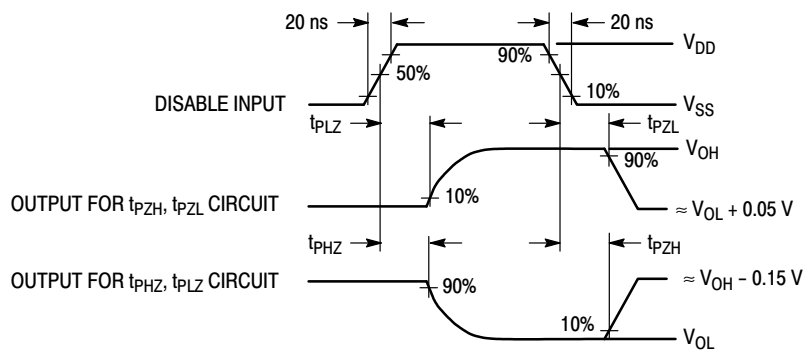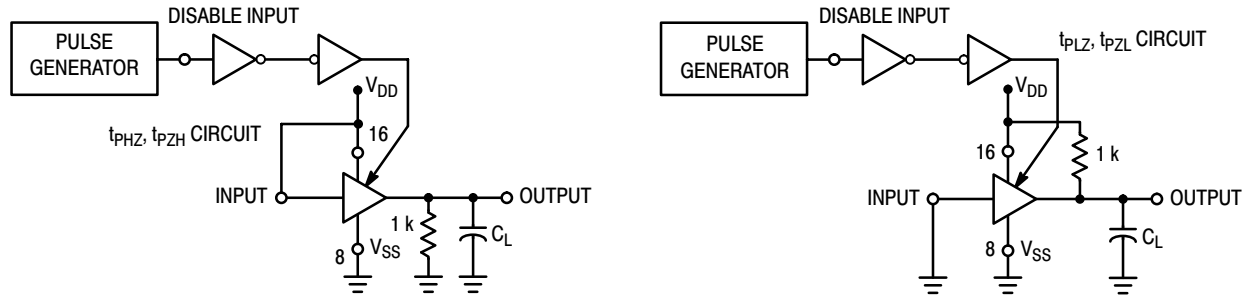
Figure 2. 3−State AC Test Circuit and Waveforms
(t_{PLZ}, t_{PHZ}, t_{PZH}, t_{PZL})

ORDERING INFORMATION

Device	Package	Shipping†
MC14503BDG	SOIC−16 (Pb−Free)	48 / Rail
MC14503BDR2G	SOIC−16 (Pb−Free)	2500 / Tape & Reel
NLV14503BDR2G*	SOIC−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.
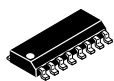
SCALE 1:1

SOIC−16
CASE 751B−05
ISSUE K

DATE 29 DEC 2006
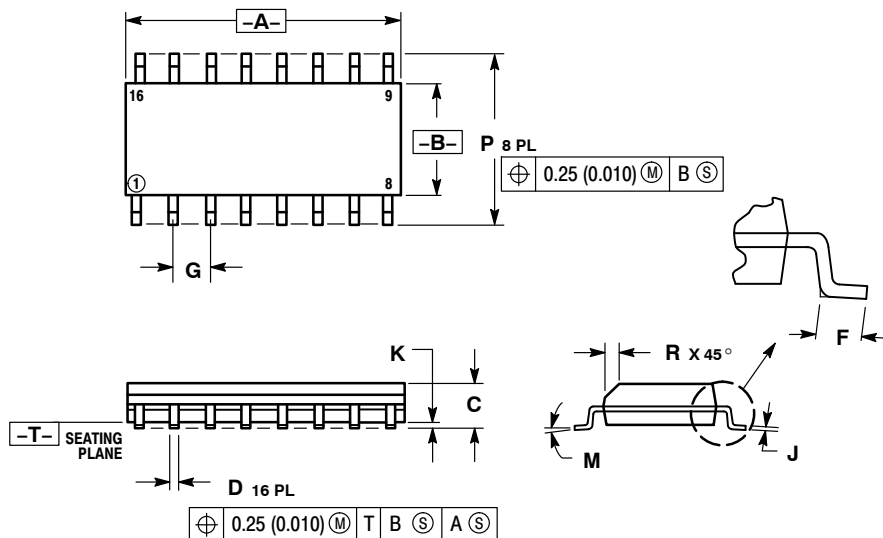
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

P 8 PL

⊕ 0.25 (0.010) Ⓜ B Ⓢ

G

K

C

−T− SEATING PLANE

D 16 PL

⊕ 0.25 (0.010) Ⓜ T B Ⓢ A Ⓢ

R X 45°

F

M   **J**

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

RECOMMENDED SOLDERING FOOTPRINT*

8X
6.40

16X 1.12

16X
0.58

1.27
PITCH
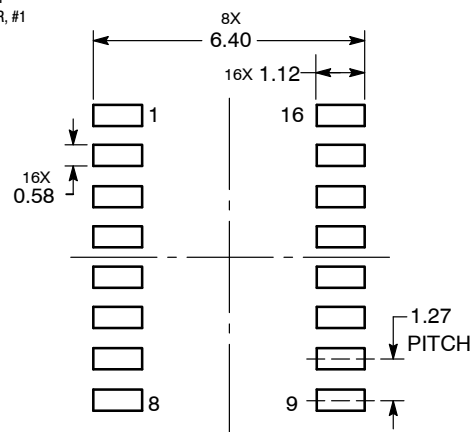
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	SOIC−16	PAGE 1 OF 1

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical–documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales

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