## Dual 1-of-4 Decoder/ Demultiplexer

High-Performance Silicon-Gate CMOS MC74HC139A

The MC74HC139A is identical in pinout to the LS139. The device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

This device consists of two independent 1-of-4 decoders, each of which decodes a two-bit Address to one-of-four active-low outputs. Active-low Selects are provided to facilitate the demultiplexing and cascading functions. The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and utilizing the Select as a data input.

## Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: $1.0 \mu \mathrm{~A}$
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 100 FETs or 25 Equivalent Gates
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable*
- These Devices are $\mathrm{Pb}-$ Free, Halogen Free/BFR Free and are RoHS Compliant


SOIC-16 D SUFFIX CASE 751B


TSSOP-16
DT SUFFIX
CASE 948F


QFN16
MN SUFFIX
CASE 485AW

MARKING DIAGRAMS


XXXX
ALYW.
ALYW•

A = Assembly Location
WL, L = Wafer Lot
YY, $\mathrm{Y}=$ Year
WW, W = Work Week
G or • = Pb-Free Package
(Note: Microdot may be in either location)

## PIN ASSIGNMENT



## ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

## MC74HC139A



## FUNCTION TABLE

| Inputs |  |  | Outputs |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Select | A1 | A0 | Y0 | Y1 | Y2 | Y3 |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | L | H | H | L | H | H |
| L | H | L | H | H | L | H |
| L | H | H | H | H | H | L |

X = don't care

Figure 1. Logic Diagram

MAXIMUM RATINGS

| Symbol | Parameter |  | Value | Unit |
| :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | DC Supply Voltage |  | -0.5 to +6.5 | V |
| $\mathrm{V}_{\text {IN }}$ | DC Input Voltage |  | -0.5 to $\mathrm{V}_{\mathrm{CC}}+0.5$ | V |
| $\mathrm{V}_{\text {OUT }}$ | DC Output Voltage |  | -0.5 to $\mathrm{V}_{\mathrm{CC}}+0.5$ | V |
| In | DC Input Current, per Pin |  | $\pm 20$ | mA |
| Iout | DC Output Current, per Pin |  | $\pm 25$ | mA |
| $\mathrm{I}_{\mathrm{CC}}$ | DC Supply Current, $\mathrm{V}_{\mathrm{CC}}$ and GND Pins |  | $\pm 50$ | mA |
| $\mathrm{IIK}^{\prime}$ | Input Clamp Current ( $\mathrm{V}_{\text {IN }}<0$ or $\mathrm{V}_{\text {IN }}>\mathrm{V}_{\text {CC }}$ ) |  | $\pm 20$ | mA |
| $\mathrm{l}_{\text {OK }}$ | Output Clamp Current ( $\mathrm{V}_{\text {OUT }}<0$ or $\mathrm{V}_{\text {OUT }}>\mathrm{V}_{\text {CC }}$ ) |  | $\pm 20$ | mA |
| $\mathrm{T}_{\text {STG }}$ | Storage Temperature |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\mathrm{L}}$ | Lead Temperature, 1 mm from Case for 10 Seconds |  | 260 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{J}$ | Junction Temperature Under Bias |  | $\pm 150$ | ${ }^{\circ} \mathrm{C}$ |
| $\theta_{\mathrm{JA}}$ | Thermal Resistance (Note 1) | $\begin{array}{r} \text { SOIC-16 } \\ \text { QFN16 } \\ \text { TSSOP-16 } \end{array}$ | $\begin{aligned} & \hline 126 \\ & 118 \\ & 159 \end{aligned}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $P_{\text {D }}$ | Power Dissipation in Still Air at $25^{\circ} \mathrm{C}$ | $\begin{array}{r} \text { SOIC-16 } \\ \text { QFN16 } \\ \text { TSSOP-16 } \end{array}$ | $\begin{gathered} \hline 995 \\ 1062 \\ 787 \end{gathered}$ | mW |
| MSL | Moisture Sensitivity |  | Level 1 | - |
| $\mathrm{F}_{\mathrm{R}}$ | Flammability Rating | Oxygen Index: 28 to 34 | $\begin{gathered} \text { UL } 94 \text { V-0 @ } \\ 0.125 \text { in } \end{gathered}$ | - |
| $\mathrm{V}_{\text {ESD }}$ | ESD Withstand Voltage (Note 2) | Human Body Model Charged Device Model | $\begin{aligned} & 2000 \\ & 1000 \end{aligned}$ | V |
| I ${ }_{\text {LATCHUP }}$ | Latchup Performance (Note 3) |  | $\pm 100$ | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76 mm -by- $114 \mathrm{~mm}, 2$-ounce copper trace no air flow per JESD51-7.
2. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.
3. Tested to EIA/JESD78 Class II.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
| :---: | :--- | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | DC Supply Voltage | 2.0 | 6.0 | V |
| $\mathrm{~V}_{\mathrm{IN}}, \mathrm{V}_{\mathrm{OUT}}$ | DC Input Voltage, Output Voltage | 0 | $\mathrm{~V}_{\mathrm{CC}}$ | V |
| $\mathrm{T}_{\mathrm{A}}$ | Operating Temperature, All Package Types | -55 | +125 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{t}_{\mathrm{r}}, \mathrm{t}_{\mathrm{f}}$ | Input Rise and Fall Time |  |  | $\mathrm{V}_{\mathrm{CC}}=2.0 \mathrm{~V}$ |
|  | (Figure 3) | $\mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}$ | 0 | 1000 |
|  |  | $\mathrm{~V}_{\mathrm{CC}}=6.0 \mathrm{~V}$ | 0 | 500 |
| nss |  |  |  |  |
|  |  | 0 | 400 |  |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
4. Unused inputs may not be left open. All inputs must be tied to a high-logic voltage level or a low-logic input voltage level.

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | $\begin{gathered} \mathrm{v}_{\mathrm{cc}} \\ \mathrm{v} \\ \hline \end{gathered}$ | Guaranteed Limit |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | $-55^{\circ} \mathrm{C}$ to $25^{\circ} \mathrm{C}$ | $\leq 85^{\circ} \mathrm{C}$ | $\leq 125^{\circ} \mathrm{C}$ |  |
| $\mathrm{V}_{\mathrm{IH}}$ | Minimum High-Level Input Voltage | $\begin{aligned} & \hline \mathrm{V}_{\text {OUT }}=0.1 \mathrm{~V} \text { or } \mathrm{V}_{\mathrm{CC}}-0.1 \mathrm{~V} \\ & \mid \mathrm{l}_{\text {OUT }} \leq 20 \mu \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{gathered} 1.5 \\ 3.15 \\ 4.2 \end{gathered}$ | $\begin{gathered} \hline 1.5 \\ 3.15 \\ 4.2 \end{gathered}$ | $\begin{gathered} \hline 1.5 \\ 3.15 \\ 4.2 \end{gathered}$ | V |
| VIL | Maximum Low-Level Input Voltage | $\begin{aligned} & \hline \mathrm{V}_{\text {OUT }}=0.1 \mathrm{~V} \text { or } \mathrm{V}_{\mathrm{CC}}-0.1 \mathrm{~V} \\ & \mid \mathrm{l}_{\text {OUT }} \leq 20 \mu \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{gathered} 0.5 \\ 1.35 \\ 1.8 \end{gathered}$ | $\begin{gathered} 0.5 \\ 1.35 \\ 1.8 \end{gathered}$ | $\begin{gathered} 0.5 \\ 1.35 \\ 1.8 \end{gathered}$ | V |
| $\mathrm{V}_{\mathrm{OH}}$ | Minimum High-Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IH}} \text { or } \mathrm{V}_{\mathrm{IL}} \\ & \mid l_{\text {lout }} \leq 20 \mu \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & 1.9 \\ & 4.4 \\ & 5.9 \end{aligned}$ | $\begin{aligned} & 1.9 \\ & 4.4 \\ & 5.9 \end{aligned}$ | $\begin{aligned} & 1.9 \\ & 4.4 \\ & 5.9 \end{aligned}$ | V |
|  |  |  | $\begin{aligned} & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & 3.98 \\ & 5.48 \end{aligned}$ | $\begin{aligned} & 3.84 \\ & 5.34 \end{aligned}$ | $\begin{aligned} & 3.70 \\ & 5.20 \end{aligned}$ |  |
| V OL | Maximum Low-Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IH}} \text { or } \mathrm{V}_{I L} \\ & \mid \mathrm{lout}^{\prime} \leq 20 \mu \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & \hline 0.1 \\ & 0.1 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & \hline 0.1 \\ & 0.1 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & \hline 0.1 \\ & 0.1 \\ & 0.1 \end{aligned}$ | V |
|  |  | $\mathrm{V}_{\text {IN }}=\mathrm{V}_{\text {IH }}$ or $\mathrm{V}_{\mathrm{IL}} \quad$$\left\lvert\, \begin{array}{l}\text { lout } \\ \mid \text { lout }\end{array} \leq 4.0 \mathrm{~mA}\right.$ <br> 1.2 mA | $\begin{aligned} & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & 0.26 \\ & 0.26 \end{aligned}$ | $\begin{aligned} & 0.33 \\ & 0.33 \end{aligned}$ | $\begin{aligned} & 0.40 \\ & 0.40 \end{aligned}$ |  |
| $\mathrm{I}_{\mathrm{N}}$ | Maximum Input Leakage Current | $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\text {CC }}$ or GND | 6.0 | $\pm 0.1$ | $\pm 1.0$ | $\pm 1.0$ | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\mathrm{CC}}$ | Maximum Quiescent Supply Current (per Package) | $\begin{aligned} & \mathrm{V}_{\text {IN }}=\mathrm{V}_{\mathrm{CC}} \text { or GND } \\ & \text { lout }=0 \mu \mathrm{~A} \end{aligned}$ | 6.0 | 4 | 40 | 160 | $\mu \mathrm{A}$ |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | $\begin{gathered} \mathrm{V}_{\mathrm{cc}} \\ \mathrm{~V} \end{gathered}$ | Guaranteed Limit |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $-55^{\circ} \mathrm{C}$ to $25^{\circ} \mathrm{C}$ | $\leq 85^{\circ} \mathrm{C}$ | $\leq 125^{\circ} \mathrm{C}$ |  |
| $\begin{aligned} & \mathrm{t}_{\text {PLH }}, \\ & \mathrm{t}_{\text {PHL }} \end{aligned}$ | Maximum Propagation Delay, Select to Output $Y$ (Figures 2 and 3) | 2.0 | 115 | 145 | 175 | ns |
|  |  | 4.5 | 23 | 29 | 35 |  |
|  |  | 6.0 | 20 | 25 | 30 |  |
| ${ }_{\text {tpLH }}$, <br> ${ }_{\text {tpHL }}$ | Maximum Propagation Delay, Input A to Output $Y$ (Figures 2 and 4) | 2.0 | 115 | 145 | 175 | ns |
|  |  | 4.5 | 23 | 29 | 35 |  |
|  |  | 6.0 | 20 | 25 | 30 |  |
| $\begin{aligned} & \mathrm{t}_{\mathrm{TLH}}, \\ & \mathrm{t}_{\mathrm{TH}} \end{aligned}$ | Maximum Output Transition Time, Any Output (Figures 2 and 3) | 2.0 | 75 | 95 | 110 | ns |
|  |  | 4.5 | 15 | 19 | 22 |  |
|  |  | 6.0 | 13 | 16 | 19 |  |
| $\mathrm{C}_{\text {in }}$ | Maximum Input Capacitance | - | 10 | 10 | 10 | pF |


|  |  | Typical @ $\mathbf{2 5}{ }^{\circ} \mathbf{C}, \mathbf{V} \mathbf{C C}=\mathbf{5 . 0} \mathbf{V}$ |  |
| :--- | :--- | :---: | :---: |
| $\mathbf{n}$ | pF |  |  |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
5. Used to determine the no-load dynamic power consumption: $P_{D}=C_{P D} V_{C C}{ }^{2} f+I_{C C} V_{C C}$.

## MC74HC139A

SWITCHING WAVEFORMS AND TEST CIRCUIT


| Test | Switch Position | $\mathbf{C}_{\mathbf{L}}$ | $\mathbf{R}_{\mathbf{L}}$ |
| :---: | :---: | :---: | :---: |
| $\mathrm{t}_{\mathrm{PLH}} / \mathrm{t}_{\mathrm{PHL}}$ | Open | 50 pF | $1 \mathrm{k} \Omega$ |
| $\mathrm{t}_{\mathrm{PLZ}} / \mathrm{t}_{\mathrm{PZL}}$ | $\mathrm{V}_{\mathrm{CC}}$ |  |  |
| $\mathrm{t}_{\mathrm{PHZ}} / \mathrm{t}_{\mathrm{PZH}}$ | GND |  |  |

Figure 2. Test Circuit


Figure 3. Switching Waveform


Figure 4. Switching Waveform

## PIN DESCRIPTIONS

## ADDRESS INPUTS

$A 0_{a}, A 1_{a}, A 0_{b}, A 1_{b}$ (Pins 2, 3, 14, 13)
Address inputs. These inputs, when the respective 1 -of -4 decoder is enabled, determine which of its four active-low outputs is selected.

## CONTROL INPUTS

## Select $_{\mathrm{a}}$, Select $_{\mathrm{b}}$ (Pins 1, 15)

Active-low select inputs. For a low level on this input, the outputs for that particular decoder follow the Address
inputs. A high level on this input forces all outputs to a high level.

## OUTPUTS

$$
\mathrm{Y} 0_{\mathrm{a}}-\mathrm{Y} 3_{\mathrm{a}}, \mathrm{Y} 0_{\mathrm{b}}-\mathrm{Y} 3_{\mathrm{b}}(\text { Pins } 4-7,12,11,10,9)
$$

Active-low outputs. These outputs assume a low level when addressed and the appropriate Select input is active. These outputs remain high when not addressed or the appropriate Select input is inactive.


Figure 5. Expanded Logic Diagram
(1/2 of Device)

## MC74HC139A

ORDERING INFORMATION

| Device | Marking | Package | Shipping $^{\dagger}$ |
| :--- | :---: | :---: | :---: |
| MC74HC139ADR2G | HC139AG | SOIC-16 | $2500 /$ Tape \& Reel |
| MC74HC139ADR2G-Q* | HC139AG | SOIC-16 | $2500 /$ Tape \& Reel |
| MC74HC139ADTR2G | HC | TSSOP-16 | $2500 /$ Tape \& Reel |
|  | 139A |  |  |
| MC74HC139ADTR2G-Q* $^{\text {M }}$ | HC | TSSOP-16 | $2500 /$ Tape \& Reel |
|  | 139A |  |  |

$\dagger$ For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

## MC74HC139A

## PACKAGE DIMENSIONS



SCALE 2:1


## QFN16, 2.5x3.5, 0.5P <br> CASE 485AW

ISSUE O
SCALE 2:1

DATE 11 DEC 2008

*For additional information on our $\mathrm{Pb}-$ Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOIC-16
CASE 751B-05
ISSUE K
SCALE 1:1


STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. EMITT
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 5:
PIN 1. DRAIN, DYE \#1
2. DRAIN, \#1
3. DRAIN, \#2
4. DRAIN, \#2
4. DRAIN, \#2
5. DRAIN, \#3
6. DRAIN, \#3 6. CATHODE
7. DRAIN, \#4 7. CATHODE
8. DRAIN, \#4
9. GATE, \#4
10. SOURCE, \#4
11. GATE, \#3
12. SOURCE, \#3
12. SOURCE, \#3
13. GATE, \#2
14. SOURCE, \#2
15. GATE, \#1
16. SOURCE, \#1

| STYLE 2: |  |
| ---: | :--- |
| PIN 1. | CATHODE |
| 2. | ANODE |
| 3. | NO CONNECTION |
| 4. | CATHODE |
| 5. | CATHODE |
| 6. | NO CONNECTION |
| 7. | ANODE |
| 8. | CATHODE |
| 9. | CATHODE |
| 10. | ANODE |
| 11. | NO CONNECTION |
| 12. | CATHODE |
| 13. | CATHODE |
| 14. | NO CONNECTION |
| 15. | ANODE |
| 16. | CATHODE |

PIN 1. CATHODE

STYLE 3:
PIN 1. COLLECTOR DYE
2. BASE,\#1
3. EMITTER, \#1
4. COLLECTOR \#1

STYLE 4:
PIN 1. COLLECTOR, DYE \#1
2. COLLECTOR,\#1
3. COLLECTOR, \#2 4. COLLECTOR, \#2 4. COLLECTOR, \#2 5. COLLECTOR, \#3 6. COLLECTOR, \#3 7. COLLECTOR, \#4 9. BASE, \#4
10. EMITTER, \#4
11. BASE, \#3
11. BASE, \#3
12. EMITTER, \#3
12. EMITTER, \#
13. BASE, \#2
14. EMITTER, \#2 R RECOMMENDED
15. BASE, \#1
16. EMITTER, \#1 8X

STYLE 6: STYLE 7:
PIN 1.
IN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
12. COMMON DR
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH


DIMENSIONS: MILLIMETERS
*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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| ---: | :--- | :--- | :--- |
| DESCRIPTION: | SOIC-16 | PAGE 1 OF 1 |  |

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TSSOP-16 WB
CASE 948F
ISSUE B
DATE 19 OCT 2006


1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 ( 0.006 ) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 ( 0.010 ) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL in EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE - $W$ -

| DIM | MILLIMETERS |  | INCHES |  |
| :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| c |  | 1.20 |  | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 | SC | 0.026 | BSC |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 | BC | 0.25 | BSC |
| M | $0^{\circ}$ | $8^{\circ}$ | $0^{\circ}$ | $8^{\circ}$ |



| GENERIC <br> MARKING DIAGRAM* |  |
| :---: | :---: |
|  |  |
| XXXX | = Specific Device Code |
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| G or - | = Pb-Free Package |

*This information is generic. Please refer to device data sheet for actual part marking. $\mathrm{Pb}-$ Free indicator, " G " or microdot " $\mathrm{\bullet}$ ", may or may not be present. Some products may not follow the Generic Marking.
*For additional information on our $\mathrm{Pb}-$ Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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| DESCRIPTION: | TSSOP-16 | PAGE 1 OF 1 |

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