

Quad 2-Input OR Gate

High-Performance Silicon-Gate CMOS

MC74HC32A, MC74HCT32A

The MC74HC32A/MC74HCT32A is identical in pinout to the LS32. The MC74HC32A device inputs are compatible with Standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. The MC74HCT32A inputs are compatible with Standard CMOS or TTL outputs.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V (HC), 4.5 to 5.5 V (HCT)
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7 A Requirements
- Chip Complexity: 48 FETs or 12 Equivalent Gates
- -Q suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

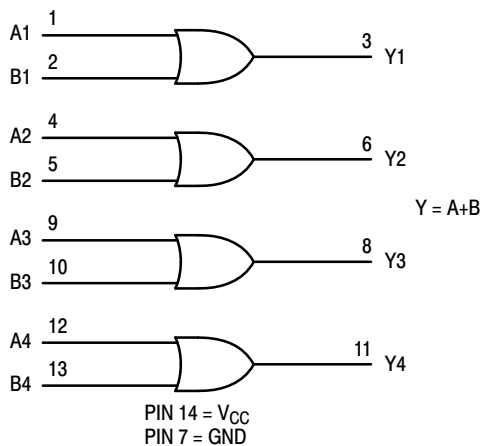


Figure 1. Logic Diagram

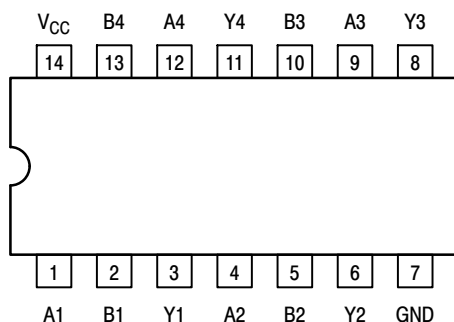
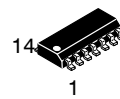
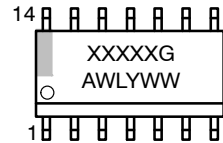


Figure 2. Pinout Diagram (Top View)

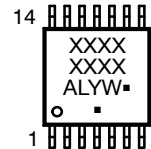
MARKING DIAGRAMS



SOIC-14
D SUFFIX
CASE 751A



TSSOP-14
DT SUFFIX
CASE 948G



XXXX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

| Inputs | | Output |
|--------|---|--------|
| A | B | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | H |

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

MC74HC32A, MC74HCT32A

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|------------------|--|--|------|
| V _{CC} | DC Supply Voltage | −0.5 to +6.5 | V |
| V _{IN} | DC Input Voltage | −0.5 to V _{CC} + 0.5 | V |
| V _{OUT} | DC Output Voltage | −0.5 to V _{CC} + 0.5 | V |
| I _{IN} | DC Input Current, per Pin | ±20 | mA |
| I _{OUT} | DC Output Current, per Pin | ±25 | mA |
| I _{CC} | DC Supply Current, V _{CC} and GND Pins | ±50 | mA |
| I _{IK} | Input Clamp Current (V _{IN} < 0 or V _{IN} > V _{CC}) | ±20 | mA |
| I _{OK} | Output Clamp Current (V _{OUT} < 0 or V _{OUT} > V _{CC}) | ±20 | mA |
| T _{STG} | Storage Temperature | −65 to +150 | °C |
| T _L | Lead Temperature, 1 mm from Case for 10 Seconds | 260 | °C |
| T _J | Junction Temperature Under Bias | ±150 | °C |
| θ _{JA} | Thermal Resistance (Note 1) | SOIC−14 TSSOP−14 116 150 | °C/W |
| P _D | Power Dissipation in Still Air at 25°C | SOIC−14 TSSOP−14 1077 833 | mW |
| MSL | Moisture Sensitivity | Level 1 | – |
| F _R | Flammability Rating | Oxygen Index: 28 to 34 UL 94 V−0 @ 0.125 in | – |
| V _{ESD} | ESD Withstand Voltage (Note 2) | Human Body Model Charged Device Model >2000 N/A | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76mm-by-114mm, 2-ounce copper trace no air flow per JESD51-7.

2. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|------------------------------------|--|--|--------------------|------|
| MC74HC | | | | |
| V _{CC} | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V |
| V _{IN} , V _{OUT} | DC Input Voltage, Output Voltage (Referenced to GND) (Note 3) | 0 | V _{CC} | V |
| T _A | Operating Free-Air Temperature | −55 | +125 | °C |
| t _r , t _f | Input Rise or Fall Time | V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V 0 0 0 | 1000 500 400 | ns |
| MC74HCT | | | | |
| V _{CC} | DC Supply Voltage (Referenced to GND) | 4.5 | 5.5 | V |
| V _{IN} , V _{OUT} | DC Input Voltage, DC Output Voltage (Referenced to GND) (Note 3) | 0 | V _{CC} | V |
| T _A | Operating Free-Air Temperature | −55 | +125 | °C |
| t _r , t _f | Input Rise or Fall Time | 0 | 500 | ns |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

MC74HC32A, MC74HCT32A

DC CHARACTERISTICS (MC74HC32A)

| Symbol | Parameter | Condition | V _{CC} V | Guaranteed Limit | | | Unit |
|-----------------|--|--|----------------------|------------------|-------|--------|------|
| | | | | -55 to 25°C | ≤85°C | ≤125°C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{out} = 0.1V or V _{CC} - 0.1V I _{out} ≤ 20μA | 2.0 | 1.50 | 1.50 | 1.50 | V |
| | | | 3.0 | 2.10 | 2.10 | 2.10 | |
| | | | 4.5 | 3.15 | 3.15 | 3.15 | |
| | | | 6.0 | 4.20 | 4.20 | 4.20 | |
| V _{IL} | Maximum Low-Level Input Voltage | V _{out} = 0.1V or V _{CC} - 0.1V I _{out} ≤ 20μA | 2.0 | 0.50 | 0.50 | 0.50 | V |
| | | | 3.0 | 0.90 | 0.90 | 0.90 | |
| | | | 4.5 | 1.35 | 1.35 | 1.35 | |
| | | | 6.0 | 1.80 | 1.80 | 1.80 | |
| V _{OH} | Minimum High-Level Output Voltage | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20μA | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | | 6.0 | 5.9 | 5.9 | 5.9 | |
| | | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4mA I _{out} ≤ 4.0mA I _{out} ≤ 5.2mA | 3.0 | 2.48 | 2.34 | 2.20 | |
| | | | 4.5 | 3.98 | 3.84 | 3.70 | |
| | | | 6.0 | 5.48 | 5.34 | 5.20 | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20μA | 2.0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5 | 0.1 | 0.1 | 0.1 | |
| | | | 6.0 | 0.1 | 0.1 | 0.1 | |
| | | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4mA I _{out} ≤ 4.0mA I _{out} ≤ 5.2mA | 3.0 | 0.26 | 0.33 | 0.40 | |
| | | | 4.5 | 0.26 | 0.33 | 0.40 | |
| | | | 6.0 | 0.26 | 0.33 | 0.40 | |
| I _{in} | Maximum Input Leakage Current | V _{in} = V _{CC} or GND | 6.0 | ±0.1 | ±1.0 | ±1.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{in} = V _{CC} or GND I _{out} = 0μA | 6.0 | 1.0 | 10 | 40 | μA |

AC CHARACTERISTICS (MC74HC32A)

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|--|---|----------------------|------------------|-------|--------|------|
| | | | −55 to 25°C | ≤85°C | ≤125°C | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, (A or B) to Y (Figures 3 and 4) | 2.0 | 75 | 95 | 110 | ns |
| | | 3.0 | 30 | 40 | 55 | |
| | | 4.5 | 15 | 19 | 22 | |
| | | 6.0 | 13 | 16 | 19 | |
| t _{TLH} , t _{THL} | Maximum Output Transition Time, Any Output (Figures 3 and 4) | 2.0 | 75 | 95 | 110 | ns |
| | | 3.0 | 27 | 32 | 36 | |
| | | 4.5 | 15 | 19 | 22 | |
| | | 6.0 | 13 | 16 | 19 | |
| C _{in} | Maximum Input Capacitance | | 10 | 10 | 10 | pF |

| | | | |
|-----------------|---|--|----|
| C _{PD} | Power Dissipation Capacitance (Per Buffer)* | Typical @ 25°C, V _{CC} = 5.0 V, V _{EE} = 0 V | pF |
| | | 20 | |

* Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}.

MC74HC32A, MC74HCT32A

DC CHARACTERISTICS (MC74HCT32A)

| Symbol | Parameter | Condition | V _{CC} V | Guaranteed Limit | | | Unit |
|-----------------|--|--|----------------------|------------------|------------|------------|------|
| | | | | -55 to 25°C | ≤85°C | ≤125°C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{out} = 0.1V or V _{CC} - 0.1V I _{out} ≤ 20μA | 4.5 to 5.5 | 2.0 | 2.0 | 2.0 | V |
| V _{IL} | Maximum Low-Level Input Voltage | V _{out} = 0.1V or V _{CC} - 0.1V I _{out} ≤ 20μA | 4.5 to 5.5 | 0.8 | 0.8 | 0.8 | V |
| V _{OH} | Minimum High-Level Output Voltage | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20μA | 4.5 5.5 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | V |
| | | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0mA | 4.5 | 3.98 | 3.84 | 3.70 | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20μA | 4.5 5.5 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | V |
| | | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0mA | 4.5 | 0.26 | 0.33 | 0.40 | |
| I _{in} | Maximum Input Leakage Current | V _{in} = V _{CC} or GND | 5.5 | ±0.1 | ±1.0 | ±1.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{in} = V _{CC} or GND I _{out} = 0μA | 5.5 | 1.0 | 10 | 40 | μA |

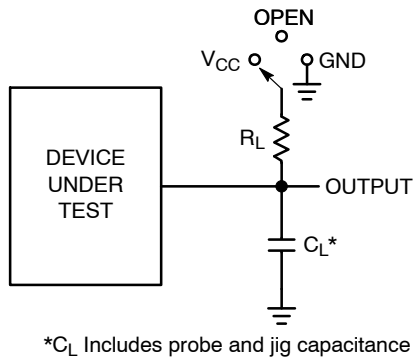
AC CHARACTERISTICS (MC74HCT32A)

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|--|---|----------------------|------------------|-------|--------|------|
| | | | -55 to 25°C | ≤85°C | ≤125°C | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, (A or B) to Y (Figures 3 and 4) | 5.0 | 15 | 19 | 22 | ns |
| t _{TLH} , t _{THL} | Maximum Output Transition Time, Any Output (Figures 3 and 4) | 5.0 | 15 | 19 | 22 | ns |
| C _{in} | Maximum Input Capacitance | | 10 | 10 | 10 | pF |

| C _{PD} | Power Dissipation Capacitance (Per Buffer)* | Typical @ 25°C, V _{CC} = 5.0 V, V _{EE} = 0 V | pF |
|-----------------|---|--|----|
| | | 20 | |

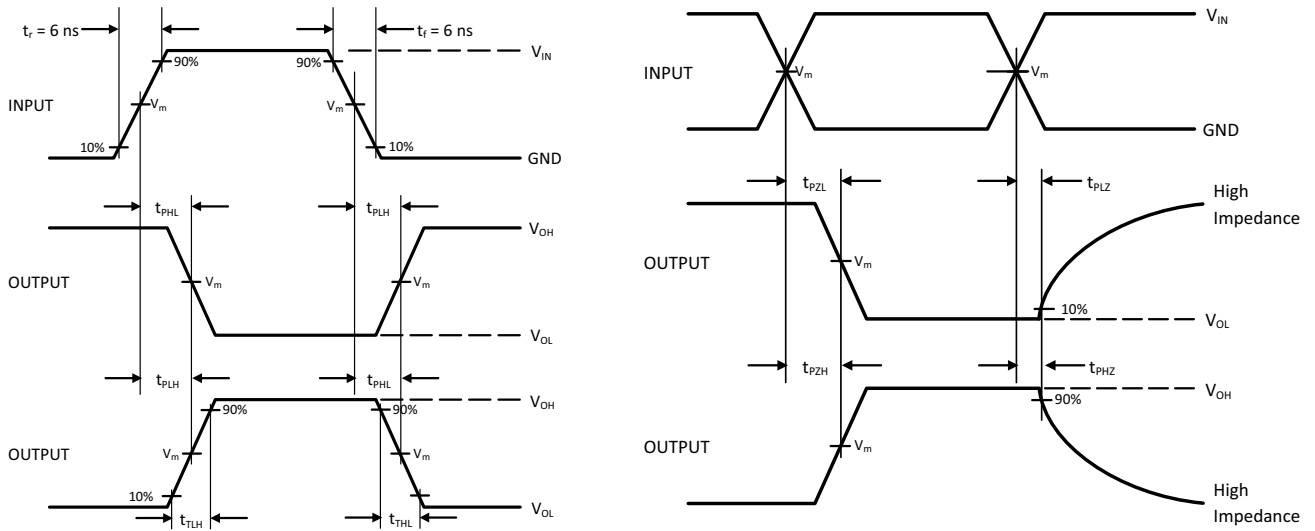
*Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}.

MC74HC32A, MC74HCT32A



| Test | Switch Position | C _L | R _L |
|-------------------------------------|-----------------|----------------|----------------|
| t _{PLH} / t _{PHL} | Open | 50 pF | 1 kΩ |
| t _{PLZ} / t _{PZL} | V _{CC} | | |
| t _{PHZ} / t _{PZH} | GND | | |

Figure 3. Test Circuit



| Device | V _{IN} , V | V _m , V |
|------------|---------------------|-----------------------|
| MC74HC32A | V _{CC} | 50% × V _{CC} |
| MC74HCT32A | 3 V | 1.3 V |

Figure 4. Switching Waveforms

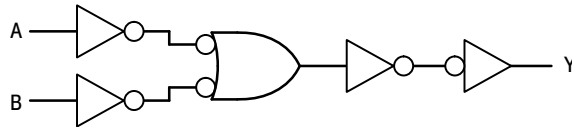


Figure 5. Expanded Logic Diagram
(1/4 of the Device)

MC74HC32A, MC74HCT32A

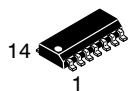
ORDERING INFORMATION

| Device | Package | Marking | Shipping [†] |
|-------------------|----------|------------|-----------------------|
| MC74HC32ADG | SOIC-14 | HC32A | 55 Units / Rail |
| MC74HC32ADG-Q* | SOIC-14 | HC32A | 55 Units / Rail |
| MC74HC32ADR2G | SOIC-14 | HC32A | 2500 / Tape & Reel |
| MC74HC32ADR2G-Q* | SOIC-14 | HC32A | 2500 / Tape & Reel |
| MC74HC32ADTR2G | TSSOP-14 | HC 32A | 2500 / Tape & Reel |
| MC74HC32ADTR2G-Q* | TSSOP-14 | HC 32A | 2500 / Tape & Reel |
| MC74HCT32ADR2G | SOIC-14 | HCT32A | 2500 / Tape & Reel |
| MC74HCT32ADTR2G | TSSOP-14 | HCT 32A | 2500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

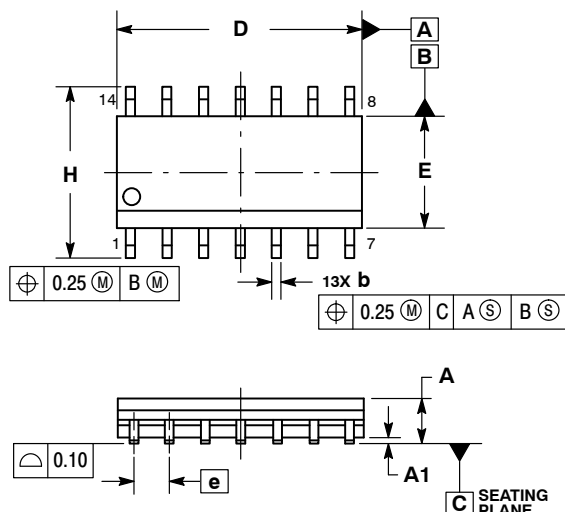
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-14 NB
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

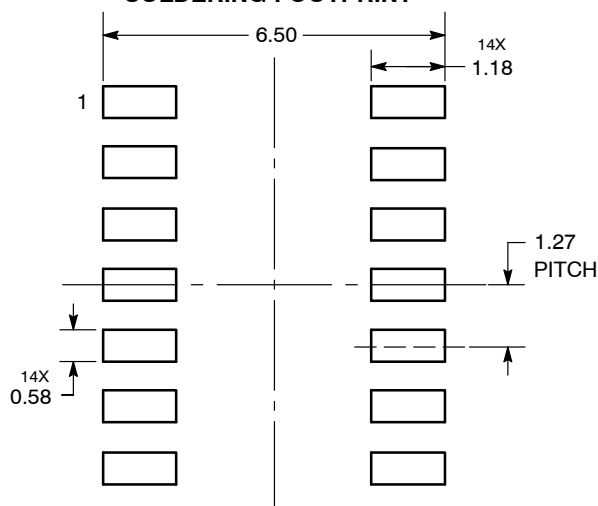


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.054 | 0.068 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |
| b | 0.35 | 0.49 | 0.014 | 0.019 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.019 |
| L | 0.40 | 1.25 | 0.016 | 0.049 |
| M | 0° | 7° | 0° | 7° |

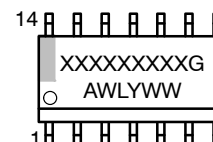
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC-14
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

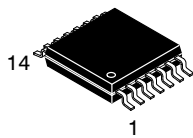
STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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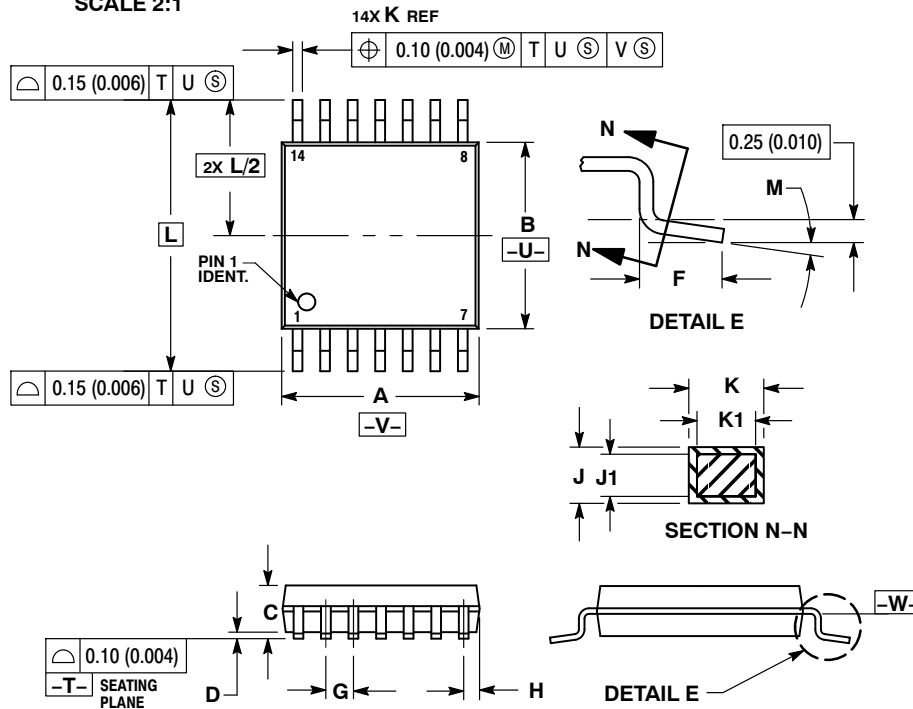
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TSSOP-14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016

SCALE 2:1

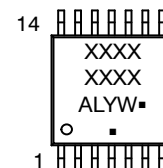


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

GENERIC MARKING DIAGRAM*

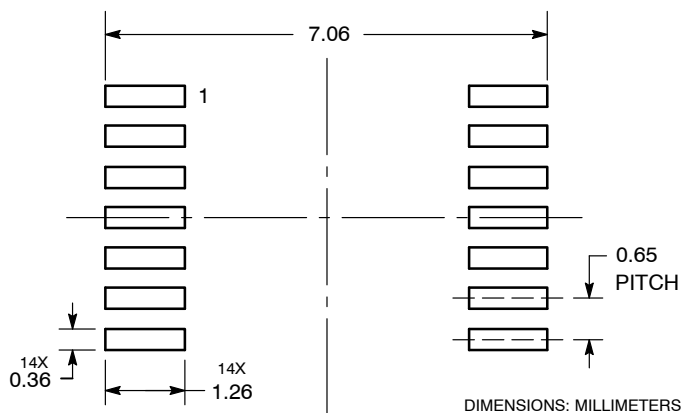


- A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT



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DESCRIPTION: TSSOP-14 WB

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