DATA SHEET
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Analog Multiplexer/ Demultiplexer

High−Performance Silicon−Gate CMOS

MC74LVX8051

The MC74LVX8051 utilizes silicon−gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. This analog multiplexer/demultiplexer controls analog voltages that may vary across the complete power supply range (from V_{CC} to GND).

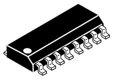
The LVX8051 is similar in pinout to the high−speed HC4051A and the metal−gate MC14051B. The Channel−Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

The Channel−Select and Enable inputs are compatible with standard CMOS outputs; with pull−up resistors they are compatible with LSTTL outputs.

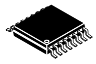
This device has been designed so that the ON resistance (R_{on}) is more linear over input voltage than R_{on} of metal−gate CMOS analog switches.

Features

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range (V_{CC} − GND) = 2.5 to 6.0 V
- Digital (Control) Power Supply Range (V_{CC} − GND) = 2.5 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal−Gate Counterparts
- Low Noise
- In Compliance With the Requirements of JEDEC Standard No. 7A
- Chip Complexity: LVX8051 − 184 FETs or 46 Equivalent Gates
- These Devices are Pb−Free and are RoHS Compliant

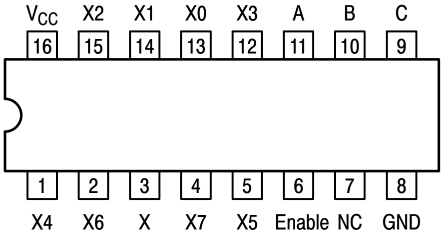


SOIC−16
D SUFFIX
CASE 751B

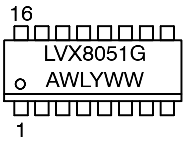


TSSOP−16
DT SUFFIX
CASE 948F

PIN ASSIGNMENT



MARKING DIAGRAMS



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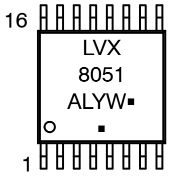


TSSOP−16

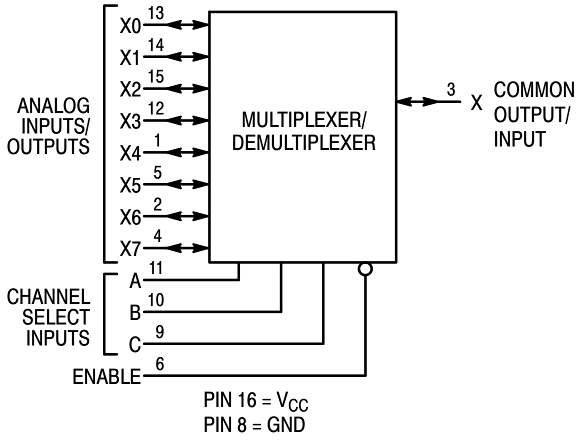
LVX8051 = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

December, 2024 − Rev. 7



LOGIC DIAGRAM
MC74LVX8051
Single−Pole, 8−Position Plus Common Off

FUNCTION TABLE − MC74LVX8051

Control Inputs				
	Select			
Enable	**C**	**B**	**A**	**ON Channels**
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	NONE

X = Don’t Care

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	–0.5 to +7.0	V
V_{IS}	Analog Input Voltage	−0.5 to V_{CC} + 0.5	V
V_{in}	Digital Input Voltage (Referenced to GND)	–0.5 to V_{CC} + 0.5	V
I	DC Current, Into or Out of Any Pin	±20	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature Range	–65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: –7 mW/°C from 65° to 125°C
TSSOP Package: –6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	2.5	6.0	V
V_{IS}	Analog Input Voltage	0.0	V_{CC}	V
V_{in}	Digital Input Voltage (Referenced to GND)	GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch		1.2	V
T_A	Operating Temperature Range, All Package Types	– 55	+ 85	°C
t_r, t_f	Input Rise/Fall Time (Channel Select or Enable Inputs) V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	 0 0	 100 20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

*For voltage drops across switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC CHARACTERISTICS — Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	2.5 3.0 4.5 5.5	1.50 2.10 3.15 3.85	1.50 2.10 3.15 3.85	1.50 2.10 3.15 3.85	V
V_{IL}	Maximum Low–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	2.5 3.0 4.5 5.5	0.5 0.9 1.35 1.65	0.5 0.9 1.35 1.65	0.5 0.9 1.35 1.65	V
I_{in}	Maximum Input Leakage Current, Channel–Select or Enable Inputs	$V_{in} = V_{CC}$ or GND	5.5	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select, Enable and $V_{IS} = V_{CC}$ or GND; $V_{IO} = 0$ V	5.5	4.0	40	160	μA

DC ELECTRICAL CHARACTERISTICS (Analog Section)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
R_{on}	Maximum "ON" Resistance	$V_{in} = V_{IL}$ or V_{IH} $V_{IS} = V_{CC}$ to GND $\lvert I_S\rvert \leq 10.0$ mA (Figures 1, 2)	3.0 4.5 5.5	40 30 25	45 32 28	50 37 30	Ω
		$V_{in} = V_{IL}$ or V_{IH} $V_{IS} = V_{CC}$ or GND (Endpoints) $\lvert I_S\rvert \leq 10.0$ mA (Figures 1, 2)	3.0 4.5 5.5	30 25 20	35 28 25	40 35 30	
ΔR_{on}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	$V_{in} = V_{IL}$ or V_{IH} $V_{IS} = 1/2\ (V_{CC} - \text{GND})$ $\lvert I_S\rvert \leq 10.0$ mA	3.0 4.5 5.5	15 8.0 8.0	20 12 12	25 15 15	Ω
I_{off}	Maximum Off–Channel Leakage Current, Any One Channel	$V_{in} = V_{IL}$ or V_{IH}; $V_{IO} = V_{CC}$ or GND; Switch Off (Figure 3)	5.5	0.1	0.5	1.0	μA
	Maximum Off–Channel Leakage Current, Common Channel	$V_{in} = V_{IL}$ or V_{IH}; $V_{IO} = V_{CC}$ or GND; Switch Off (Figure 4)	5.5	0.2	2.0	4.0	
I_{on}	Maximum On–Channel Leakage Current, Channel–to–Channel	$V_{in} = V_{IL}$ or V_{IH}; Switch–to–Switch = V_{CC} or GND; (Figure 5)	5.5	0.2	2.0	4.0	μA

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 3 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Channel–Select to Analog Output (Figure 9)	2.5	30	35	40	ns
		3.0	20	25	30	
		4.5	15	18	22	
		5.5	15	18	20	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figure 10)	2.5	4.0	6.0	8.0	ns
		3.0	3.0	5.0	6.0	
		4.5	1.0	2.0	2.0	
		5.5	1.0	2.0	2.0	
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.5	30	35	40	ns
		3.0	20	25	30	
		4.5	15	18	22	
		5.5	15	18	20	
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.5	20	25	30	ns
		3.0	12	14	15	
		4.5	8.0	10	12	
		5.5	8.0	10	12	
C_{in}	Maximum Input Capacitance, Channel–Select or Enable Inputs		10	10	10	pF
$C_{I/O}$	Maximum Capacitance Analog I/O		35	35	35	pF
	(All Switches Off) Common O/I		130	130	130	
	Feedthrough		1.0	1.0	1.0	

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Figure 13)*	45	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Condition	V_{CC} V	Limit* 25°C	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 6)	f_{in} = 1MHz Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{OS}; Increase f_{in} Frequency Until dB Meter Reads –3 dB; R_L = 50 Ω, C_L = 10 pF	3.0	80	MHz
			4.5	80	
			5.5	80	
–	Off–Channel Feedthrough Isolation (Figure 7)	f_{in} = Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{IS}	3.0	–50	dB
			4.5	–50	
		f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	5.5	–50	
			3.0	–37	
			4.5	–37	
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	5.5	–37	
–	Feedthrough Noise. Channel–Select Input to Common I/O (Figure 8)	V_{in} ≤ 1MHz Square Wave ($t_r = t_f$ = 6ns); Adjust R_L at Setup so that I_S = 0 A;	3.0	25	mV$_{PP}$
			4.5	105	
		Enable = GND R_L = 600 Ω, C_L = 50 pF	5.5	135	
			3.0	35	
			4.5	145	
		R_L = 10 kΩ, C_L = 10 pF	5.5	190	
THD	Total Harmonic Distortion (Figure 14)	f_{in} = 1 kHz, R_L = 10 kΩ, C_L = 50 pF THD = $THD_{measured} - THD_{source}$			%
		V_{IS} = 2.0 V_{PP} sine wave	3.0	0.10	
		V_{IS} = 4.0 V_{PP} sine wave	4.5	0.08	
		V_{IS} = 5.0 V_{PP} sine wave	5.5	0.05	

*Limits not tested. Determined by design and verified by qualification.

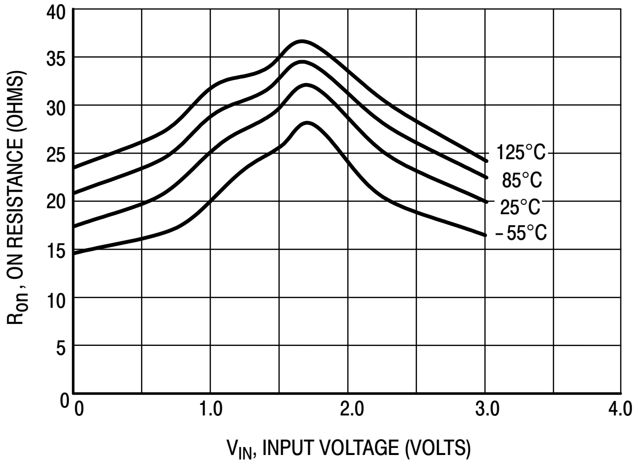


Figure 1a. Typical On Resistance, V_{CC} = 3.0 V

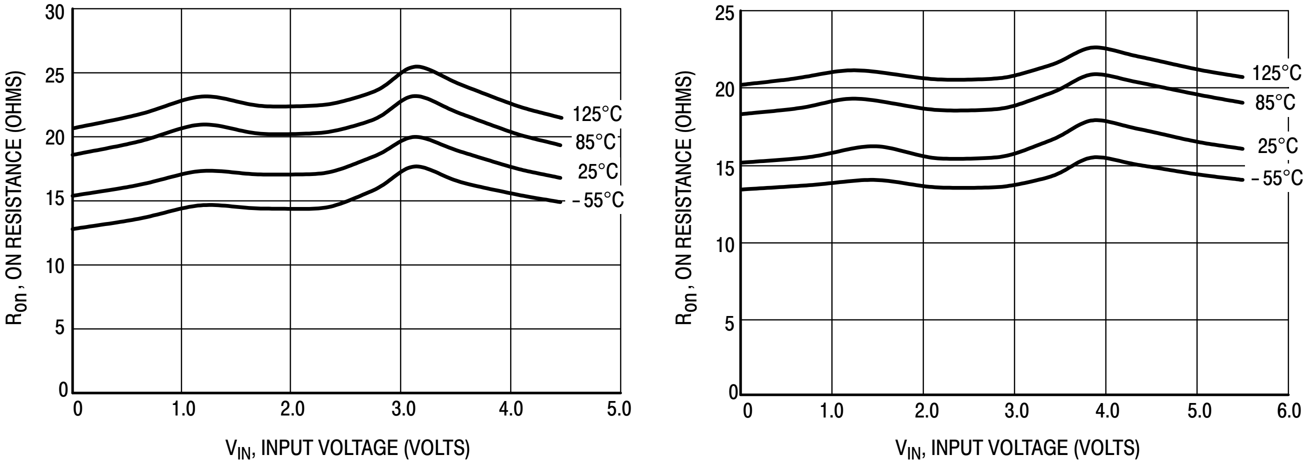


Figure 1b. Typical On Resistance, V_{CC} = 4.5 V

Figure 1c. Typical On Resistance, V_{CC} = 5.5 V

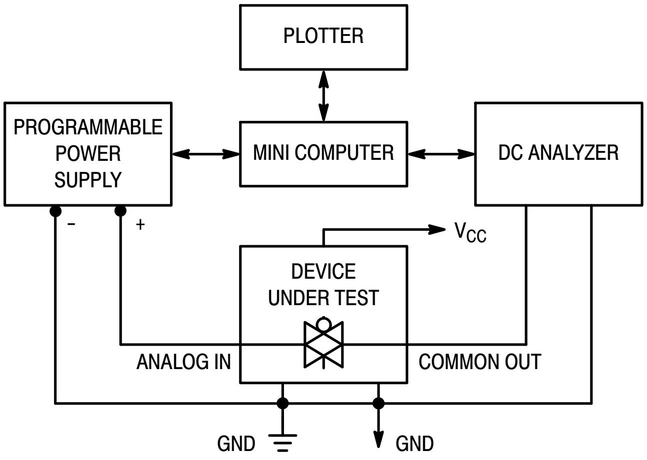


Figure 2. On Resistance Test Set–Up

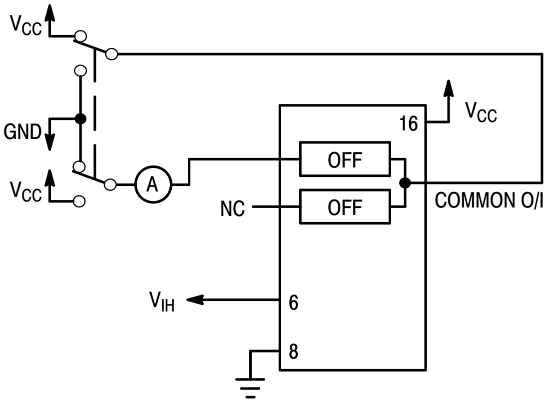


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set−Up

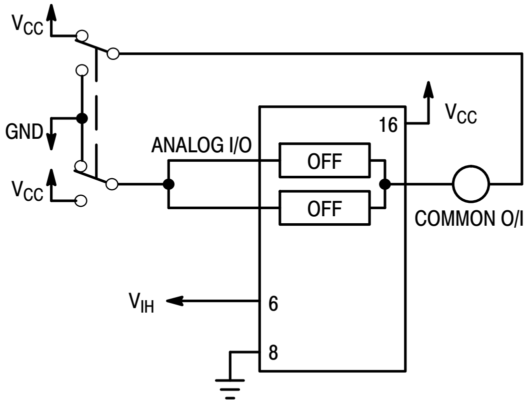


Figure 4. Maximum Off Channel Leakage Current, Common Channel, Test Set−Up

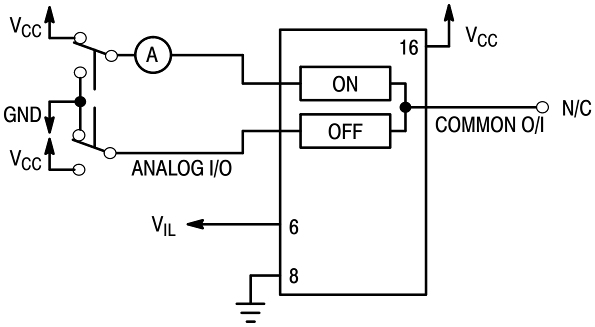
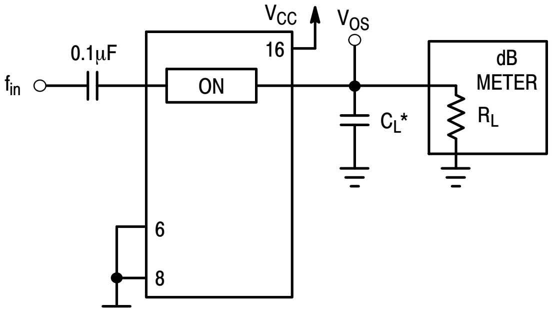
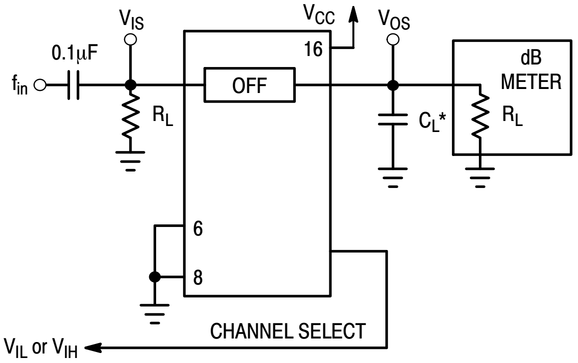


Figure 5. Maximum On Channel Leakage Current, Channel to Channel, Test Set−Up



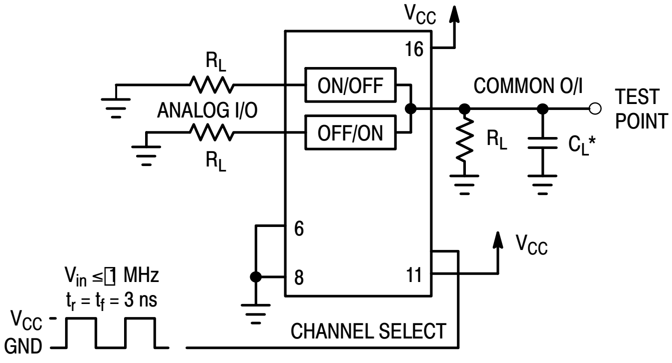
*Includes all probe and jig capacitance

Figure 6. Maximum On Channel Bandwidth, Test Set−Up



*Includes all probe and jig capacitance

Figure 7. Off Channel Feedthrough Isolation, Test Set−Up



*Includes all probe and jig capacitance

Figure 8. Feedthrough Noise, Channel Select to Common Out, Test Set−Up

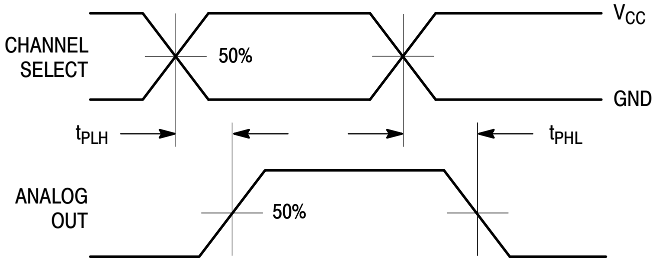
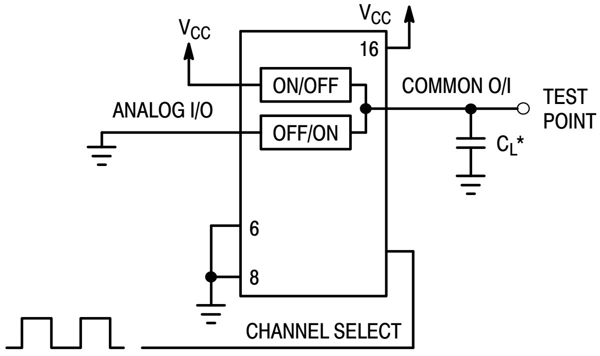


Figure 9a. Propagation Delays, Channel Select to Analog Out



*Includes all probe and jig capacitance

Figure 9b. Propagation Delay, Test Set−Up Channel Select to Analog Out

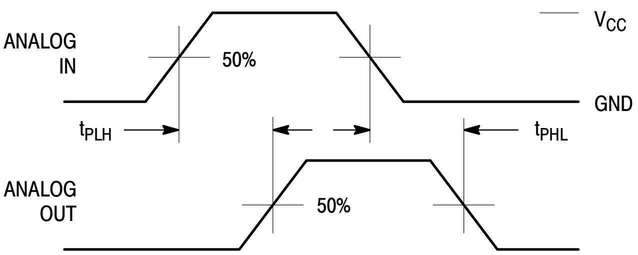
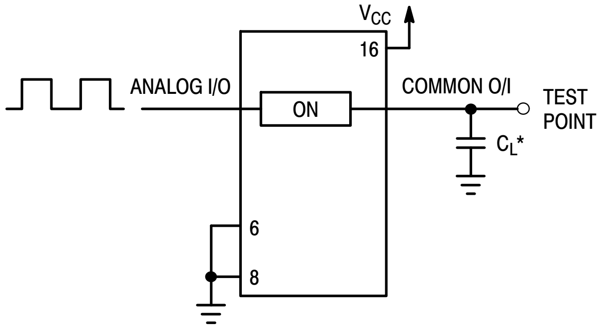


Figure 10a. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance

Figure 10b. Propagation Delay, Test Set−Up Analog In to Analog Out

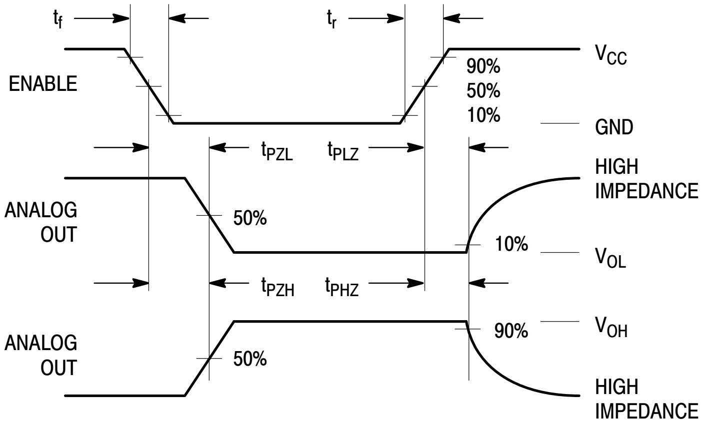


Figure 11a. Propagation Delays, Enable to Analog Out

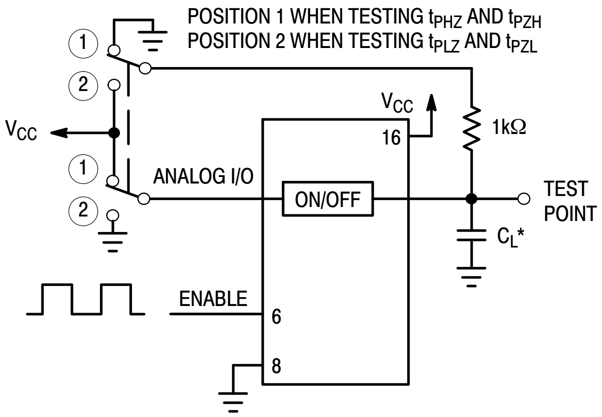
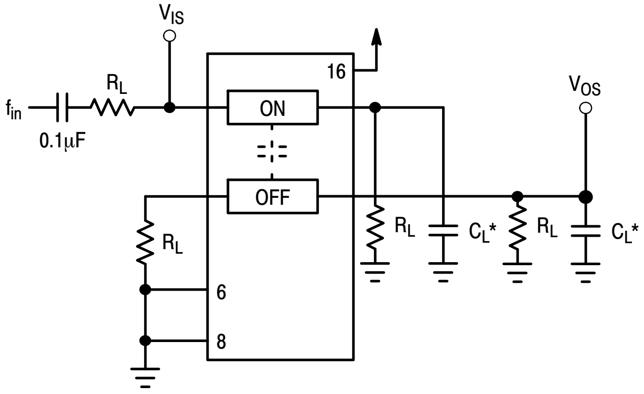


Figure 11b. Propagation Delay, Test Set−Up Enable to Analog Out



*Includes all probe and jig capacitance

Figure 12. Crosstalk Between Any Two Switches, Test Set−Up

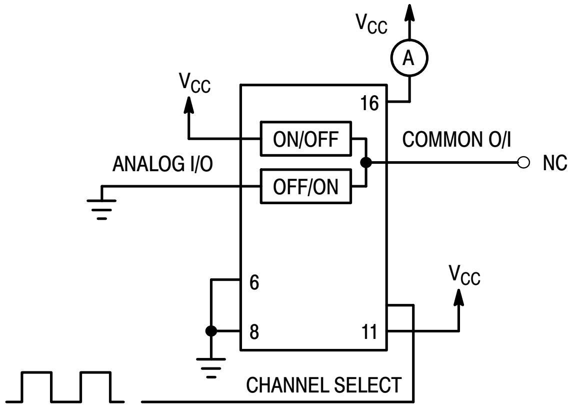
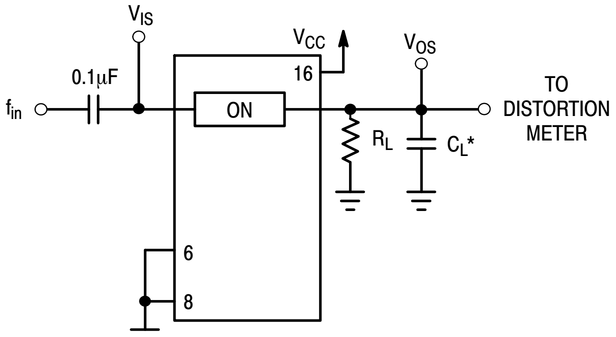


Figure 13. Power Dissipation Capacitance, Test Set−Up



*Includes all probe and jig capacitance

Figure 14a. Total Harmonic Distortion, Test Set−Up

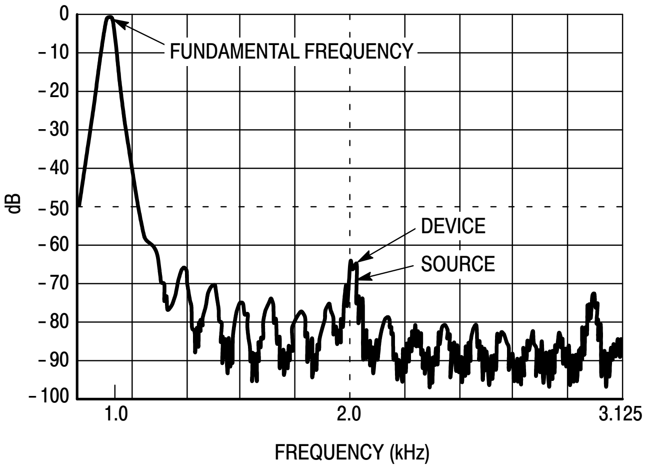


Figure 14b. Plot, Harmonic Distortion

APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at V_{CC} or GND logic levels. V_{CC} being recognized as a logic high and GND being recognized as a logic low. In this example:

V_{CC} = +5V = logic high
GND = 0V = logic low

The maximum analog voltage swing is determined by the supply voltage V_{CC}. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below GND. In this example, the difference between V_{CC} and GND is five volts. Therefore, using the configuration of Figure 15, a maximum analog signal of five volts peak−to−peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and outputs to V_{CC} or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

V_{CC} − GND = 2 to 6 volts

When voltage transients above V_{CC} and/or below GND are anticipated on the analog channels, external Germanium or Schottky diodes (D_x) are recommended as shown in Figure 16. These diodes should be able to absorb the maximum anticipated current surges during clipping.

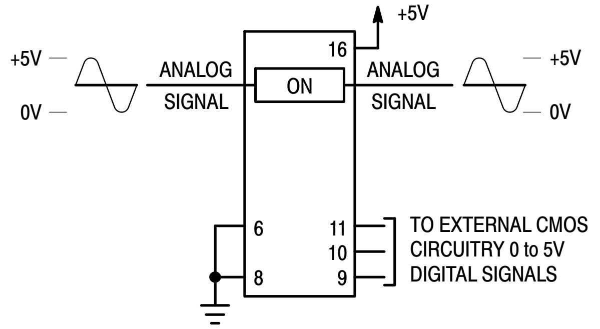


Figure 15. Application Example

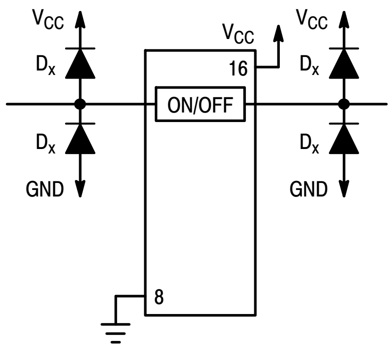
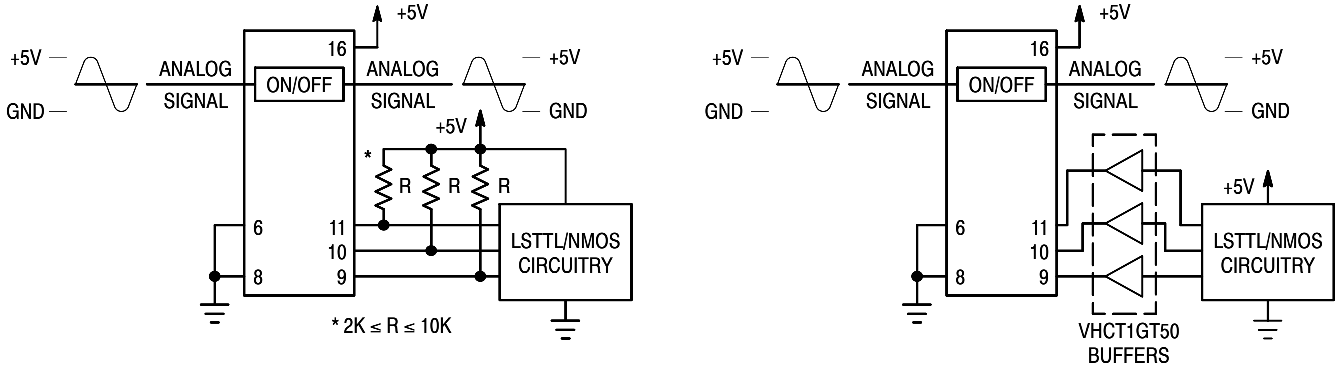


Figure 16. External Germanium or Schottky Clipping Diodes



a. Using Pull−Up Resistors

b. Using HCT Interface

Figure 17. Interfacing LSTTL/NMOS to CMOS Inputs

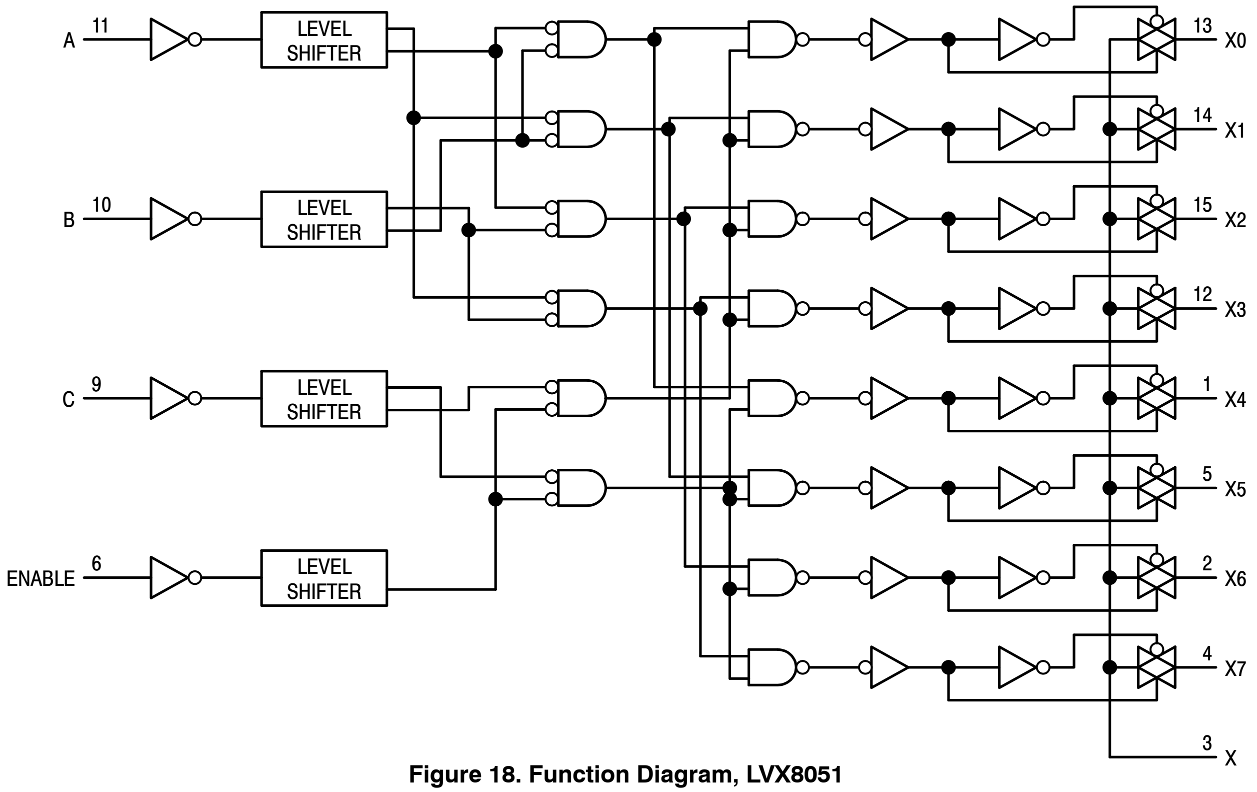


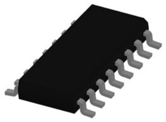
Figure 18. Function Diagram, LVX8051

ORDERING INFORMATION

Device	Package	Shipping†
MC74LVX8051DR2G	SOIC−16 (Pb−Free)	2500 Tape & Reel
MC74LVX8051DTG	TSSOP−16 (Pb−Free)	96 Units / Rail
MC74LVX8051DTR2G	TSSOP−16 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

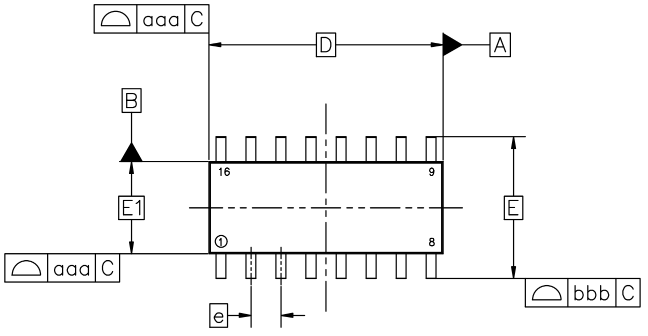
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



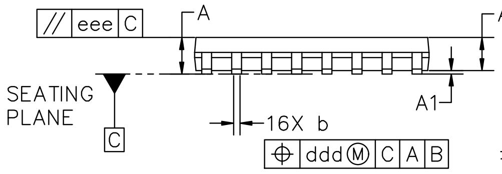
SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

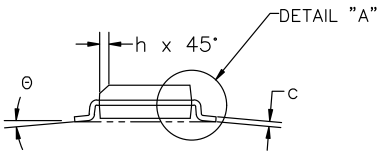
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



TOP VIEW

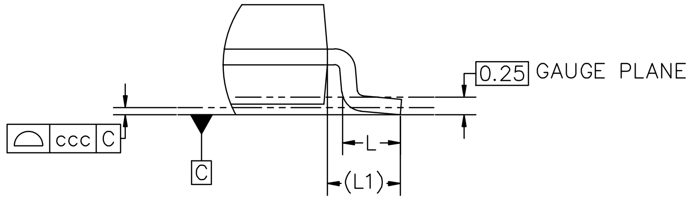


SIDE VIEW

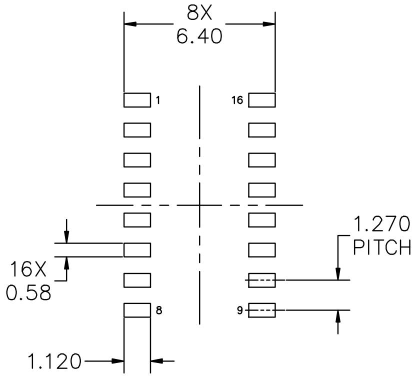


END VIEW

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



DETAIL "A"
Scale 3:1



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

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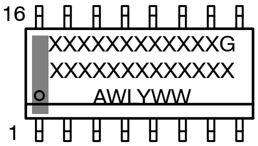
DESCRIPTION:	**SOIC−16 9.90X3.90X1.37 1.27P**	**PAGE 1 OF 2**

SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

PIN 1.	COLLECTOR
2.	BASE
3.	EMITTER
4.	NO CONNECTION
5.	EMITTER
6.	BASE
7.	COLLECTOR
8.	COLLECTOR
9.	BASE
10.	EMITTER
11.	NO CONNECTION
12.	EMITTER
13.	BASE
14.	COLLECTOR
15.	EMITTER
16.	COLLECTOR

STYLE 2:

PIN 1.	CATHODE
2.	ANODE
3.	NO CONNECTION
4.	CATHODE
5.	CATHODE
6.	NO CONNECTION
7.	ANODE
8.	CATHODE
9.	CATHODE
10.	ANODE
11.	NO CONNECTION
12.	CATHODE
13.	CATHODE
14.	NO CONNECTION
15.	ANODE
16.	CATHODE

STYLE 3:

PIN 1.	COLLECTOR, DYE #1
2.	BASE, #1
3.	EMITTER, #1
4.	COLLECTOR, #1
5.	COLLECTOR, #2
6.	BASE, #2
7.	EMITTER, #2
8.	COLLECTOR, #2
9.	COLLECTOR, #3
10.	BASE, #3
11.	EMITTER, #3
12.	COLLECTOR, #3
13.	COLLECTOR, #4
14.	BASE, #4
15.	EMITTER, #4
16.	COLLECTOR, #4

STYLE 4:

PIN 1.	COLLECTOR, DYE #1
2.	COLLECTOR, #1
3.	COLLECTOR, #2
4.	COLLECTOR, #2
5.	COLLECTOR, #3
6.	COLLECTOR, #3
7.	COLLECTOR, #4
8.	COLLECTOR, #4
9.	BASE, #4
10.	EMITTER, #4
11.	BASE, #3
12.	EMITTER, #3
13.	BASE, #2
14.	EMITTER, #2
15.	BASE, #1
16.	EMITTER, #1

STYLE 5:

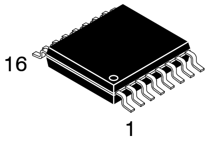
PIN 1.	DRAIN, DYE #1
2.	DRAIN, #1
3.	DRAIN, #2
4.	DRAIN, #2
5.	DRAIN, #3
6.	DRAIN, #3
7.	DRAIN, #4
8.	DRAIN, #4
9.	GATE, #4
10.	SOURCE, #4
11.	GATE, #3
12.	SOURCE, #3
13.	GATE, #2
14.	SOURCE, #2
15.	GATE, #1
16.	SOURCE, #1

STYLE 6:

PIN 1.	CATHODE
2.	CATHODE
3.	CATHODE
4.	CATHODE
5.	CATHODE
6.	CATHODE
7.	CATHODE
8.	CATHODE
9.	ANODE
10.	ANODE
11.	ANODE
12.	ANODE
13.	ANODE
14.	ANODE
15.	ANODE
16.	ANODE

STYLE 7:

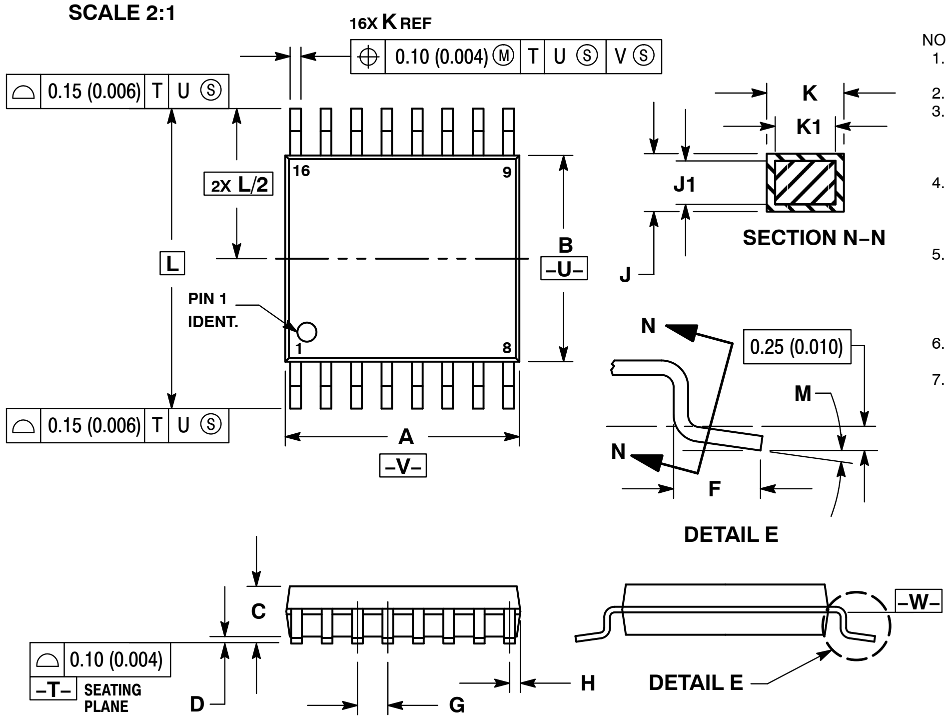
PIN 1.	SOURCE N-CH
2.	COMMON DRAIN (OUTPUT)
3.	COMMON DRAIN (OUTPUT)
4.	GATE P-CH
5.	COMMON DRAIN (OUTPUT)
6.	COMMON DRAIN (OUTPUT)
7.	COMMON DRAIN (OUTPUT)
8.	SOURCE P-CH
9.	SOURCE P-CH
10.	COMMON DRAIN (OUTPUT)
11.	COMMON DRAIN (OUTPUT)
12.	COMMON DRAIN (OUTPUT)
13.	GATE N-CH
14.	COMMON DRAIN (OUTPUT)
15.	COMMON DRAIN (OUTPUT)
16.	SOURCE N-CH



SCALE 2:1

TSSOP−16 WB
CASE 948F
ISSUE B

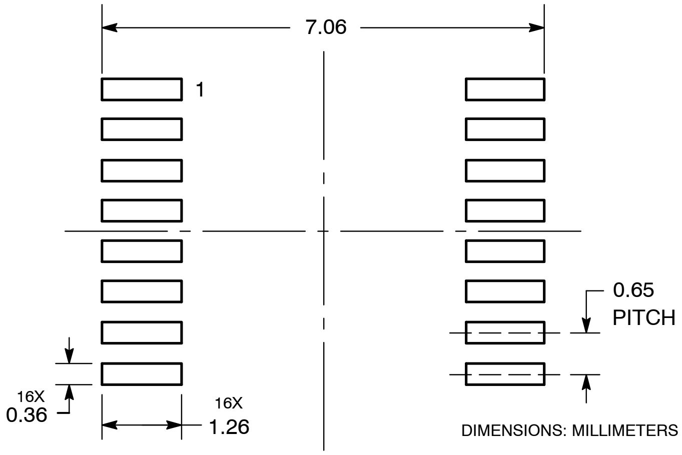
DATE 19 OCT 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

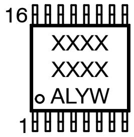
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	TSSOP−16	PAGE 1 OF 1

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