

MJ11015 (PNP); MJ11012, MJ11016 (NPN)

MJ11016 is a Preferred Device

High-Current Complementary Silicon Transistors

... for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain –
 $h_{FE} = 1000$ (Min) @ $I_C = 20$ Adc
- Monolithic Construction with Built-in Base Emitter Shunt Resistor
- Junction Temperature to $+200^\circ\text{C}$

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--|----------------|-------------|--------------------------|
| Collector-Emitter Voltage MJ11012 MJ11015/6 | V_{CEO} | 60 120 | Vdc |
| Collector-Base Voltage MJ11012 MJ11015/6 | V_{CB} | 60 120 | Vdc |
| Emitter-Base Voltage | V_{EB} | 5 | Vdc |
| Collector Current | I_C | 30 | Adc |
| Base Current | I_B | 1 | Adc |
| Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C @ $T_C = 100^\circ\text{C}$ | P_D | 200 1.15 | W W/ $^\circ\text{C}$ |
| Operating Storage Junction Temperature Range | T_J, T_{stg} | -55 to +200 | $^\circ\text{C}$ |

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|-----------------|------|---------------------------|
| Thermal Resistance, Junction-to-Case | $R_{\theta JC}$ | 0.87 | $^\circ\text{C}/\text{W}$ |
| Maximum Lead Temperature for Soldering Purposes for ≤ 10 Seconds | T_L | 275 | $^\circ\text{C}$ |

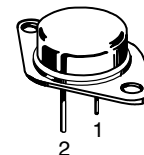
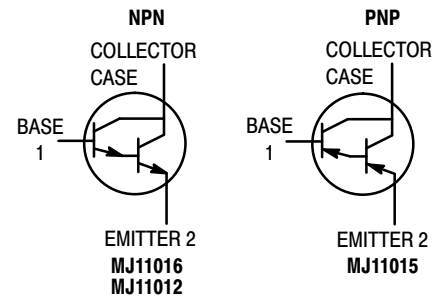
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.



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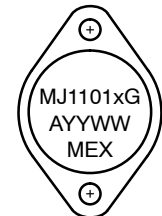
<http://onsemi.com>

30 AMPERE DARLINGTON POWER TRANSISTORS COMPLEMENTARY SILICON 60 – 120 VOLTS, 200 WATTS



TO-204AA (TO-3)
CASE 1-07
STYLE 1

MARKING DIAGRAM



- MJ1101x = Device Code
x = 2, 5 or 6
- G = Pb-Free Package
- A = Location Code
- YY = Year
- WW = Work Week
- MEX = Country of Origin

ORDERING INFORMATION

| Device | Package | Shipping |
|----------|-------------------|----------------|
| MJ11012 | TO-3 | 100 Units/Tray |
| MJ11012G | TO-3 (Pb-Free) | 100 Units/Tray |
| MJ11015 | TO-3 | 100 Units/Tray |
| MJ11015G | TO-3 (Pb-Free) | 100 Units/Tray |
| MJ11016 | TO-3 | 100 Units/Tray |
| MJ11016G | TO-3 (Pb-Free) | 100 Units/Tray |

Preferred devices are recommended choices for future use and best overall value.

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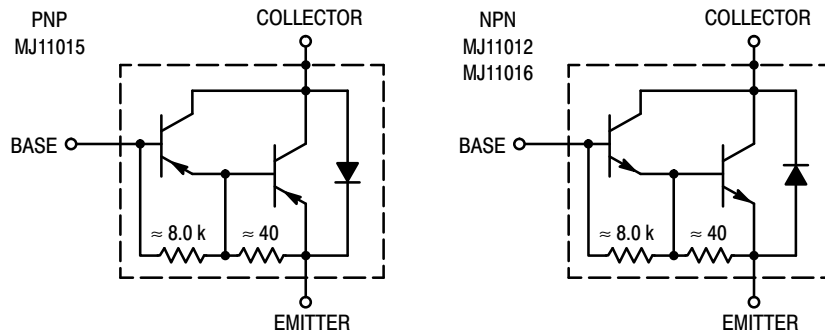


Figure 1. Darlington Circuit Schematic

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

| Characteristics | Symbol | Min | Max | Unit |
|---|---------------|------------------|------------------|------|
| OFF CHARACTERISTICS | | | | |
| Collector–Emitter Breakdown Voltage(1) ($I_C = 100\text{ mA}$, $I_B = 0$) | $V_{(BR)CEO}$ | 60 120 | – – | Vdc |
| Collector–Emitter Leakage Current ($V_{CE} = 60\text{ Vdc}$, $R_{BE} = 1\text{ k ohm}$) ($V_{CE} = 120\text{ Vdc}$, $R_{BE} = 1\text{ k ohm}$) ($V_{CE} = 60\text{ Vdc}$, $R_{BE} = 1\text{ k ohm}$, $T_C = 150^\circ\text{C}$) ($V_{CE} = 120\text{ Vdc}$, $R_{BE} = 1\text{ k ohm}$, $T_C = 150^\circ\text{C}$) | I_{CER} | – – – – | 1 1 5 5 | mAdc |
| Emitter Cutoff Current ($V_{BE} = 5\text{ Vdc}$, $I_C = 0$) | I_{EBO} | – | 5 | mAdc |
| Collector–Emitter Leakage Current ($V_{CE} = 50\text{ Vdc}$, $I_B = 0$) | I_{CEO} | – | 1 | mAdc |
| ON CHARACTERISTICS(1) | | | | |
| DC Current Gain ($I_C = 20\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$) ($I_C = 30\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$) | h_{FE} | 1000 200 | – – | – |
| Collector–Emitter Saturation Voltage ($I_C = 20\text{ Adc}$, $I_B = 200\text{ mAdc}$) ($I_C = 30\text{ Adc}$, $I_B = 300\text{ mAdc}$) | $V_{CE(sat)}$ | – – | 3 4 | Vdc |
| Base–Emitter Saturation Voltage ($I_C = 20\text{ A}$, $I_B = 200\text{ mAdc}$) ($I_C = 30\text{ A}$, $I_B = 300\text{ mAdc}$) | $V_{BE(sat)}$ | – – | 3.5 5 | Vdc |
| DYNAMIC CHARACTERISTICS | | | | |
| Current–Gain Bandwidth Product ($I_C = 10\text{ A}$, $V_{CE} = 3\text{ Vdc}$, $f = 1\text{ MHz}$) | h_{fe} | 4 | – | MHz |

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2.0\%$.

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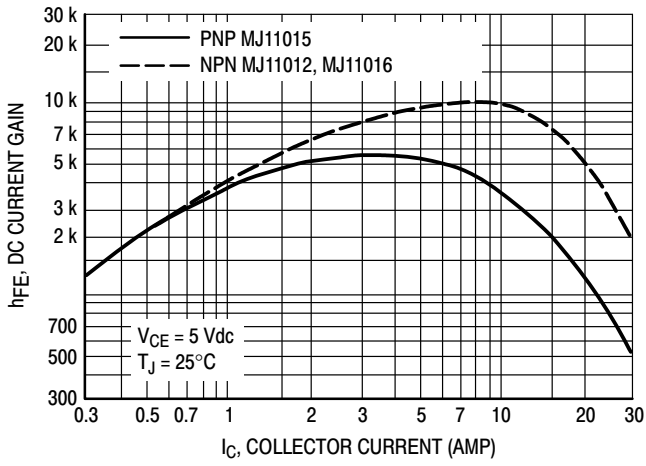


Figure 2. DC Current Gain (1)

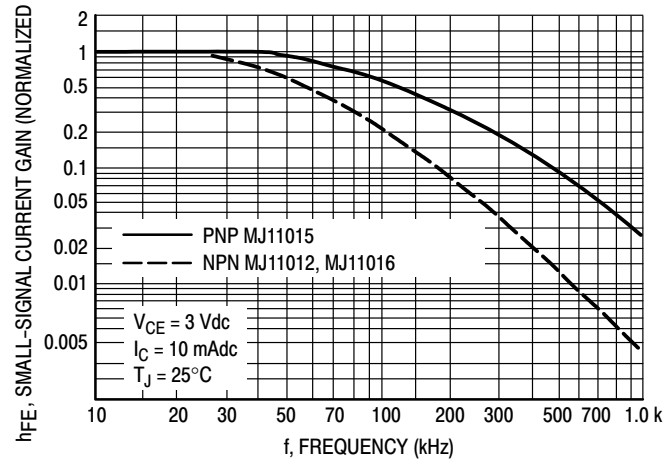


Figure 3. Small-Signal Current Gain

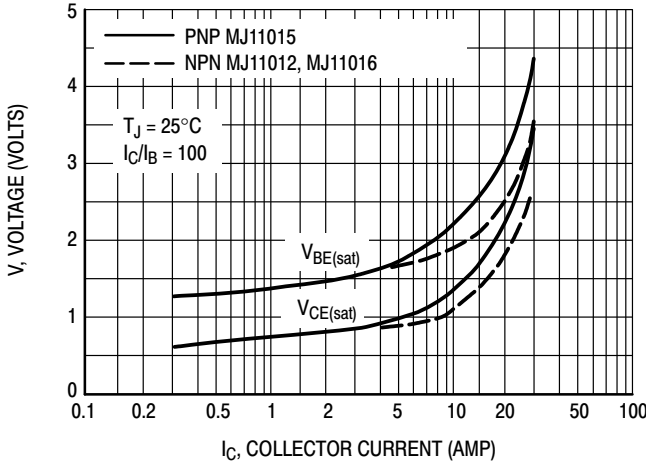


Figure 4. "On" Voltages (1)

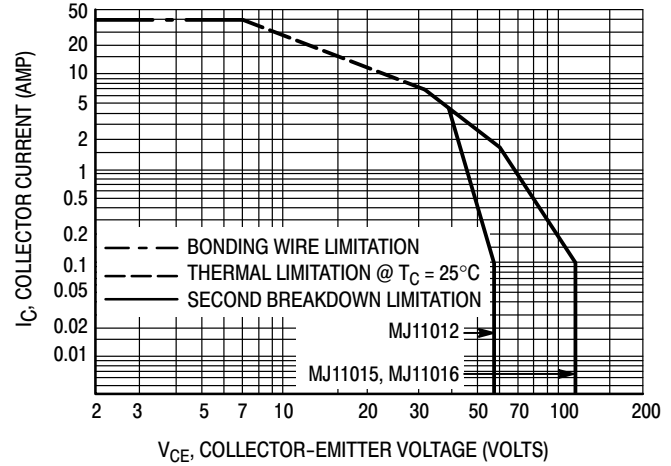


Figure 5. Active Region DC Safe Operating Area

There are two limitations on the power handling ability of a transistor average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operations e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

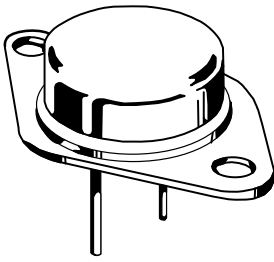
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor

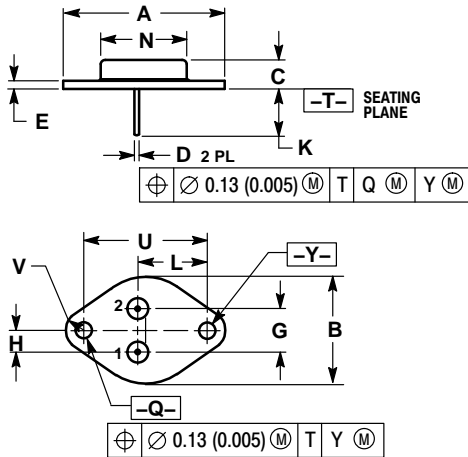


TO-204 (TO-3)
CASE 1-07
ISSUE Z

DATE 05/18/1988



SCALE 1:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-----------|-------------|-----------|
| | MIN | MAX | MIN | MAX |
| A | 1.550 REF | --- | 39.37 REF | --- |
| B | --- | 1.050 | --- | 26.67 |
| C | 0.250 | 0.335 | 6.35 | 8.51 |
| D | 0.038 | 0.043 | 0.97 | 1.09 |
| E | 0.055 | 0.070 | 1.40 | 1.77 |
| G | 0.430 BSC | --- | 10.92 BSC | --- |
| H | 0.215 BSC | --- | 5.46 BSC | --- |
| K | 0.440 | 0.480 | 11.18 | 12.19 |
| L | --- | 0.665 BSC | --- | 16.89 BSC |
| N | --- | 0.830 | --- | 21.08 |
| Q | 0.151 | 0.165 | 3.84 | 4.19 |
| U | 1.187 BSC | --- | 30.15 BSC | --- |
| V | 0.131 | 0.188 | 3.33 | 4.77 |

- | | | | | |
|--|--|---|---|---|
| <p>STYLE 1: PIN 1. BASE 2. EMITTER CASE: COLLECTOR</p> | <p>STYLE 2: PIN 1. BASE 2. COLLECTOR CASE: EMITTER</p> | <p>STYLE 3: PIN 1. GATE 2. SOURCE CASE: DRAIN</p> | <p>STYLE 4: PIN 1. GROUND 2. INPUT CASE: OUTPUT</p> | <p>STYLE 5: PIN 1. CATHODE 2. EXTERNAL TRIP/DELAY CASE: ANODE</p> |
| <p>STYLE 6: PIN 1. GATE 2. EMITTER CASE: COLLECTOR</p> | <p>STYLE 7: PIN 1. ANODE 2. OPEN CASE: CATHODE</p> | <p>STYLE 8: PIN 1. CATHODE #1 2. CATHODE #2 CASE: ANODE</p> | <p>STYLE 9: PIN 1. ANODE #1 2. ANODE #2 CASE: CATHODE</p> | |

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