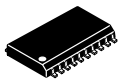
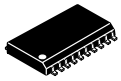
# 3-STATE Octal D-Type Latch

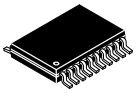
# MM74HC373



SOIC−20 WB
CASE 751D−05



SOIC−20, 300 mils
CASE 751BJ−01



TSSOP−20 WB
CASE 948E

## General Description

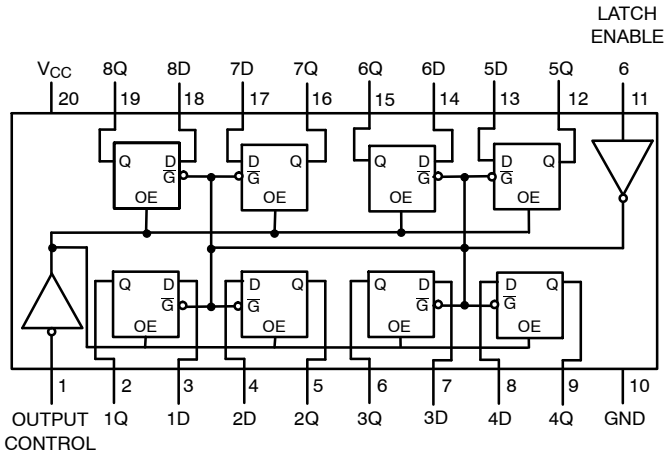
The MM74HC373 high speed octal D−type latches utilize advanced silicon−gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS−TTL loads. Due to the large output drive capability and the 3−STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE input is HIGH, the Q outputs will follow the D inputs. When the LATCH ENABLE goes LOW, data at the D inputs will be retained at the outputs until LATCH ENABLE returns HIGH again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The 74HC logic family is speed, function, and pin−out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to $V_{CC}$ and ground.

## Features

- Typical Propagation Delay: 18 ns
- Wide Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 160 μA Maximum (74 Series)
- Output Drive Capability: 15 LS−TTL Loads
- This is a Pb−Free Device

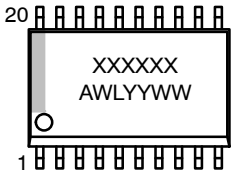



Pin Assignments for SOIC and TSSOP (Top View)

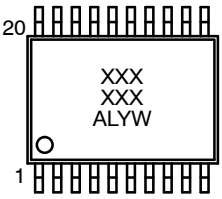
**Figure 1. Connection Diagram**

## MARKING DIAGRAMS

SOIC−20




TSSOP−20




| | | |
|---|---|---|
| XXXXXX | = | Specific Device Code |
| A | = | Assembly Location |
| WL, L | = | Wafer Lot Number |
| Y | = | Year |
| WW, YW | = | Work Week |

## ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

## TRUTH TABLE

| Output Control | Latch Enable | Data | 373 Output |
|---|---|---|---|
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

NOTES:
H = HIGH Level
L = LOW Level
X = Don't Care
$Q_0$ = Level of output before steady−state input conditions were established.
Z = High Impedance

## ABSOLUTE MAXIMUM RATINGS (Note 1)

| Symbol | Rating | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | −0.5 to +6.5 V | V |
| $V_{IN}$ | DC Input Voltage | | −0.5 to $V_{CC}$ +0.5 V | V |
| $V_{OUT}$ | DC Output Voltage | | −0.5 to $V_{CC}$ +0.5 V | V |
| $I_{IK}$, $I_{OK}$ | Clamp Diode Current | | ±20 | mA |
| $I_{OUT}$ | DC Output Current, per pin | | ±35 | mA |
| $I_{CC}$ | DC $V_{CC}$ or GND Current, per pin | | ±70 | mA |
| $T_{STG}$ | Storage Temperature Range | | −65 to +150 | °C |
| $P_D$ | Power Dissipation | SOIC | 1302 | mW |
| | | TSSOP | 833 | mW |
| $T_L$ | Lead Temperature (Soldering 10 seconds) | | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Unless otherwise specified all voltages are referenced to ground.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 2 | 6 | V |
| $V_{IN}$, $V_{OUT}$ | DC Input or Output Voltage | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature Range | | −55 | +125 | °C |
| $t_r$, $t_f$ | Input Rise or Fall Times | $V_{CC}$ = 2.0 V | − | 1000 | ns |
| | | $V_{CC}$ = 4.5 V | − | 500 | ns |
| | | $V_{CC}$ = 6.0 V | − | 400 | ns |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS (Note 2)

| Symbol | Parameter | Conditions | $V_{CC}$ | $T_A$ = 25°C | $T_A$ = −40 to 85°C | $T_A$ = −55 to 125°C | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | |
| $V_{IH}$ | Minimum HIGH Level Input Voltage | | 2.0 V<br>4.5 V<br>6.0 V | | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | V<br>V<br>V |
| $V_{IL}$ | Maximum LOW Level Input Voltage | | 2.0 V<br>4.5 V<br>6.0 V | | 0.5<br>1.35<br>1.8 | 0.5<br>1.35<br>1.8 | 0.5<br>1.35<br>1.8 | V<br>V<br>V |
| $V_{OH}$ | Minimum HIGH Level Output Voltage | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$\|I_{OUT}\| \le 20$ μA | 2.0 V<br>4.5 V<br>6.0 V | 2.0<br>4.5<br>6.0 | 1.9<br>4.4<br>5.9 | 1.9<br>4.4<br>5.9 | 1.9<br>4.4<br>5.9 | V<br>V<br>V |
| | | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$\|I_{OUT}\| \le 6.0$ mA<br>$\|I_{OUT}\| \le 7.8$ mA | <br>4.5 V<br>6.0 V | <br>4.2<br>5.7 | <br>3.98<br>5.48 | <br>3.84<br>5.34 | <br>3.7<br>5.2 | <br>V<br>V |
| $V_{OL}$ | Maximum LOW Level Output Voltage | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$\|I_{OUT}\| \le 20$ μA | 2.0 V<br>4.5 V<br>6.0 V | 0<br>0<br>0 | 0.1<br>0.1<br>0.1 | 0.1<br>0.1<br>0.1 | 0.1<br>0.1<br>0.1 | V<br>V<br>V |
| | | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$\|I_{OUT}\| \le 6.0$ mA<br>$\|I_{OUT}\| \le 7.8$ mA | <br>4.5 V<br>6.0 V | <br>0.2<br>0.2 | <br>0.26<br>0.26 | <br>0.33<br>0.33 | <br>0.4<br>0.4 | <br>V<br>V |
| $I_{IN}$ | Maximum Input Current | $V_{IN} = V_{CC}$ or GND | 6.0 V | | ±0.1 | ±1.0 | ±1.0 | μA |
| $I_{OZ}$ | Maximum 3−STATE Output Leakage Current | $V_{IN} = V_{IH}$ or $V_{IL}$,<br>OC = $V_{IH}$<br>$V_{OUT} = V_{CC}$ or GND | 6.0 V | | ±0.5 | ±5 | ±10 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current | $V_{IN} = V_{CC}$ or GND<br>$I_{OUT}$ = 0 μA | 6.0 V | | 8.0 | 80 | 160 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. For a power supply of 5 V ±10% the worst case output voltages ($V_{OH}$, and $V_{OL}$) occur for HC at 4.5 V. Thus the 4.5 V values should be used when designing with this supply. Worst case $V_{IH}$ and $V_{IL}$ occur at $V_{CC}$ = 5.5 V and 4.5 V respectively. (The $V_{IH}$ value at 5.5 V is 3.85 V.) The worst case leakage current ($I_{IN}$, $I_{CC}$, and $I_{OZ}$) occur for CMOS at the higher voltage and so the 6.0 V values should be used.

## AC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 5 V, $T_A$ = 25°C, $t_r = t_f$ = 6 ns)

| Symbol | Parameter | Conditions | Typ | Guaranteed Limit | Unit |
|---|---|---|---|---|---|
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay, Data to Q | $C_L$ = 45 pF | 18 | 25 | ns |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay, LE toQ | $C_L$ = 45 pF | 21 | 30 | ns |
| $t_{PZH}$, $t_{PZL}$ | Maximum Output Enable Time | $R_L$ = 1 kΩ,<br>$C_L$ = 45 pF | 20 | 28 | ns |
| $t_{PHZ}$, $t_{PLZ}$ | Maximum Output Disable Time | $R_L$ = 1 kΩ,<br>$C_L$ = 5 pF | 18 | 25 | ns |
| $t_s$ | Minimum Set Up Time | | | 5 | ns |
| $t_H$ | Minimum Hold Time | | | 10 | ns |
| $t_W$ | Minimum Pulse Width | | 9 | 16 | ns |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## AC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 2.0–6.0 V, $C_L$ = 50 pF, $t_r = t_f$ = 6 ns, unless otherwise specified)

| Symbol | Parameter | Conditions | $V_{CC}$ | $T_A$ = 25°C | $T_A$ = −40 to 85°C | $T_A$ = −55 to 125°C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | | |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay, Data to Q | $C_L$ = 50 pF | 2.0 V | 50 | 150 | 188 | 225 | ns |
| | | $C_L$ = 150 pF | 2.0 V | 80 | 200 | 250 | 300 | ns |
| | | $C_L$ = 50 pF | 4.5 V | 22 | 30 | 37 | 45 | ns |
| | | $C_L$ = 150 pF | 4.5 V | 30 | 40 | 50 | 60 | ns |
| | | $C_L$ = 50 pF | 6.0 V | 19 | 26 | 31 | 39 | ns |
| | | $C_L$ = 150 pF | 6.0 V | 26 | 35 | 44 | 53 | ns |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay, LE to Q | $C_L$ = 50 pF | 2.0 V | 63 | 175 | 220 | 263 | ns |
| | | $C_L$ = 150 pF | 2.0 V | 110 | 225 | 280 | 338 | ns |
| | | $C_L$ = 50 pF | 4.5 V | 25 | 35 | 44 | 52 | ns |
| | | $C_L$ = 150 pF | 4.5 V | 35 | 45 | 56 | 68 | ns |
| | | $C_L$ = 50 pF | 6.0 V | 21 | 30 | 37 | 45 | ns |
| | | $C_L$ = 150 pF | 6.0 V | 28 | 39 | 49 | 59 | ns |
| $t_{PZH}$, $t_{PZL}$ | Maximum Output Enable Time | $R_L$ = 1 kΩ | | | | | | |
| | | $C_L$ = 50 pF | 2.0 V | 50 | 150 | 188 | 225 | ns |
| | | $C_L$ = 150 pF | 2.0 V | 80 | 200 | 250 | 300 | ns |
| | | $C_L$ = 50 pF | 4.5 V | 21 | 30 | 37 | 45 | ns |
| | | $C_L$ = 150 pF | 4.5 V | 30 | 40 | 50 | 60 | ns |
| | | $C_L$ = 50 pF | 6.0 V | 19 | 26 | 31 | 39 | ns |
| | | $C_L$ = 150 pF | 6.0 V | 26 | 35 | 44 | 53 | ns |
| $t_{PHZ}$, $t_{PLZ}$ | Maximum Output Disable Time | $R_L$ = 1 kΩ | 2.0 V | 50 | 150 | 188 | 225 | ns |
| | | $C_L$ = 50 pF | 4.5 V | 21 | 30 | 37 | 45 | ns |
| | | | 6.0 V | 19 | 26 | 31 | 39 | ns |
| $t_s$ | Minimum Set Up Time | | 2.0 V | – | 50 | 60 | 75 | ns |
| | | | 4.5 V | – | 9 | 13 | 15 | ns |
| | | | 6.0 V | – | 9 | 11 | 13 | ns |
| $t_H$ | Minimum Hold Time | | 2.0 V | – | 5 | 5 | 5 | ns |
| | | | 4.5 V | – | 5 | 5 | 5 | ns |
| | | | 6.0 V | – | 5 | 5 | 5 | ns |
| $t_W$ | Minimum Pulse Width | | 2.0 V | 30 | 80 | 100 | 120 | ns |
| | | | 4.5 V | 10 | 16 | 20 | 24 | ns |
| | | | 6.0 V | 9 | 14 | 18 | 20 | ns |
| $t_{THL}$, $t_{TLH}$ | Maximum Output Rise and Fall Time | $C_L$ = 50 pF | 2.0 V | 25 | 60 | 75 | 90 | ns |
| | | | 4.5 V | 7 | 12 | 15 | 18 | ns |
| | | | 6.0 V | 6 | 10 | 13 | 15 | ns |
| $C_{PD}$ | Power Dissipation Capacitance (Note 3) | (per latch) | | | | | | |
| | | OC = $V_{CC}$ | – | 30 | – | – | – | pF |
| | | OC = GND | – | 50 | – | – | – | pF |
| $C_{IN}$ | Maximum Input Capacitance | | – | 5 | 10 | 10 | 10 | pF |
| $C_{OUT}$ | Maximum Output Capacitance | | – | 15 | 20 | 20 | 20 | pF |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. $C_{PD}$ determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

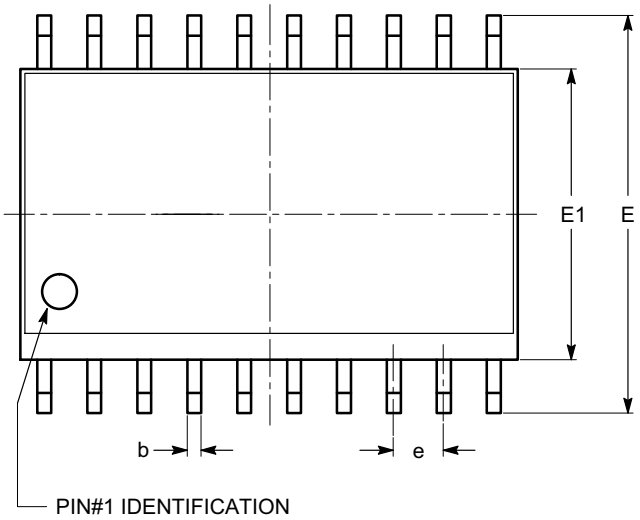
## ORDERING INFORMATION

| Device | Marking | Package | Shipping† |
|---|---|---|---|
| MM74HC373WM | HC373A | SOIC−20 WB<br>(Pb−Free and Halide Free) | 38 Units / Tube |
| MM74HC373WMX | HC373A | SOIC−20, 300 mils<br>(Pb−Free and Halide Free) | 1000 / Tape & Reel |
| MM74HC373MTC | HC<br>373A | TSSOP−20 WB<br>(Pb−Free) | 75 Units / Tube |
| MM74HC373MTCX | HC<br>373A | TSSOP−20 WB<br>(Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

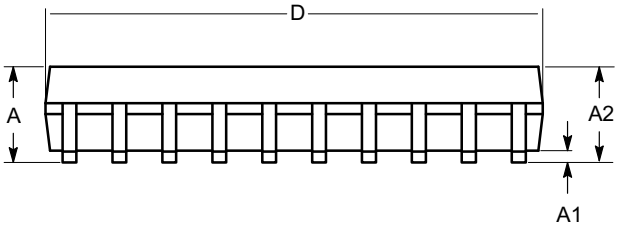
**SOIC−20, 300 mils**
CASE 751BJ
ISSUE O

DATE 19 DEC 2008

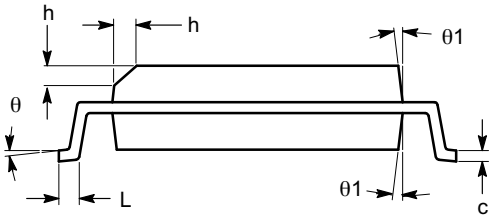



**TOP VIEW**

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 2.36 | 2.49 | 2.64 |
| A1 | 0.10 | | 0.30 |
| A2 | 2.05 | | 2.55 |
| b | 0.31 | 0.41 | 0.51 |
| c | 0.20 | 0.27 | 0.33 |
| D | 12.60 | 12.80 | 13.00 |
| E | 10.01 | 10.30 | 10.64 |
| E1 | 7.40 | 7.50 | 7.60 |
| e | | 1.27 BSC | |
| h | 0.25 | | 0.75 |
| L | 0.40 | 0.81 | 1.27 |
| θ | 0° | | 8° |
| θ1 | 5° | | 15° |




**SIDE VIEW**




**END VIEW**

**Notes:**
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-013.

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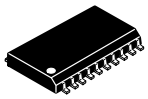
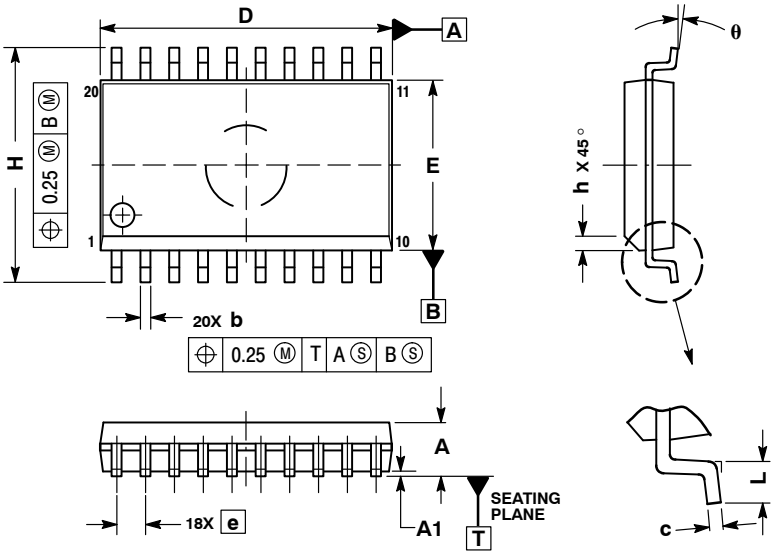
|---|---|---|
| DESCRIPTION: | SOIC−20, 300 MILS | PAGE 1 OF 1 |

**SOIC−20 WB**
CASE 751D−05
ISSUE H

DATE 22 APR 2015



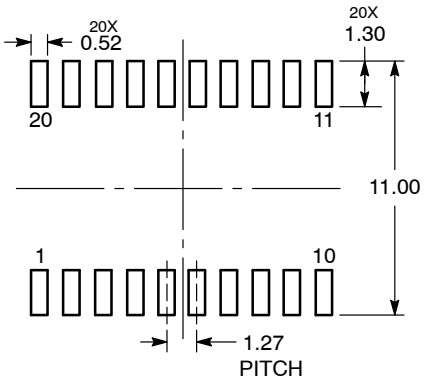
**SCALE 1:1**




NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

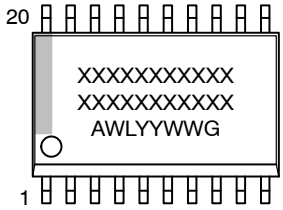
## RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*



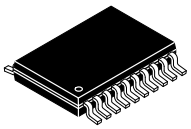

XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

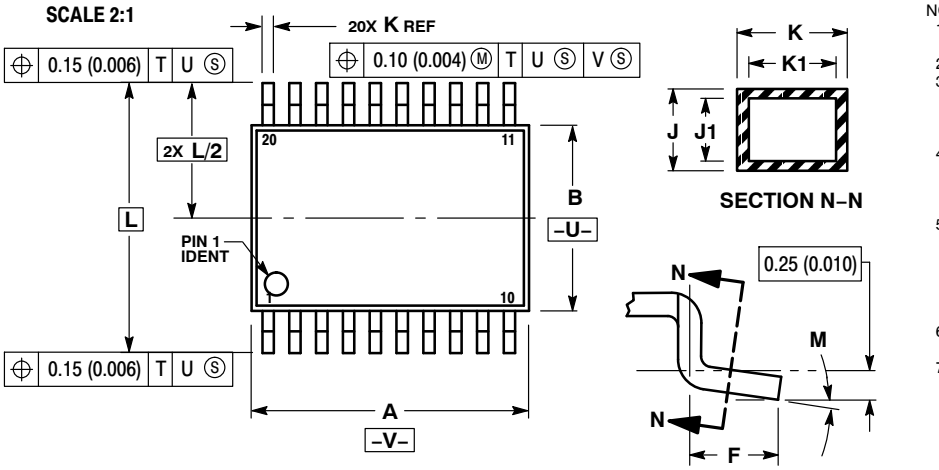
| | | | |
|---|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB42343B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. | |
| **DESCRIPTION:** | **SOIC−20 WB** | | **PAGE 1 OF 1** |

**TSSOP–20 WB**
CASE 948E
ISSUE D

DATE 17 FEB 2016



SCALE 2:1



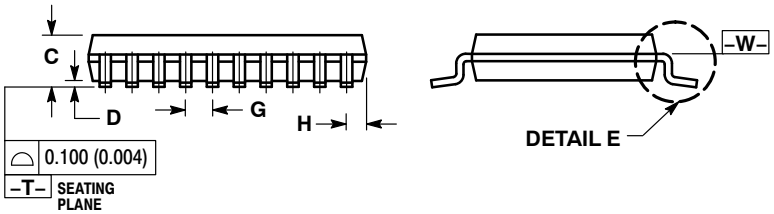




SECTION N–N




DETAIL E



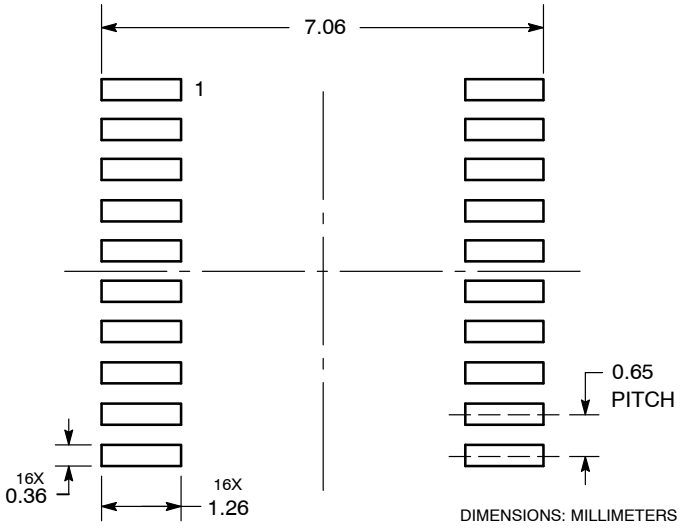




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

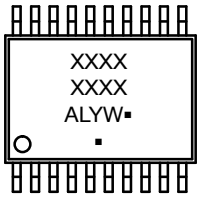
## RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb–Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | | |
|---|---|---|---|
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| **DESCRIPTION:** | **TSSOP–20 WB** | | **PAGE 1 OF 1** |

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