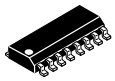
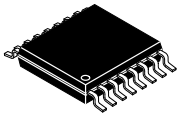
8-Bit Shift Register with Output Latches

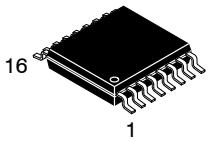
MM74HC595



SOIC−16
CASE 751B−05



TSSOP 16
CASE 948AH−01



TSSOP−16
CASE 948F−01

General Description

The MM74HC595 high−speed shift register utilizes advanced silicon−gate CMOS technology. This device possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS−TTL loads.

This device contains an eight−bit serial−in, parallel−out, shift register that feeds an eight−bit D−type storage register. The storage register has eight 3−state outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct−overriding clear, serial input, and serial output (standard) pins for cascading. Both the shift register and storage register use positive−edge triggered clocks. If both clocks are connected together, the shift register state is one clock pulse ahead of the storage register.

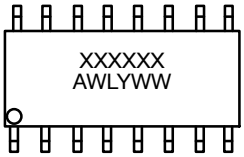
The 74HC logic family is speed, function, and pin−out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

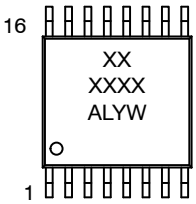
- Low Quiescent Current: 160 μA Maximum (74HC Series)
- Low Input Current: 1 μA Maximum
- 8−Bit Serial−In, Parallel−Out Shift Register with Storage
- Wide Operating Voltage Range: 2 V−6 V
- Cascadable
- Shift Register has Direct Clear
- Guaranteed Shift Frequency: DC to 30 MHz
- This Device is Pb−Free and is RoHS Compliant

MARKING DIAGRAMS

SOIC−16



TSSOP−16



XXXXXX	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot Number
Y	= Year
WW, YW	= Work Week

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

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Block Diagram

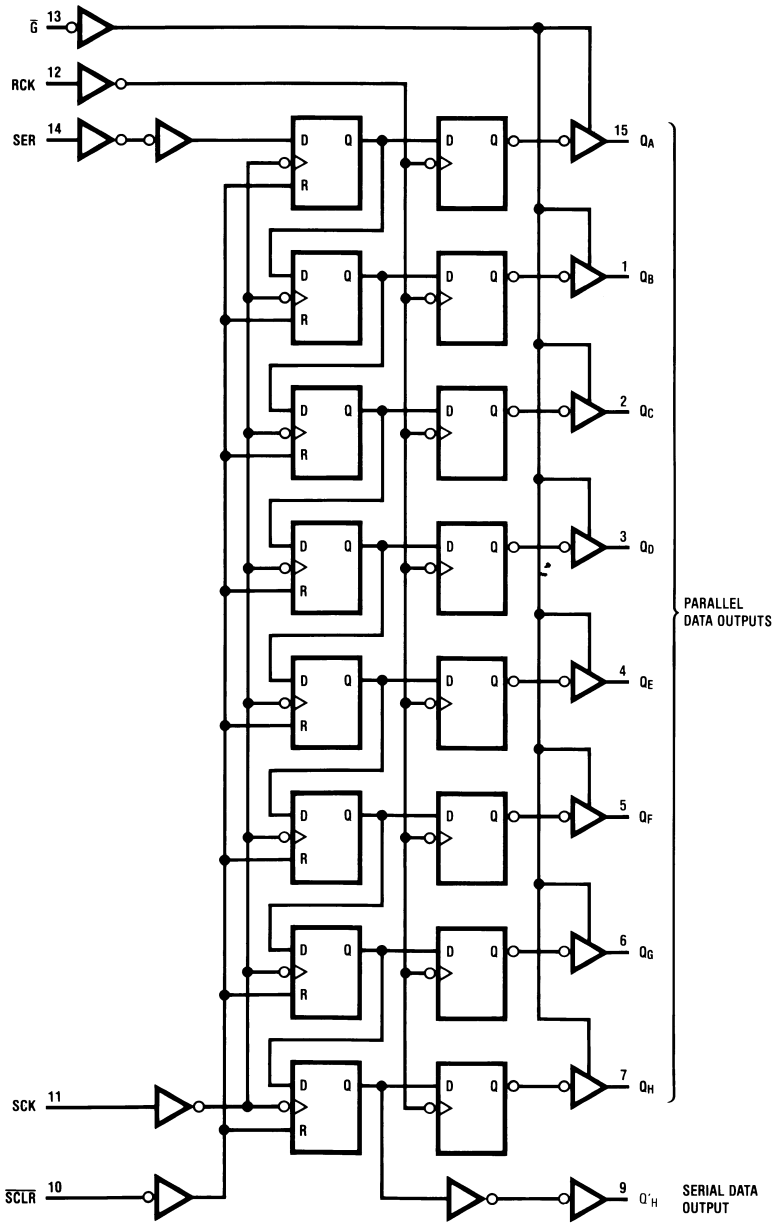


Figure 1. Logic Diagram (Positive Logic)

Pin Configuration

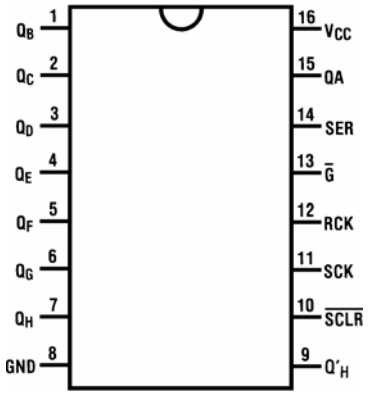


Figure 2. Pin Configuration

PIN DEFINITIONS

Pin No.	Symbol	Description
1	Q_B	Output Bit B
2	Q_C	Output Bit C
3	Q_D	Output Bit D
4	Q_E	Output Bit E
5	Q_F	Output Bit F
6	Q_G	Output Bit G
7	Q_H	Output Bit H
8	GND	Ground
9	Q'_H	Serial Data Output
10	$\overline{SCLR}$	Shift Register Clear
11	SCK	Shift Register Clock Input
12	RCK	Storage Register Clock Input
13	$\overline{G}$	Output Enable
14	SER	Serial Data Input
15	QA	Output Bit A
16	V_{CC}	Supply Voltage

TRUTH TABLE

RCK	SCK	SCLR	G	Function
X	X	X	H	QA through Q_H = 3−state
X	X	L	L	Shift register clocked; $Q'_H = 0$
X	↑	H	L	Shift register clocked; $Q_N = Q_{n-1}$, Q_0 = SER
↑	X	H	L	Contents of shift; register transferred to output latches

NOTES: L = Logic Level LOW
H = Logic Level HIGH
X = Don't Care
↑ = Transition from LOW to HIGH level

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Rating		Min	Max	Unit
V_{CC}	Supply Voltage		−0.5	6.5	V
V_{IN}	DC Input Voltage		−0.5	V_{CC} + 0.5	V
V_{OUT}	DC Output Voltage		−0.5	V_{CC} + 0.5	V
I_{IK}, I_{OK}	Clamp Diode Current			±20	mA
I_{OUT}	DC Output Current, per pin			±35	mA
I_{CC}	DC VCC or GND Current, per pin			±70	mA
T_{STG}	Storage Temperature Range		−65	+150	°C
P_D	Power Dissipation	SOIC Package only		500	mW
T_L	Lead Temperature			+260	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22−A114		4000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Unless otherwise specified all voltages are referenced to ground.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		2	6	V
V_{IN}, V_{OUT}	DC Input or Output Voltage		0	V_{CC}	V
T_A	Operating Temperature Range		−55	+125	°C
t_R, t_F	Input Rise and Fall Times	V_{CC} = 2.0 V	–	1000	ns
		V_{CC} = 4.5 V	–	500	
		V_{CC} = 6.0 V	–	400	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 2)

Symbol	Parameter	Conditions		V_{CC}	T_A = 25°C Typ	T_A = 25°C Guaranteed Limits	T_A = −40 to 85°C Guaranteed Limits	T_A = −55 to 125°C Guaranteed Limits	Unit
V_{IH}	Minimum HIGH Level Input Voltage			2.0 V		1.50	1.50	1.50	V
				4.5 V		3.15	3.15	3.15	V
				6.0 V		4.20	4.20	4.20	V
V_{IL}	Minimum LOW Level Input Voltage			2.0 V		0.50	0.50	0.50	V
				4.5 V		1.35	1.35	1.35	V
				6.0 V		1.80	1.80	1.80	V
V_{OH}	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}	$\lvert I_{OUT} \rvert \le 20\ \mu A$	2.0 V	2.00	1.90	1.90	1.90	V
				4.5 V	4.50	4.40	4.40	4.40	V
				6.0 V	6.00	5.90	5.90	5.90	V
	Q'_H	$V_{IN} = V_{IH}$ or V_{IL}	$\lvert I_{OUT} \rvert \le 4.0$ mA	4.5 V	4.20	3.98	3.84	3.70	V
			$\lvert I_{OUT} \rvert \le 5.2$ mA	6.0 V	5.20	5.48	5.34	5.20	V
	QA through Q_H	$V_{IN} = V_{IH}$ or V_{IL}	$\lvert I_{OUT} \rvert \le 6.0$ mA	4.5 V	4.20	3.98	3.84	3.70	V
			$\lvert I_{OUT} \rvert \le 7.8$ mA	6.0 V	5.70	5.48	5.34	5.20	V
V_{OL}	Minimum LOW Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}	$\lvert I_{OUT} \rvert \le 20\ \mu A$	2.0 V	0	0.10	0.10	0.10	V
				4.5 V	0	0.10	0.10	0.10	V
				6.0 V	0	0.10	0.10	0.10	V
	Q'_H	$V_{IN} = V_{IH}$ or V_{IL}	$\lvert I_{OUT} \rvert \le 4.0$ mA	4.5 V	0.20	0.26	0.33	0.40	V
			$\lvert I_{OUT} \rvert \le 5.2$ mA	6.0 V	0.20	0.26	0.33	0.40	V
	QA through Q_H	$V_{IN} = V_{IH}$ or V_{IL}	$\lvert I_{OUT} \rvert \le 6.0$ mA	4.5 V	0.20	0.26	0.33	0.40	V
			$\lvert I_{OUT} \rvert \le 7.8$ mA	6.0 V	0.20	0.26	0.33	0.40	V
I_{IN}	Maximum Input Output Leakage	$V_{IN} = V_{CC}$ or GND		6.0 V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum 3−STATE Output Leakage	$V_{OUT} = V_{CC}$ or GND	$\overline{G} = V_{IH}$	6.0 V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	$I_{OUT} = 0\ \mu A$	6.0 V		8.0	80	160	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. For a power supply of 5 V ±10% the worst−case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5 V. The 4.5 V values should be used when designing with this supply. Worst−case V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V, respectively; V_{IH} value at 5.5 V is 3.85 V. The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage; so the 6.0 V values should be used.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5 V, T_A = 25°C, $t_r = t_f$ = 6 ns)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Unit
f_{MAX}	Maximum Operating Frequency of SCK		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SCK to Q'_H	C_L = 45 pF	12	20	ns
	Maximum Propagation Delay, RCK to Q_A thru Q'_H		18	30	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time from $\overline{G}$ to Q_A thru Q'_H	R_L = 1 kΩ C_L = 45 pF	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time from $\overline{G}$ to Q_A thru Q'_H	R_L = 1 kΩ C_L = 45 pF	15	25	ns
t_S	Minimum Setup Time from SER to SCK			20	ns
	Minimum Setup Time from $\overline{SCLR}$ to SCK			20	ns
	Minimum Setup Time from SER to RCK (Note 3)			40	ns

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 6 ns)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Unit
t_H	Minimum Hold Time from SER to SCK			5	ns
t_W	Minimum Pulse Width of SCK or RCK			16	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. This setup time ensures the register will see stable data from the shift−register outputs. The clocks may be connected together in which case the storage register state will be one clock pulse behind the shift register.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.0 V−6.0 V, C_L = 50 pF, t_r = t_f = 6 ns, unless otherwise specified)

Symbol	Parameter	Conditions		V_{CC}	T_A = 25°C Typ	T_A = 25°C Guaranteed Limits	T_A = −40 to 85°C Guaranteed Limits	T_A = −55 to 125°C Guaranteed Limits	Unit
f_{MAX}	Maximum Operating Frequency	C_L = 50 pF		2.0 V	10.0	6.0	4.8	4.0	ns
				4.5 V	45.0	30.0	24.0	20.0	ns
				6.0 V	50.0	35.0	28.0	24.0	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SCK to Q'_H	C_L = 50 pF		2.0 V	58.0	210.0	235.0	315.0	ns
		C_L = 150 pF		2.0 V	83.0	294.0	367.0	441.0	ns
		C_L = 50 pF		4.5 V	14.0	42.0	53.0	63.0	ns
		C_L = 150 pF		4.5 V	17.0	58.0	74.0	88.0	ns
		C_L = 50 pF		6.0 V	10.0	36.0	45.0	54.0	ns
		C_L = 150 pF		6.0 V	14.0	50.0	63.0	76.0	ns
	Maximum Propagation Delay, RCK to Q_A thru Q'_H	C_L = 50 pF		2.0 V	70.0	175.0	220.0	265.0	ns
		C_L = 150 pF		2.0 V	105.0	245.0	306.0	368.0	ns
		C_L = 50 pF		4.5 V	21.0	35.0	44.0	53.0	ns
		C_L = 150 pF		4.5 V	28.0	49.0	61.0	74.0	ns
		C_L = 50 pF		6.0 V	18.0	30.0	37.0	45.0	ns
		C_L = 150 pF		6.0 V	26.0	42.0	53.0	63.0	ns
	Maximum Propagation Delay, $\overline{SCLR}$ to Q'_H			2.0 V		175.0	221.0	261.0	ns
				4.5 V		35.0	44.0	52.0	ns
				6.0 V		30.0	37.0	44.0	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time from $\overline{G}$ to Q_A thru Q'_H	R_L = 1 kΩ	C_L = 50 pF	2.0 V	75.0	175.0	220.0	265.0	ns
			C_L = 150 pF	2.0 V	100.0	245.0	306.0	368.0	ns
		C_L = 50 pF		4.5 V	15.0	35.0	44.0	53.0	ns
		C_L = 150 pF		4.5 V	20.0	49.0	61.0	74.0	ns
		C_L = 50 pF		6.0 V	13.0	30.0	37.0	45.0	ns
		C_L = 150 pF		6.0 V	17.0	42.0	53.0	63.0	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time from $\overline{G}$ to Q_A thru Q'_H	R_L = 1 kΩ		2.0 V	75.0	175.0	220.0	265.0	ns
		C_L = 50 pF		4.5 V	15.0	35.0	44.0	53.0	ns
				6.0 V	13.0	30.0	37.0	45.0	ns
t_S	Minimum Setup Time from SER to SCK	R_L = 1 kΩ		2.0 V		100.0	125.0	150.0	ns
		C_L = 50 pF		4.5 V		20.0	25.0	30.0	ns
				6.0 V		17.0	21.0	25.0	ns
t_R	Minimum Removal Time from $\overline{SCLR}$ to SCK			2.0 V		50.0	63.0	75.0	ns
				4.5 V		10.0	13.0	15.0	ns
				6.0 V		9.0	11.0	13.0	ns
t_S	Minimum Setup Time from SCK to RCK			2.0 V		100.0	125.0	150.0	ns
				4.5 V		20.0	25.0	30.0	ns
				6.0 V		17.0	21.0	26.0	ns

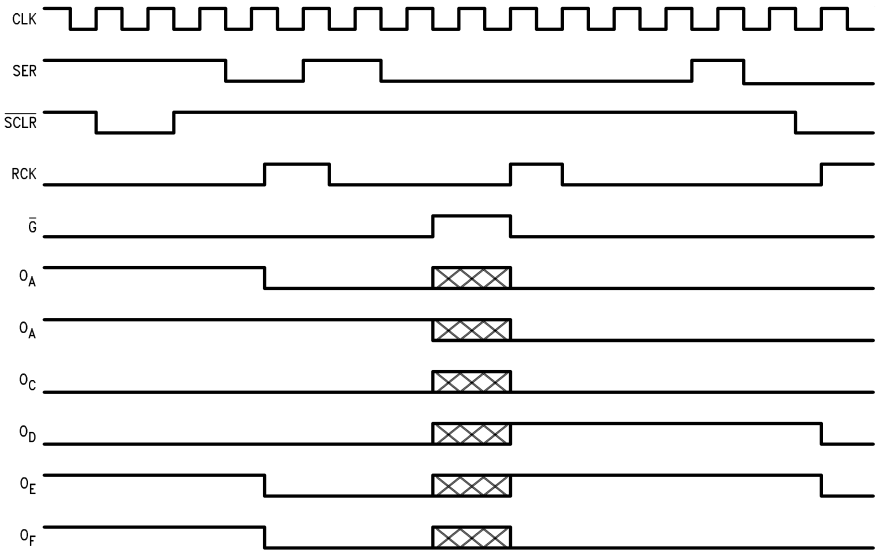
ELECTRICAL CHARACTERISTICS (continued)
(V_{CC} = 2.0 V−6.0 V, C_L = 50 pF, t_r = t_f = 6 ns, unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C Typ	T_A = 25°C Guaranteed Limits	T_A = −40 to 85°C Guaranteed Limits	T_A = −55 to 125°C Guaranteed Limits	Unit
t_H	Minimum Hold Time from SER to SCK		2.0 V		5.0	5.0	5.0	ns
			4.5 V		5.0	5.0	5.0	ns
			6.0 V		5.0	5.0	5.0	ns
t_W	Minimum Pulse Width of SCK or $\overline{SCLR}$		2.0 V	30.0	80.0	100.0	120.0	ns
			4.5 V	9.0	16.0	20.0	24.0	ns
			6.0 V	8.0	14.0	18.0	22.0	ns
t_R, t_F	Maximum Input Rise and Fall Time, Clock		2.0 V		1000.0	1000.0	1000.0	ns
			4.5 V		500.0	500.0	500.0	ns
			6.0 V		400.0	400.0	400.0	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time Q_A–Q_H		2.0 V	25.0	60.0	75.0	90.0	ns
			4.5 V	7.0	12.0	15.0	18.0	ns
			6.0 V	6.0	10.0	13.0	15.0	ns
	Maximum Output Rise and Fall Time Q'_H		2.0 V		75.0	95.0	110.0	ns
			4.5 V		15.0	19.0	22.0	ns
			6.0 V		13.0	16.0	19.0	ns
C_{PD}	Power Dissipation Capacitance, Outputs Enabled (Note 4)	$\overline{G}$ = V_{CC}		90.0				pF
		$\overline{G}$ = GND		150.0				pF
C_{IN}	Maximum Input Capacitance			5.0	10.0	10.0	10.0	pF
C_{OUT}	Maximum Output Capacitance			15.0	20.0	20.0	20.0	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Timing Diagram



NOTE:

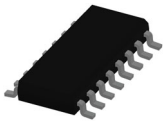
5. ⊠ Implies that the output is in 3−state mode.

Figure 3. Timing Diagram

ORDERING INFORMATION

Device	Top Marking	Package	Shipping†
MM74HC595M	HC595A	SOIC−16 (Pb−Free)	48 Units / Tube
MM74HC595MX	HC595A		2500 / Tape & Reel
MM74HC595MTC	HC 595A	TSSOP−16 (Pb−Free and Halide Free)	96 Units / Tube
MM74HC595MTCX	HC 595A	TSSOP 16 (Pb−Free and Halide Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

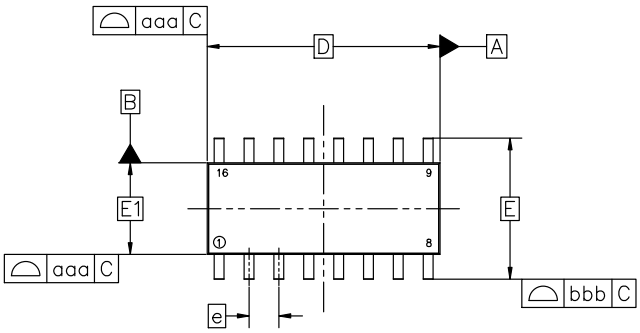


SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

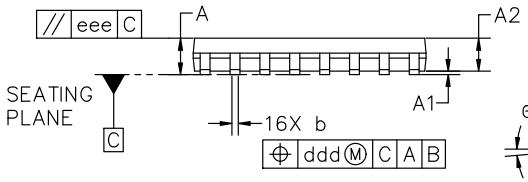
DATE 29 MAY 2024

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.

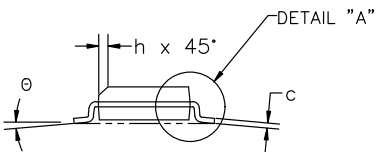
MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.00	0.05	0.10
A2	1.35	1.50	1.65
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	---	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



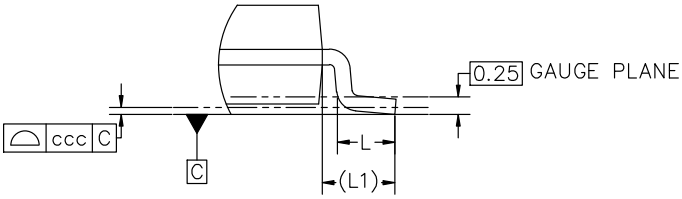
TOP VIEW



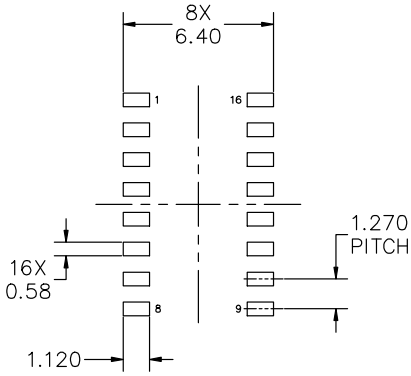
SIDE VIEW



END VIEW



DETAIL "A"
Scale 3:1



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

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DESCRIPTION:	SOIC−16 9.90X3.90X1.50 1.27P	PAGE 1 OF 2

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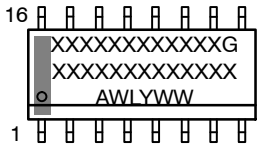
SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

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DESCRIPTION:	SOIC−16 9.90X3.90X1.50 1.27P	PAGE 2 OF 2

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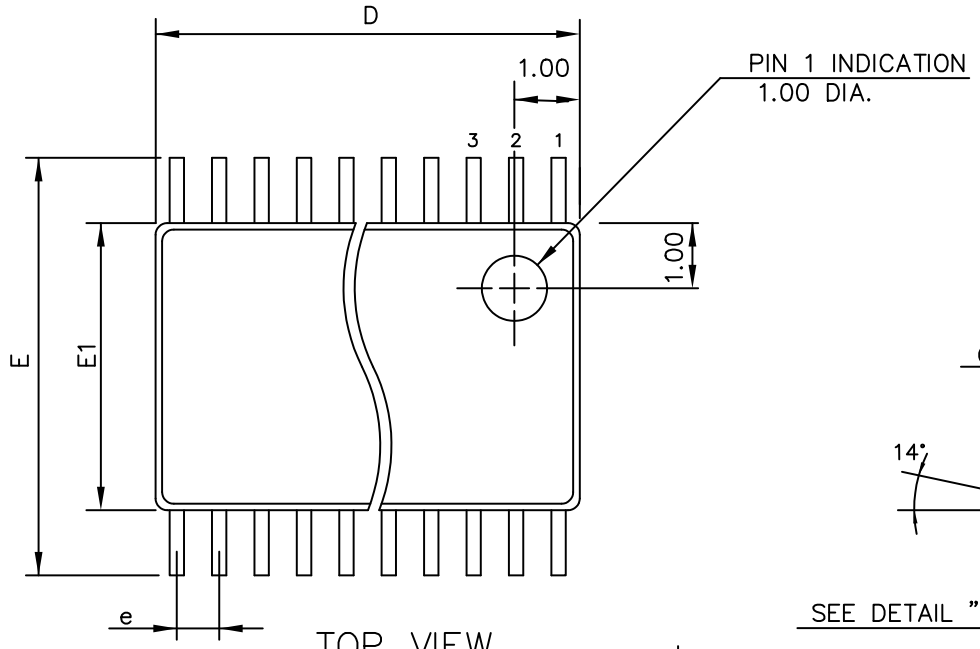
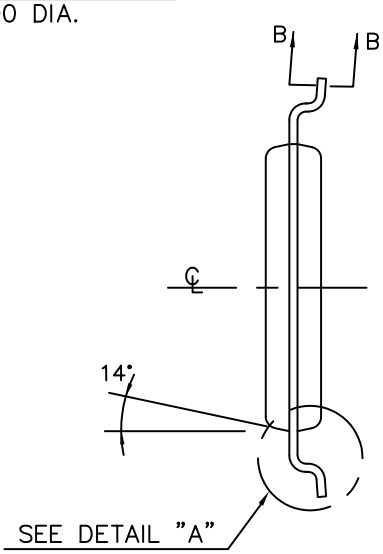
TSSOP 16
CASE 948AH
ISSUE O

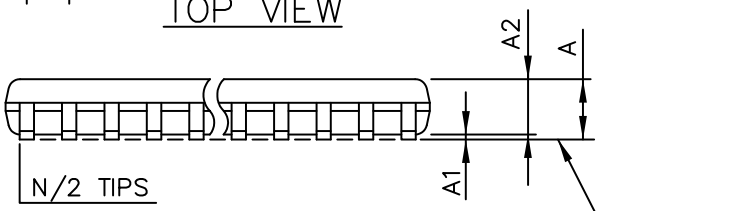
DATE 19 SEP 2008



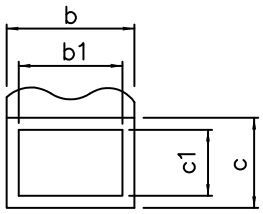
TOP VIEW



END VIEW



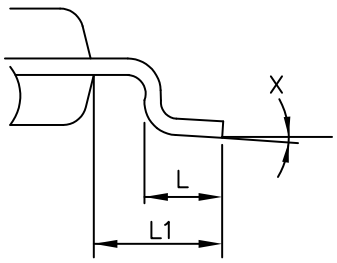
SIDE VIEW



SECTION "B–B"

THIS TABLE FOR 0.65mm PITCH

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE VARI–ATIONS	D	N
A	——	——	1.10	AA/AAT	3.00 BSC	8
A_1	0.05	——	0.15	AB–1/ABT	5.00 BSC	14
A_2	0.85	0.90	0.95	AB/ABT	5.00 BSC	16
b	0.19	–	0.30	AD/ADT	7.80 BSC	24
b1	0.19	0.22	0.25			
c	0.09	–	0.20			
c1	0.09	0.127	0.16			
D	SEE VARIATIONS					
E1	4.30	4.40	4.50			
e	0.65 BSC					
E	6.40 BSC					
L	0.50	0.60	0.70			
L1	1.00 REF					
N	SEE VARIATIONS					
X	0°	——	8°			



DETAIL 'A'

ALL DIMENSIONS IN MILLIMETERS

MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm ON D PER SIDE

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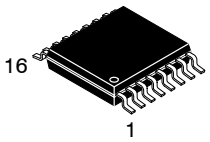
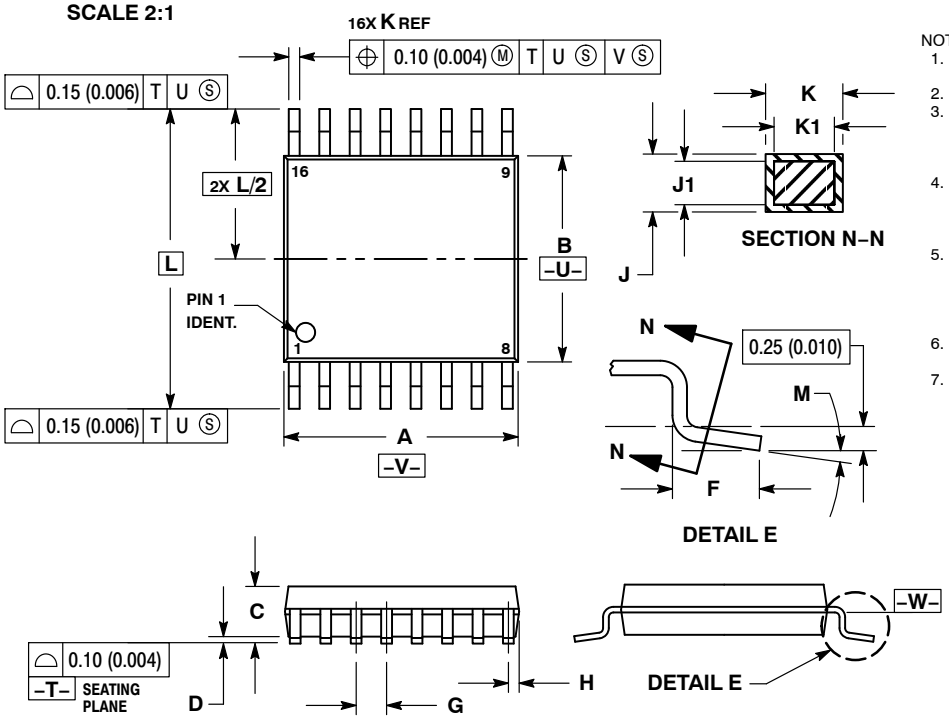


SCALE 2:1

TSSOP−16 WB
CASE 948F
ISSUE B

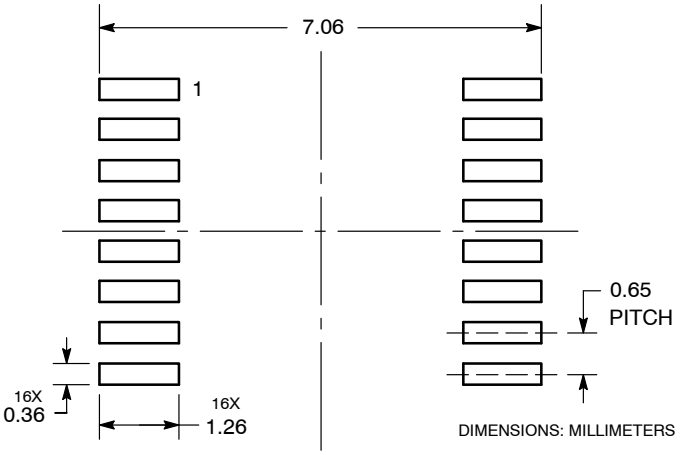
DATE 19 OCT 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

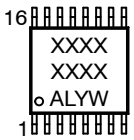
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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