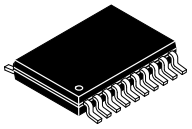
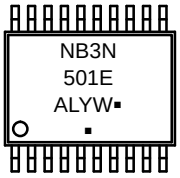
# 3.3 V LVTTL/LVCMOS 2:1 MUX to 4 LVPECL Differential Clock Fanout Buffer Outputs with Clock Enable and Clock Select

# NB3N853501E



**TSSOP−20**
**DT SUFFIX**
**CASE 948E**

**MARKING DIAGRAM**




| | |
|---|---|
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

### Description

The NB3N853501E is a pure 3.3 V supply 2:1:4 clock distribution fanout buffer. Input MUX selects one of two LVCMOS/LVTTL CLK lines by the CLK_SEL pin (HIGH for CLK1, LOW for CLK0) using LVCMOS/LVTTL levels. Outputs are LVPECL levels and are synchronously enabled by CLK_EN using LVCMOS/LVTTL levels (HIGH to enable outputs, LOW to disable output).

### Features

- Four differential LVPECL Outputs
- Two Selectable LVCMOS/LVTTL CLOCK Inputs
- Up to 266 MHz Clock Operation
- Output to Output Skew: 30 ps (Max.)
- Device to Device Skew 250 ps (Max.)
- Propagation Delay 2.0 ns (Max.)
- Operating range: $V_{CC}$ = 3.3 ±5% V( 3.135 to 3.465 V)
- Additive Phase Jitter, RMS: 62 fs (Typ)
- Synchronous Clock Enable Control
- Industrial Temp. Range (−40°C to 85°C)
- Pb−Free TSSOP20 Package
- These are Pb−Free Devices

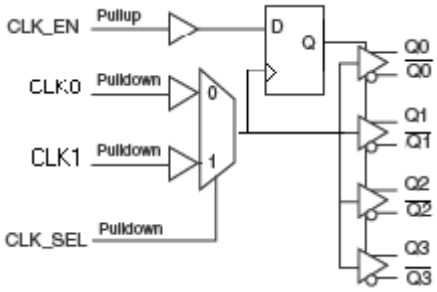



**Figure 1. Simplified Logic Diagram**

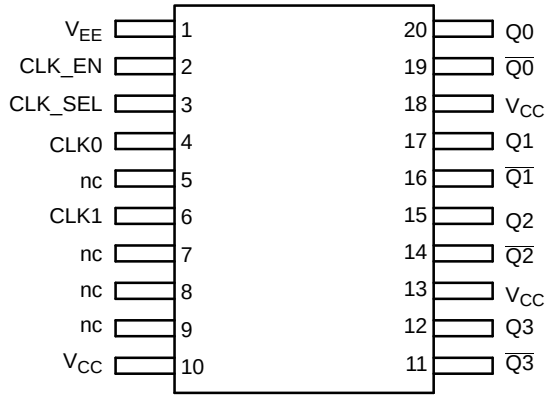



**Figure 2. Pinout Diagram (Top View)**

**Table 1. PIN DESCRIPTION**

| Number | Name | I/O | Open Default | Description |
|---|---|---|---|---|
| 1 | $V_{EE}$ | | | Negative (Ground) Power Supply pin must be externally connected to power supply to guarantee proper operation. |
| 2 | CLK_EN | LVCMOS / LVTTL | Pullup | Synchronized Clock Enable when HIGH. When LOW, outputs are disabled (Qx HIGH, $\overline{Qx}$ LOW) |
| 3 | CLK_SEL | LVCMOS / LVTTL | Pulldown | Clock Input Select (HIGH selects CLK1, LOW selects CLK0 input) |
| 4 | CLK0 | LVCMOS / LVTTL | Pulldown | Clock 0 Input. Float open when unused. |
| 5, 6, 8, 9 | nc | | | No Connect |
| 6 | CLK1 | LVCMOS / LVTTL | Pulldown | Clock 1 Input. Float open when unused. |
| 10, 13, 18 | $V_{CC}$ | | | Positive Power Supply pins must be externally connected to power supply to guarantee proper operation. |
| 11, 14, 16, 19 | $\overline{Q[3:0]}$ | LVPECL | | Invert Differential Outputs |
| 12, 15, 16, 20 | Q[3:0] | LVPECL | | True Differential Outputs |

**Table 2. FUNCTIONS**

| Inputs | | | Outputs | | |
|---|---|---|---|---|---|
| **CLK_EN** | **CLK_SEL** | **Input Function** | **Output Function** | **Qx** | **$\overline{Qx}$** |
| 0 | 0 | CLK0 input selected | Disabled | LOW | HIGH |
| 0 | 1 | CLK1 Input Selected | Disabled | LOW | HIGH |
| 1 | 0 | CLK0 input selected | Enabled | CLK0 | Invert of CLK1 |
| 1 | 1 | CLK1 Input Selected | Enabled | CLK1 | Invert of CLK1 |

1. After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as show in Figure 3.

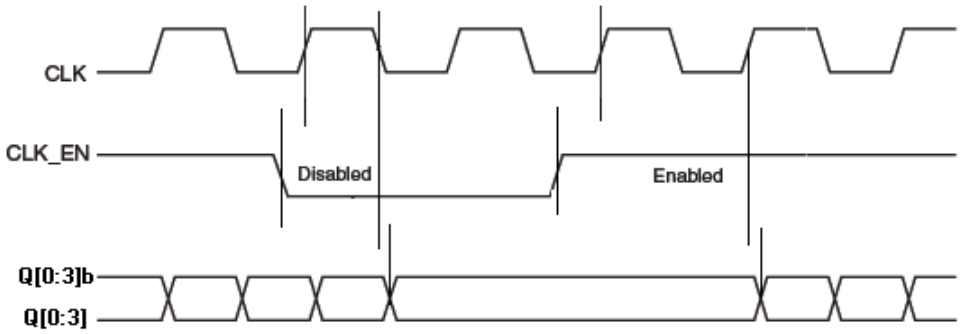



**Figure 3. CLK_EN TIMING DIAGRAM**

**Table 3. ATTRIBUTES** (Note 2)

| Characteristics | | Value |
|---|---|---|
| Internal Input Pullup Resistor | | 50 kΩ |
| Internal Input Pulldown Resistor | | 50 kΩ |
| ESD Protection | Human Body Model<br>Machine Model | > 2 kV<br>> 200 V |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 2) | | Level 1 |
| Flammability Rating<br>Oxygen Index | | UL 94 V−0 @ 0.125 in<br>28 to 34 |
| Transistor Count | | 317 Devices |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | |

2. For additional information, see Application Note AND8003/D.

**Table 4. MAXIMUM RATINGS** (Note 3)

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | | 4.6 | V |
| $V_{in}$ | Input Voltage | | | $-0.5 \le V_I \le V_{CC} + 0.5$ | V |
| $C_{in}$ | Input Capacitance | | | 4 | pF |
| $I_{out}$ | Output Current | Continuous<br>Surge | | 50<br>100 | mA |
| $T_A$ | Operating Temperature Range, Industrial | | | −40 to ≤ +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) | 0 lfpm<br>500 lfpm | TSSOP−20 | 140<br>50 | °C/W |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) | 0 lfpm | Single−Layer PCB (700 mm$^2$, 2 oz) | 128 | °C/W |
| | | 200 lfpm | Multi−Layer PCB (700 mm$^2$, 2 oz) | 94 | |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) | (Note 4) | TSSOP−20 | 23 to 41 | °C/W |
| $T_{sol}$ | Wave Solder | | | 265 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
4. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).

**Table 5. DC CHARACTERISTICS** $V_{CC}$ = 3.3 ±5% V (3.135 to 3.465 V), GND = 0 V, $T_A$ = −40°C to +85°C (Note 5)

| Symbol | Characteristic | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{EE}$ | Power Supply Current | | | | 50 | mA |
| $V_{IH}$ | Input HIGH Voltage | | 2 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input LOW Voltage | CLK0 CLK1<br>CLK_EN CLK_SEL | −0.3<br>−0.3 | | 1.3<br>0.8 | V |
| $I_{IH}$ | Input High Current ($V_{CC}$ = $V_{in}$ = 3.456 V) | CLKx, CLK_SEL<br>CLK_EN | | | 150<br>5 | μA |
| $I_{IL}$ | Input LOW Current ($V_{CC}$ = 3.456 V; $V_{in}$ = GND) | CLKx, CLK_SEL<br>CLK_EN | −5<br>−150 | | | μA |
| $V_{OH}$ | Output HIGH Voltage | | $V_{CC}$ − 1.4 | | $V_{CC}$ − 0.9 | V |
| $V_{OL}$ | Output LOW Voltage | | $V_{CC}$ − 2.0 | | $V_{CC}$ − 1.7 | V |
| $VOUT_{SWING}$ | Output Voltage Swing (peak−to−peak) | | 0.6 | | 1.0 | V |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

5. Outputs terminated 50 Ω to $V_{CC}$ − 2.0 V, see Figure 4. Input levels of 0.8 V and 2.4 V unless stated otherwise.

**Table 6. AC CHARACTERISTICS** $V_{CC}$ = 3.3 ±5% V (3.135 to 3.465 V), GND = 0 V, $T_A$ = −40°C to +85°C (Note 6)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $F_{MAX}$ | Maximum Operating Frequency | 0 | | 266 | MHz |
| $t_{PD}$ | Propagation Delay | 0.9 | | 2.0 | ns |
| $tSKEW_{DC}$ | Duty Cycle Skew same path similar conditions at 50 MHz | 48 | 50 | 52 | % |
| $tSKEW_{O-O}$ | Output to Output Skew Within A Device | | | 30 | ps |
| $tSKEW_{D-D}$ | Device−to−Device Skew similar path and conditions | | | 250 | ps |
| $t_{JIT}$ | Additive Phase Noise Jitter (RMS) @ 155.52 MHz (Integrated from 12 kHz to 20 MHz) See Figure 6. | | 0.062 | | ps |
| $t_r/t_f$ | Output rise and fall times @ 266 MHz (20% and 80% points) | 240 | | 700 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

6. Outputs terminated 50 Ω to $V_{CC}$ − 2.0 V, see Figure 4. Input levels of 0.8 V and 2.4 V unless stated otherwise. Measured from Input Midpoint ($V_{DD}$/2) to differential Output crosspoints, see Figure 5.

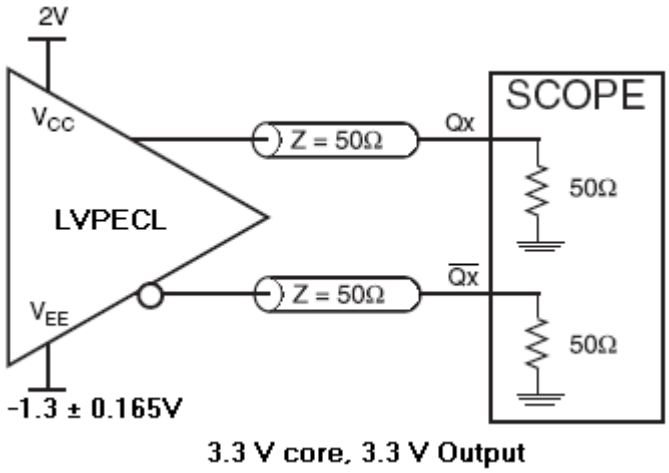



**Figure 4. Typical Test Setup and Termination for Evaluation. The $V_{CC}$ of 2.0 V and $V_{EE}$ of −1.3 ±0.165 V Split supply allows a direct connection to an oscilloscope 50 Ω impedance input module. Also reference AND8020.**

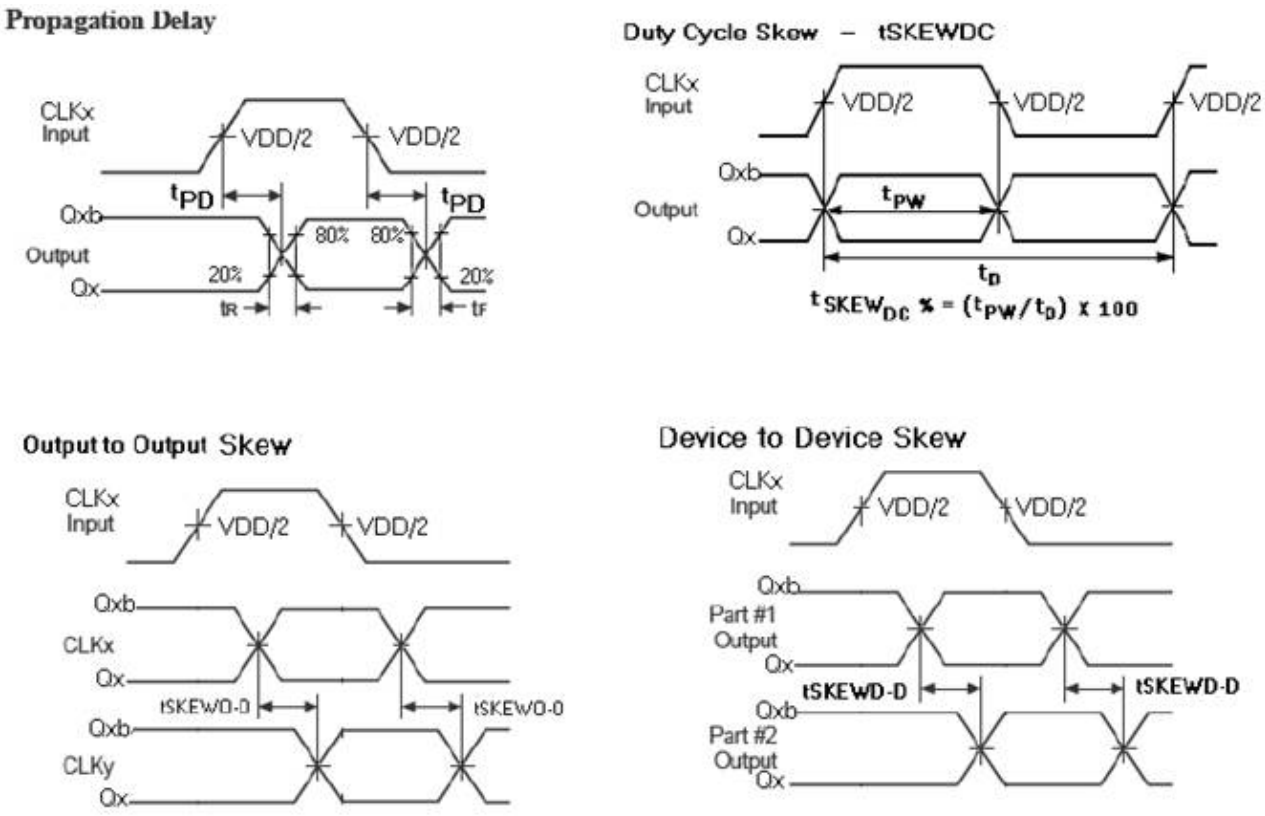



**Figure 5. AC Measurement Reference**

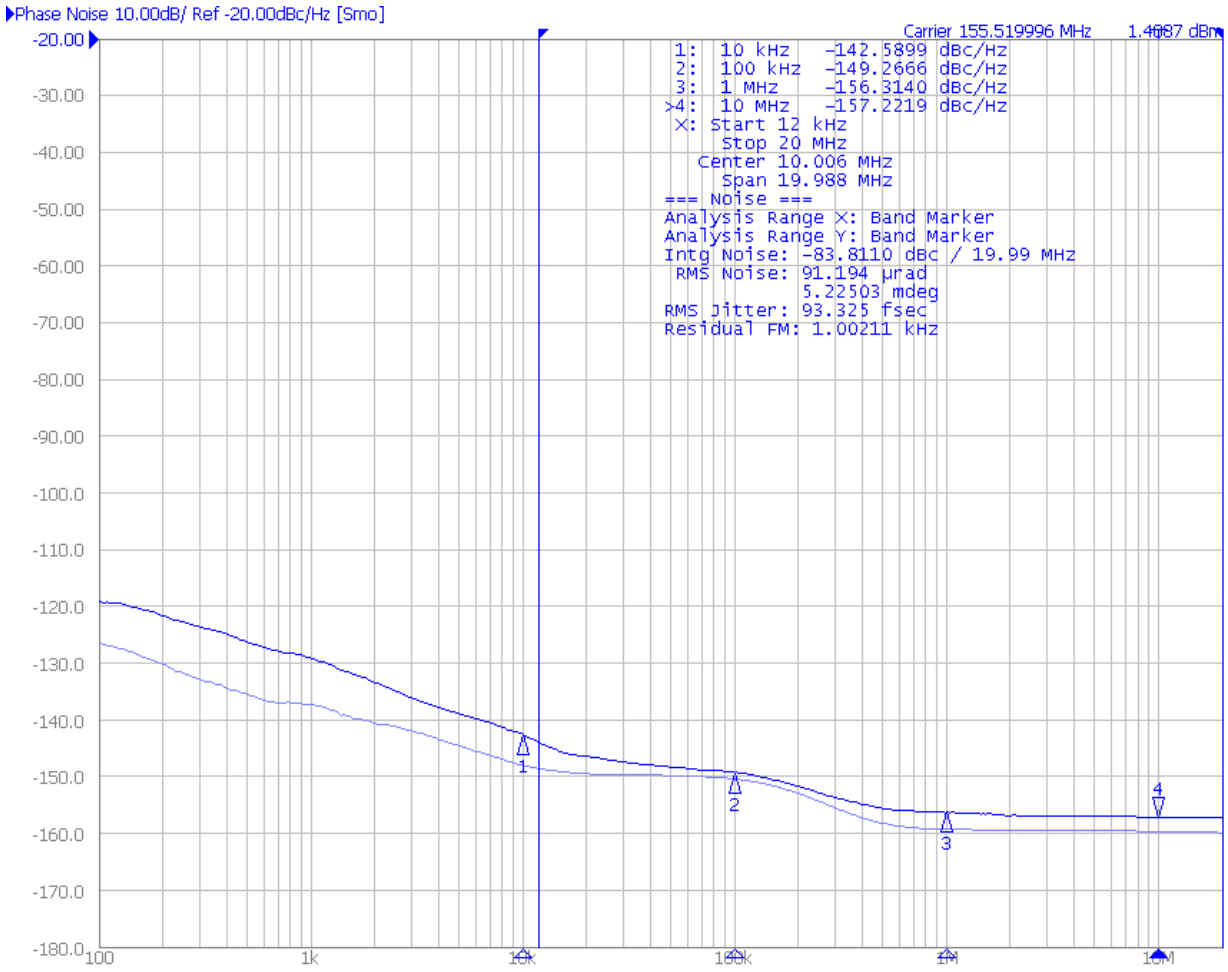



**Figure 6. For 155.52 MHz carrier, the NB3N853501E Additive Phase Noise (dBc/Hz) verses SSB Offset Frequency (Hz) Integrated Jitter from 12 kHz to 20 MHz (Upper Heavy Line) is 93.3 fs RMS. The E8663B Source Generator Additive Phase Noise (Lower Light Line) is 70.1 fs RMS. Where $t_{JIT} = \sqrt{(t_{JITouput})^2 - (t_{JITinput})^2} = 61.6$ fs**

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NB3N853501EDTR2G | TSSOP−20<br>(Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT**: www.onsemi.com/support
**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales