

# 2.5 V/3.3 V, 5 Gb/s Multi Level Clock/Data Input to CML Driver/Receiver/Buffer/Translator with Internal Termination

## NB4L16M

### Description

The NB4L16M is a differential driver/receiver/buffer/translator which can accept LVPECL, LVDS, CML, HSTL, LVCMOS/LVTTL and produce 400 mV CML output. The device is capable of receiving, buffering, and translating a clock or data signal that is as small as 75 mV operating up to 3.5 GHz or 5.0 Gb/s, respectively. As such, it is ideal for SONET, GigE, Fiber Channel and backplane applications (see Table 6 and Figures 20, 21, 22, and 23).

Differential inputs incorporate internal 50  $\Omega$  termination resistors and accept LVPECL (Positive ECL), LVTTL/LVCMOS, CML, HSTL or LVDS. The differential 16 mA CML output provides matching internal 50  $\Omega$  termination, and 400 mV output swing when externally receiver terminated, 50  $\Omega$  to  $V_{CC}$  (see Figure 19). These features provide transmission line termination on chip, at the receiver and driver end, eliminating any use of additional external components.

The  $V_{BB}$ , an internally generated voltage supply, is available to this device only. For single-ended input configuration, the unused complementary differential input is connected to  $V_{BB}$  as a switching reference voltage. The  $V_{BB}$  reference output can be used also to re-bias capacitor coupled differential or single-ended output signals. For the capacitor coupled input signals,  $V_{BB}$  should be connected to the  $V_{TD}$  pin and bypassed to ground with a 0.01  $\mu$ F capacitor. When not used  $V_{BB}$  should be left open.

This device is housed in a 3x3 mm 16 pin QFN package. Application notes, models, and support documentation are available at [www.onsemi.com](http://www.onsemi.com).

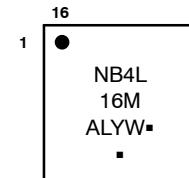
### Features

- Maximum Input Clock Frequency up to 3.5 GHz
- Maximum Input Data Rate up to 5.0 Gb/s
- < 0.7 ps Maximum Clock RMS Jitter
- < 10 ps Maximum Data Dependent Jitter at 2.5 Gb/s
- 220 ps Typical Propagation Delay
- 60 ps Typical Rise and Fall Times
- CML Output with Operating Range:
  - ♦  $V_{CC} = 2.375$  V to 3.6 V with  $V_{EE} = 0$  V
- CML Output Level (400 mV Peak-to-Peak Output), Differential Output Only
- 50  $\Omega$  Internal Input and Output Termination Resistors
- Functionally Compatible with Existing 2.5 V / 3.3 V LVEL, LVEP, EP, and SG Devices
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



QFN-16  
MN SUFFIX  
CASE 485G-01

### MARKING DIAGRAM\*



- A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 W = Work Week  
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note [AND8002/D](#).

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NB4L16MMNG	QFN-16 (Pb-Free)	123 Units/Tube
NB4L16MMNR2G	QFN-16 (Pb-Free)	3000/Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# NB4L16M

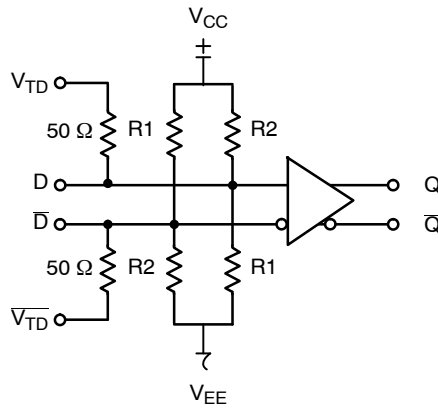


Figure 1. Functional Block Diagram

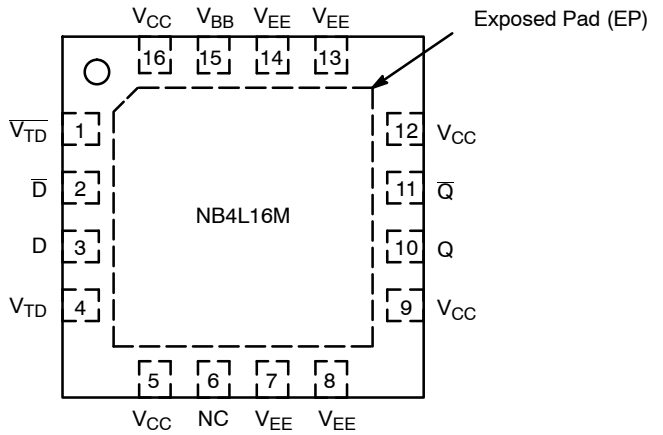


Figure 2. Pin Configuration (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	$\overline{V_{TD}}$	-	Internal 50 $\Omega$ termination pin. See Table 4 (Note 1).
2	$\overline{D}$	LVPECL, CML, HSTL, LVCMOS, LVDS, LVTTL Input	Inverted differential input. Internal 36.5 k $\Omega$ to $V_{CC}$ and 73 k $\Omega$ to $V_{EE}$ (Note 1).
3	D	LVPECL, CML, HSTL, LVCMOS, LVDS, LVTTL Input	Non-inverted differential input. Internal 73 k $\Omega$ to $V_{CC}$ and 36.5 k $\Omega$ to $V_{EE}$ (Note 1).
4	$V_{TD}$	-	Internal 50 $\Omega$ termination pin. See Table 4. (Note 1)
15	$V_{BB}$	-	Internally generated reference voltage supply.
6	NC		No Connect pin. The No Connect (NC) pin is electrically connected to the die and MUST be left open.
10	Q	CML Output	Non-inverted differential output. Typically receiver terminated with 50 $\Omega$ resistor to $V_{CC}$ .
11	$\overline{Q}$	CML Output	Inverted differential output. Typically receiver terminated with 50 $\Omega$ resistor to $V_{CC}$ .
7, 8, 13, 14	$V_{EE}$	-	Negative supply voltage
5, 9, 12, 16	$V_{CC}$	-	Positive supply voltage
-	EP	-	Exposed pad (EP). EP on the package bottom is thermally connected to the die for improved heat transfer out of the package. The pad is not electrically connected to the die, but is recommended to be soldered to $V_{EE}$ on the PC Board.

1. In the differential configuration when the input termination pins ( $V_{TD}$ ,  $\overline{V_{TD}}$ ) are connected to a common termination voltage and if no signal is applied on D/ $\overline{D}$  input then the device will be susceptible to self-oscillation.

# NB4L16M

**Table 2. ATTRIBUTES**

Characteristics	Value
Input Default State Resistors R1 R2	37.5 k $\Omega$ 73 k $\Omega$
ESD Protection Human Body Model Machine Model Charged Device Model	> 2 kV > 200 V > 1 kV
Moisture Sensitivity (Note 1)	Pb-Free Pkg
QFN-16	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	157
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note [AND8003/D](#).

**Table 3. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
$V_{CC}$	Positive Power Supply	$V_{EE} = 0\text{ V}$		6	V
$V_{EE}$	Negative Power Supply	$V_{CC} = 0\text{ V}$		-6	V
$V_I$	Positive Input Negative Input	$V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$	$V_I = V_{CC}$ $V_I = V_{EE}$	6 -6	V
$V_{INPP}$	Differential Input Voltage	$ D - \bar{D} $		$ V_{CC} - V_{EE} $	V
$I_{IN}$	Input Current Through $R_T$ (50 $\Omega$ Resistor)	Static Surge		45 80	mA
$I_{OUT}$	Output Current	Continuous Surge		25 50	mA
$I_{BB}$	$V_{BB}$ Sink/Source			$\pm 0.5$	mA
$T_A$	Operating Temperature Range			-40 to +85	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range			-65 to +150	$^{\circ}\text{C}$
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient) (Note 1)	0 lfpm 500 lfpm	QFN-16	42 35	$^{\circ}\text{C/W}$
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	1S2P (Note 1)	QFN-16	4	$^{\circ}\text{C/W}$
$T_{sol}$	Wave Solder (Pb-Free)			265	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. JEDEC standard multilayer board – 1S2P (1 signal, 2 power) with 8 filled thermal vias under exposed pad.

# NB4L16M

**Table 4. DC CHARACTERISTICS, CLOCK INPUTS, CML OUTPUTS** ( $V_{CC} = 2.375 \text{ V to } 3.8 \text{ V}$ ,  $V_{EE} = 0 \text{ V}$ ,  $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ )

Symbol	Characteristic	Min	Typ	Max	Unit
$I_{CC}$	Power Supply Current (Inputs and Outputs Open)	30	45	55	mA
$V_{OH}$	Output HIGH Voltage (Note 1)	$V_{CC} - 40$	$V_{CC} - 10$	$V_{CC}$	mV
$V_{OL}$	Output LOW Voltage (Note 1)	$V_{CC} - 500$	$V_{CC} - 400$	$V_{CC} - 300$	mV

**DIFFERENTIAL INPUT DRIVEN SINGLE-ENDED** (Figures 15 and 17)

$V_{TH}$	Input Threshold Reference Voltage Range (Note 3)	1050		$V_{CC} - 150$	mV
$V_{IH}$	Single-ended Input HIGH Voltage	$V_{th} + 150$		$V_{CC}$	mV
$V_{IL}$	Single-ended Input LOW Voltage	$V_{EE}$		$V_{th} - 150$	mV
$V_{BB}$	Internally Generated Reference Voltage Supply (Loaded with $-100 \mu\text{A}$ )	$V_{CC} - 1500$	$V_{CC} - 1400$	$V_{CC} - 1300$	mV

**DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY** (Figures 16 and 18)

$V_{IHD}$	Differential Input HIGH Voltage	1200		$V_{CC}$	mV
$V_{ILD}$	Differential Input LOW Voltage	$V_{EE}$		$V_{CC} - 150$	mV
$V_{CMR}$	Input Common Mode Range (Differential Configuration)	950		$V_{CC} - 75$	mV
$V_{ID}$	Differential Input Voltage ( $V_{IHD} - V_{ILD}$ )	150		$V_{CC} - V_{EE}$	mV
$I_{IH}$	Input HIGH Current ( $V_{TD}/\sqrt{V_{TD}}$ Open) D D	0 0	100 50	150 100	$\mu\text{A}$
$I_{IL}$	Input LOW Current ( $V_{TD}/\sqrt{V_{TD}}$ Open) D D	-100 -150	-50 -100	0 0	$\mu\text{A}$
$R_{TIN}$	Internal Input Termination Resistor	40	50	60	$\Omega$
$R_{TOUT}$	Internal Output Termination Resistor	40	50	60	$\Omega$
$R_{Temp}$ Coef	Internal I/O Termination Resistor Temperature Coefficient		16		$\text{m}\Omega/^\circ\text{C}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. CML outputs require  $50 \Omega$  receiver termination resistors to  $V_{CC}$  for proper operation. See Figure 14.
2. Input and output parameters vary 1:1 with  $V_{CC}$ .
3.  $V_{th}$  is applied to the complementary input when operating in single-ended mode.
4.  $V_{CMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{CMRmax}$  varies 1:1 with  $V_{CC}$ . The  $V_{CMR}$  range is referenced to the most positive side of the differential input signal.

# NB4L16M

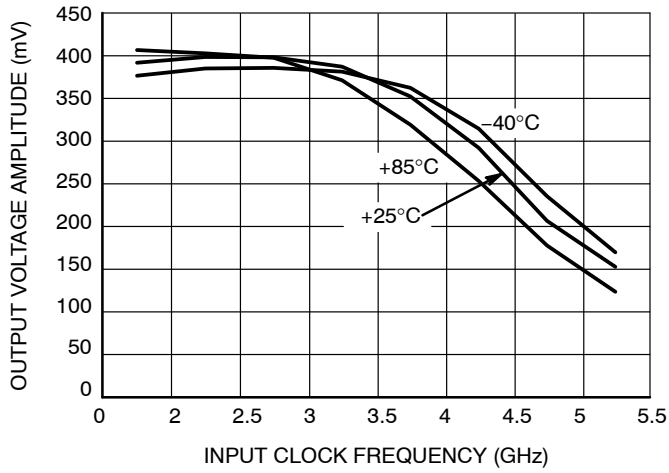
**Table 5. AC CHARACTERISTICS** ( $V_{CC} = 2.375\text{ V}$  to  $3.8\text{ V}$ ,  $V_{EE} = 0\text{ V}$ ; (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{OUTPP}$	Output Voltage Amplitude (@ $V_{INPPmin}$ ) (Figures 3 and 4) $f_{in} \leq 3.5\text{ GHz}$ $f_{in} \leq 4.5\text{ GHz}$	280 150	400 300		280 150	400 300		280 150	400 300		mV
$f_{DATA}$	Maximum Operating Data Rate	3.5	5.0		3.5	5.0		3.5	5.0		Gb/s
$t_{PLH}$ , $t_{PHL}$	Propagation Delay to Output Differential @ 0.5 GHz (Figure 6)	175	215	265	175	220	265	175	225	265	ps
$t_{SKEW}$	Duty Cycle Skew (Note 2) Device-to-Device Skew (Note 6)		2.0 6.0	10 90		2.0 6.0	10 90		2.0 6.0	10 90	ps
$t_{JITTER}$	RMS Random Clock Jitter (Note 4) $f_{in} \leq 4.5\text{ GHz}$ Peak-to-Peak Data Dependent Jitter (Note 5) $f_{DATA} = 2.5\text{ Gb/s}$ $f_{DATA} = 3.5\text{ Gb/s}$ $f_{DATA} = 5.0\text{ Gb/s}$		0.2 1.5 2.0 9.0	0.7 10 12 25		0.2 1.5 2.0 9.0	0.7 10 12 25		0.2 1.5 2.0 9.0	0.7 10 12 25	ps
$V_{INPP}$	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 3)	75		$V_{CC}$ $-V_{EE}$	75		$V_{CC}$ $-V_{EE}$	75	$V_{CC}$ $-V_{EE}$		mV
$t_r$ $t_f$	Output Rise/Fall Times @ 0.5 GHz (Figure 5) (20% – 80%)		60	90		60	90		60	90	ps

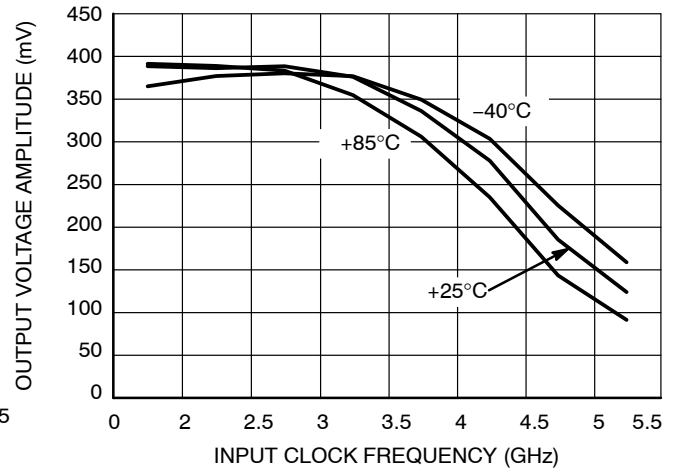
NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Measured by forcing  $V_{INPP(MIN)}$  from a 50% duty cycle clock source. All loading with an external  $R_L = 50\ \Omega$  to  $V_{CC}$ . Input edge rates 40 ps (20% – 80%). See Figure 12 and 14.
2. Duty cycle skew is measured between differential outputs using the deviations of the sum of  $T_{pw-}$  and  $T_{pw+}$  @ 0.5 GHz.
3.  $V_{INPP(MAX)}$  cannot exceed  $V_{CC} - V_{EE}$ . Input voltage swing is a single-ended measurement operating in differential mode. See Figure 11.
4. Additive RMS jitter with 50% duty cycle input clock signal.
5. Additive peak-to-peak data dependent jitter with NRZ input data signal, PRBS 2<sup>23</sup>-1 and K28.7 pattern. See Figures 7, 8, 9, 10, 11 and 12.
6. Device-to-device skew is measured between outputs under identical transition @ 0.5 GHz.

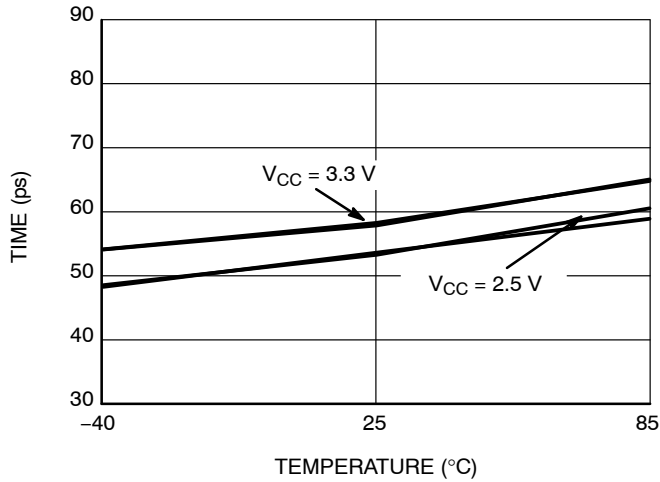
TYPICAL OPERATING CHARACTERISTICS



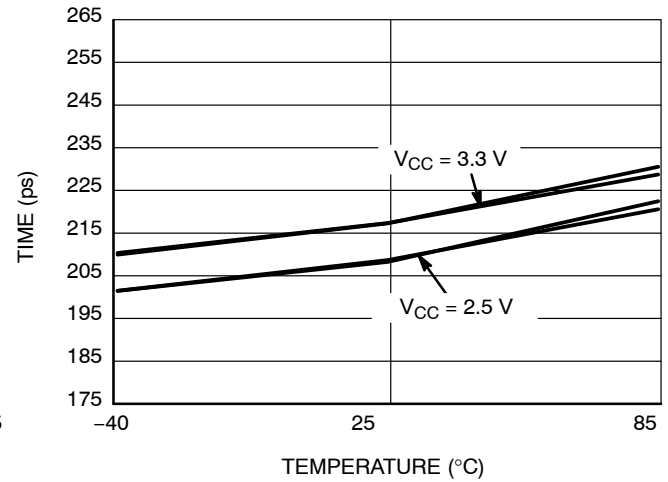
**Figure 3. Output Voltage Amplitude ( $V_{OUTPP}$ ) vs. Input Clock Frequency ( $f_{in}$ ) and Temperature at 3.3 V Power Supply**



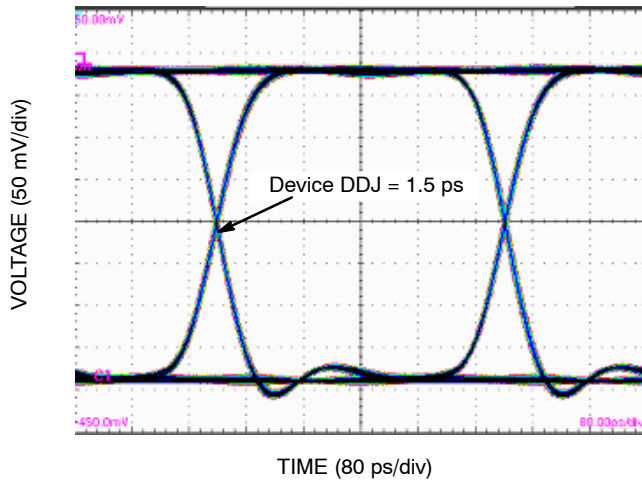
**Figure 4. Output Voltage Amplitude ( $V_{OUTPP}$ ) vs Input Clock Frequency ( $f_{in}$ ) and Temperature at 2.5 V Power Supply**



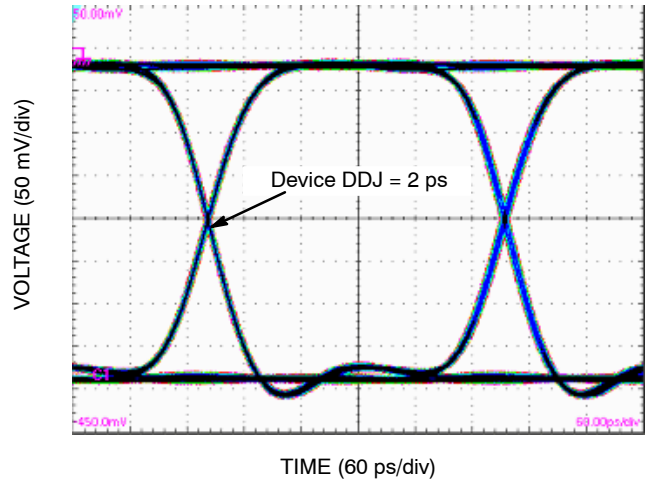
**Figure 5. Rise/Fall Time vs Temperature and Power Supply**



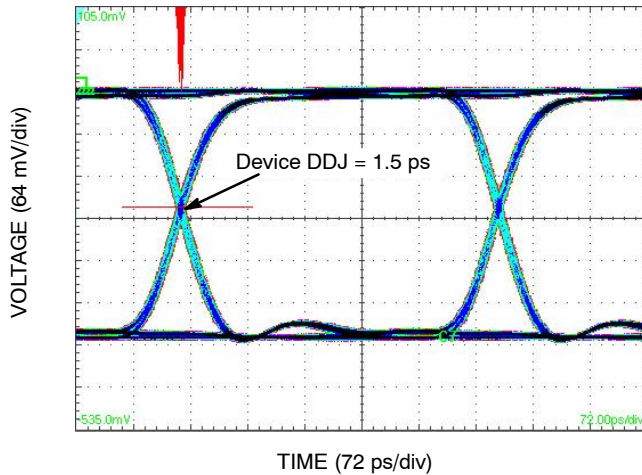
**Figure 6. Propagation Delay vs Temperature and Power Supply**



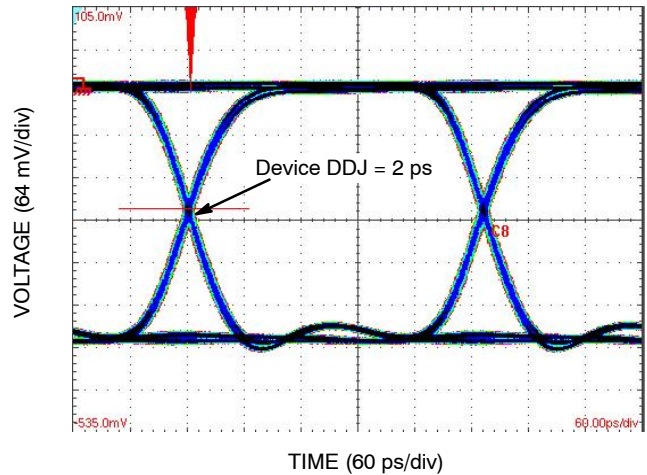
**Figure 7. Typical Output Waveform at 2.488 Gb/s with PRBS  $2^{23}-1$  ( $V_{INPP} = 75$  mV; Input Signal DDJ = 12 ps)**



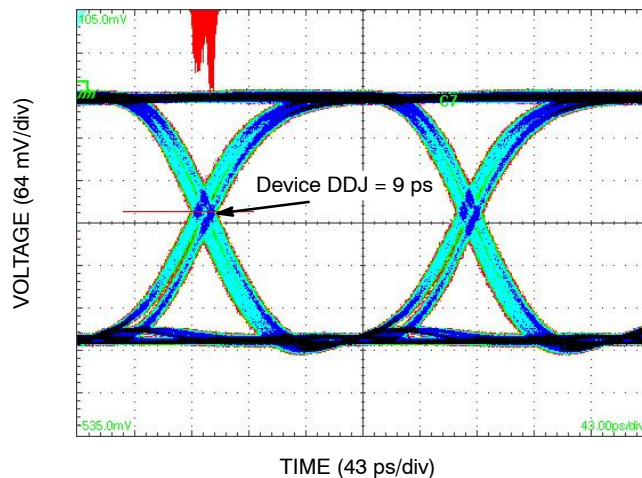
**Figure 8. Typical Output Waveform at 3.2 Gb/s with PRBS  $2^{23}-1$  ( $V_{INPP} = 75$  mV; Input Signal DDJ = 12 ps)**



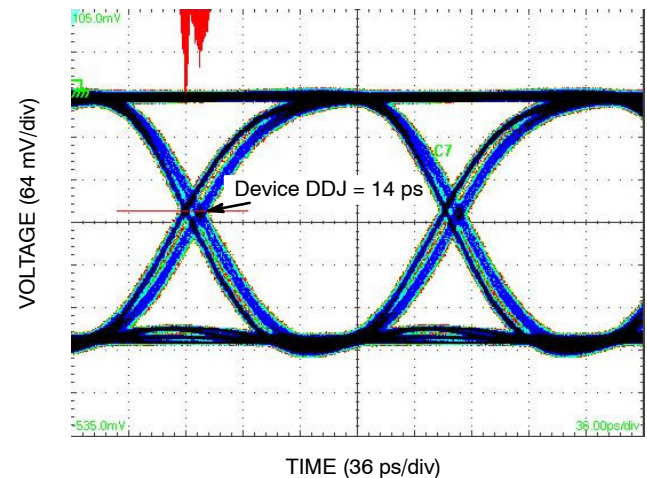
**Figure 9. Typical Output Waveform at 2.488 Gb/s with PRBS  $2^{23}-1$  ( $V_{INPP} = 400$  mV; Input Signal DDJ = 12 ps)**



**Figure 10. Typical Output Waveform at 3.2 Gb/s with PRBS  $2^{23}-1$  ( $V_{INPP} = 400$  mV; Input Signal DDJ = 12 ps)**



**Figure 11. Typical Output Waveform at 5 Gb/s with PRBS  $2^{23}-1$  ( $V_{INPP} = 400$  mV; Input Signal DDJ = 13 ps)**



**Figure 12. Typical Output Waveform at 6.125 Gb/s with PRBS  $2^{23}-1$  ( $V_{INPP} = 400$  mV; Input Signal DDJ = 15 ps)**

# NB4L16M

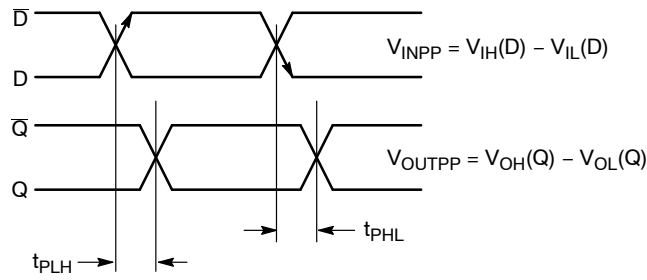


Figure 13. AC Reference Measurement

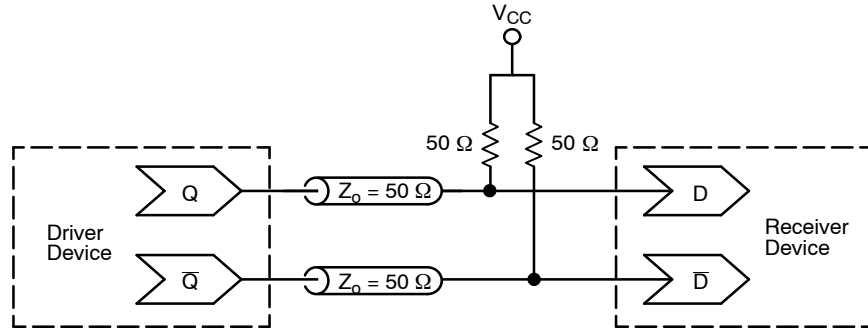


Figure 14. Typical Termination for Output Driver and Device Evaluation

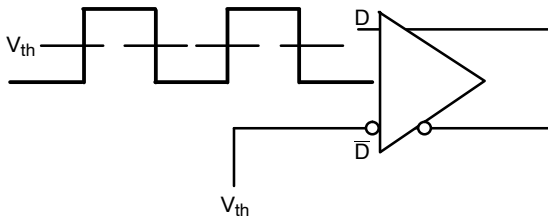


Figure 15. Differential Input Driven Single-Ended

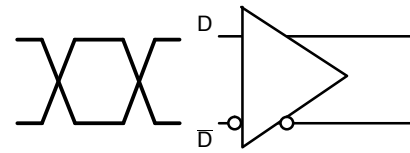


Figure 16. Differential Inputs Driven Differentially

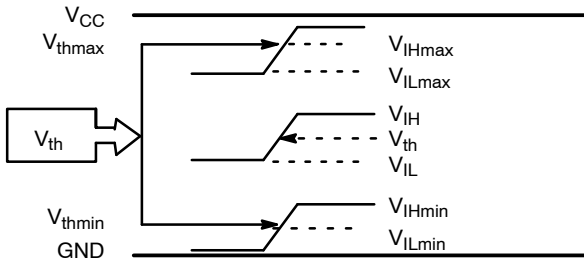


Figure 17.  $V_{th}$  Diagram

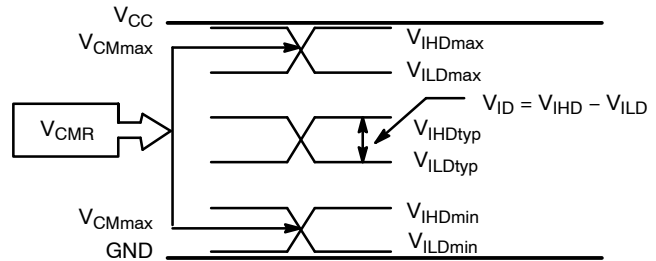


Figure 18.  $V_{CMR}$  Diagram

NOTE:  $V_{EE} + V_{IN} + V_{CC}$ ;  $V_{IH} > V_{IL}$



## NB4L16M

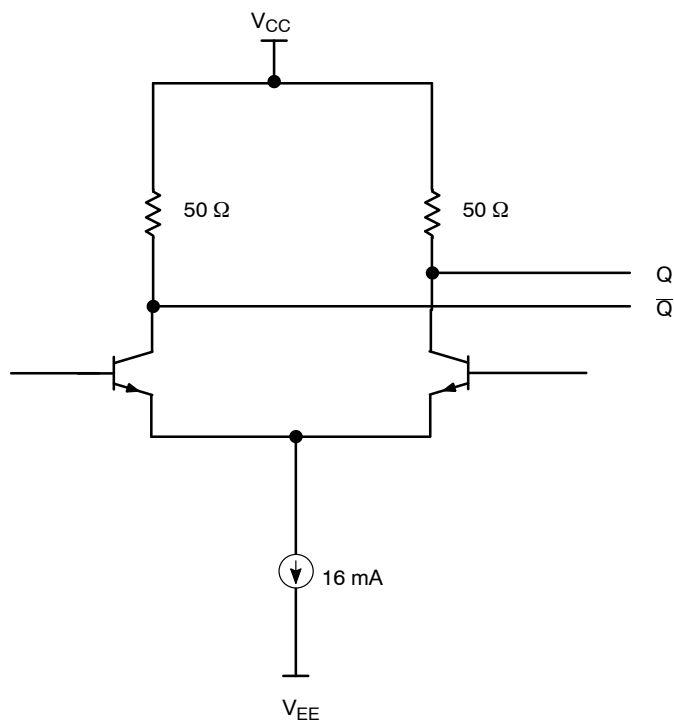


Figure 19. CML Output Structure

Table 6. INTERFACING OPTIONS

INTERFACING OPTIONS	CONNECTIONS
CML	Connect $V_{TD}$ and $\overline{V_{TD}}$ to $V_{CC}$
LVDS	Connect $V_{TD}$ and $\overline{V_{TD}}$ Together
AC-COUPLED	Bias $V_{TD}$ and $\overline{V_{TD}}$ Inputs within Common Mode Range ( $V_{CMR}$ )
RSECL, PECL, NECL	Standard ECL Termination Techniques
LVTTL, LVCMOS	An External Voltage ( $V_{THR}$ ) should be applied to the unused complementary differential input. Nominal $V_{THR}$ is 1.5 V for LVTTL and $V_{CC}/2$ for LVCMOS inputs. This voltage must be within the $V_{THR}$ specification.

# APPLICATION INFORMATION

All NB4L16M inputs can accept LVPECL, CML, LVTTTL, LVCMOS and LVDS signal levels. The limitations for differential input signal (LVDS, PECL, or CML) are minimum input swing of 75 mV and the maximum input swing of 2500 mV. Within these conditions, the input voltage can range from  $V_{CC}$  to 1.2 V. Examples interfaces are illustrated below in a 50  $\Omega$  environment ( $Z = 50 \Omega$ ).

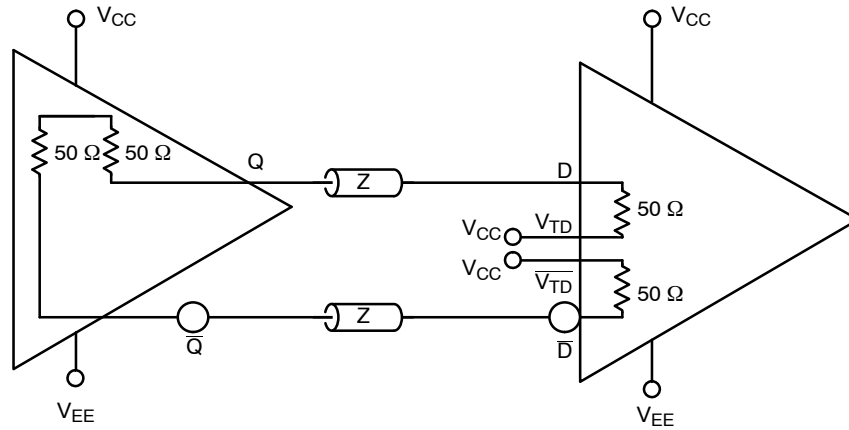


Figure 20. CML to CML Interface

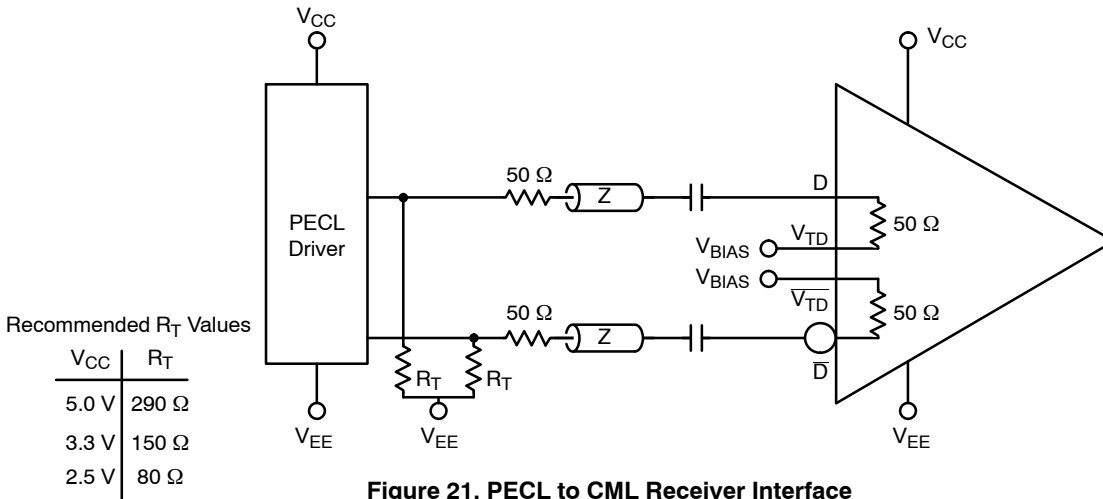


Figure 21. PECL to CML Receiver Interface

# NB4L16M

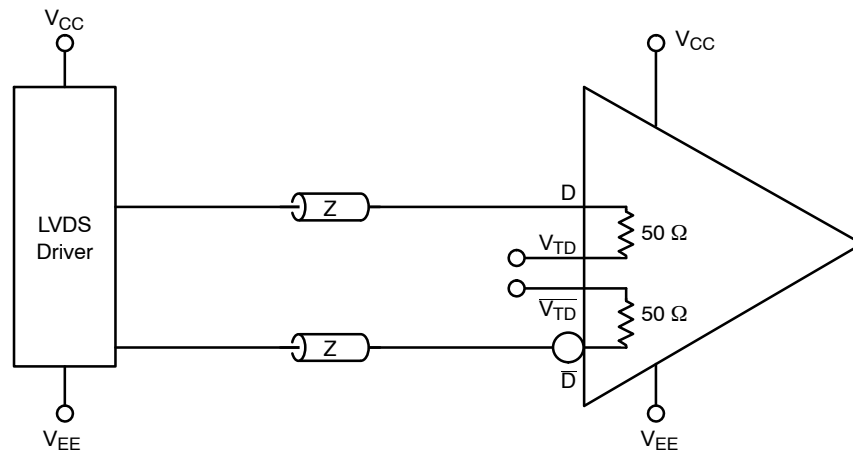


Figure 22. LVDS to CML Receiver Interface

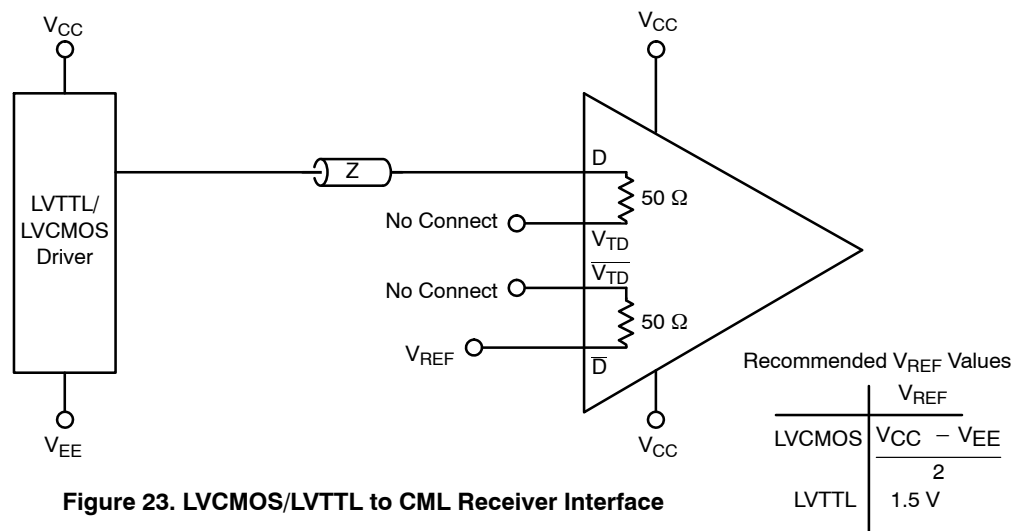


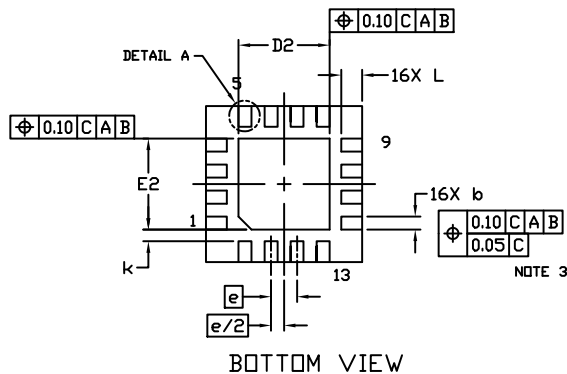
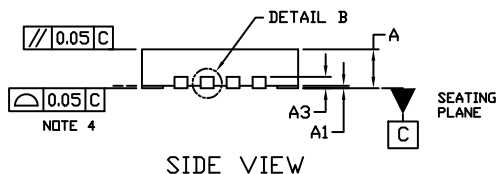
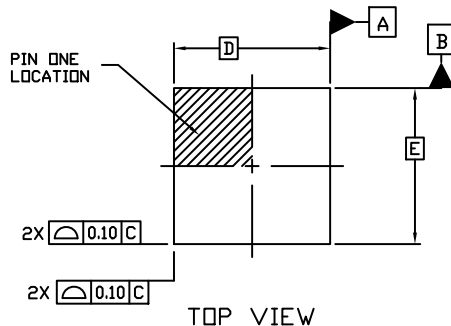
Figure 23. LVCMOS/LVTTL to CML Receiver Interface



SCALE 2:1

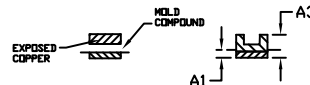
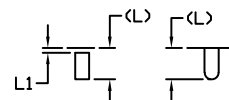
**QFN16 3x3, 0.5P**  
CASE 485G  
ISSUE G

DATE 08 OCT 2021



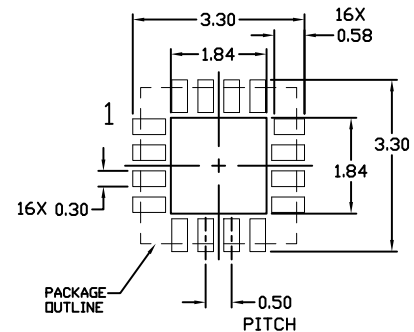
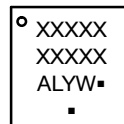
## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.


DETAIL B  
ALTERNATE  
CONSTRUCTIONS

DETAIL A  
ALTERNATE TERMINAL  
CONSTRUCTIONS

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3	0.20 REF		
b	0.18	0.24	0.30
D	3.00 BSC		
D2	1.65	1.75	1.85
E	3.00 BSC		
E2	1.65	1.75	1.85
e	0.50 BSC		
k	0.18 TYP		
L	0.30	0.40	0.50
L1	0.00	0.08	0.15

## MOUNTING FOOTPRINT


**GENERIC  
MARKING DIAGRAM\***


XXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

<b>DOCUMENT NUMBER:</b>	<b>98AON04795D</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>QFN16 3X3, 0.5P</b>	<b>PAGE 1 OF 1</b>

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at  
[www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)