NCP1381, NCP1382

Low-Standby High Performance PWM Controller

Housed in a SO-14 package, the NCP1381/82 includes everything needed to build rugged and efficient Quasi-Resonant (QR) Switching Power Supplies. When powered by a front-end Power Factor Correction circuitry, the NCP1381/82 automatically disconnects the PFC controller in low output loading conditions (with an adjustable level), thus improving the standby power. This is particularly well suited for medium to high power offline applications, e.g. notebook adapters. When the current setpoint falls below a given value, e.g. the output power demand diminishes, the IC automatically enters the so-called skip cycle mode and provides excellent efficiency at light loads. Because this occurs at an adjustable low peak current together with a proprietary Soft-Skip™ technique, no acoustic noise takes place. Skip cycle also offers the ability to easily select the maximum switching frequency at which foldback and standby take place.

The NCP1381/82 also features several efficient protection options like a) a short-circuit / overload detection independent of the auxiliary voltage b) an auto-recovery brown-out detection and c) an input to externally latch the circuit in case of Overvoltage Protection or Over Temperature Protection.

Features

- Current-Mode Quasi-Resonant Operation
- Adjustable Line Over Power Protection
- Extremely Low Startup Current of 15 μA Maximum
- Soft-Skip Cycle Capability at Adjustable Peak Currents
- Plateau Sensing Overvoltage
- Brown-Out Protection
- Maximum t_{ON} Limitation
- Overpower Protection by current Sense Offset
- Internal 5 ms Soft-Start Management
- Short-Circuit Protection Independent from Auxiliary Level
- External Latch Input Pin for an OTP Signal
- Go-To-Standby Signal for the PFC Front Stage
- True Frequency (t_{ON} + t_{OFF}) Clamp Circuit
- Low and Noiseless, No-Load Standby Power
- Internal Leading Edge Blanking
- +500 mA / -800 mA Peak Current Drive Capability
- 5 V / 10 mA Reference Voltage
- These are Pb-Free Devices

Typical Applications

- High Power AC/DC Adapters for Notebooks, etc
- Offline Battery Chargers
- Set-Top Boxes Power Supplies, TV, Monitors, etc

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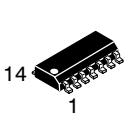
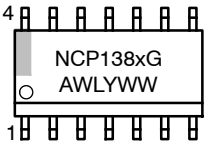
HIGH PERFORMANCE QR CONTROLLER FEATURING PFC SHUTDOWN

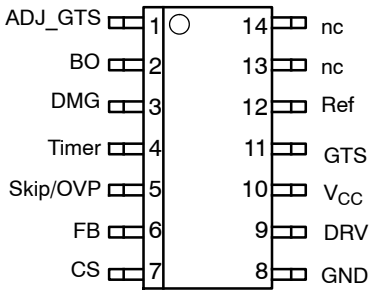
MARKING DIAGRAM



SOIC-14
D SUFFIX
CASE 751A



NCP138xG = Specific Device Code
x = 1 or 2
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package



ORDERING INFORMATION

Device	Package	Shipping†
NCP1381DR2G	SOIC-14 (Pb-Free)	2500/Tape & Reel
NCP1382DR2G	SOIC-14 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL APPLICATION EXAMPLE

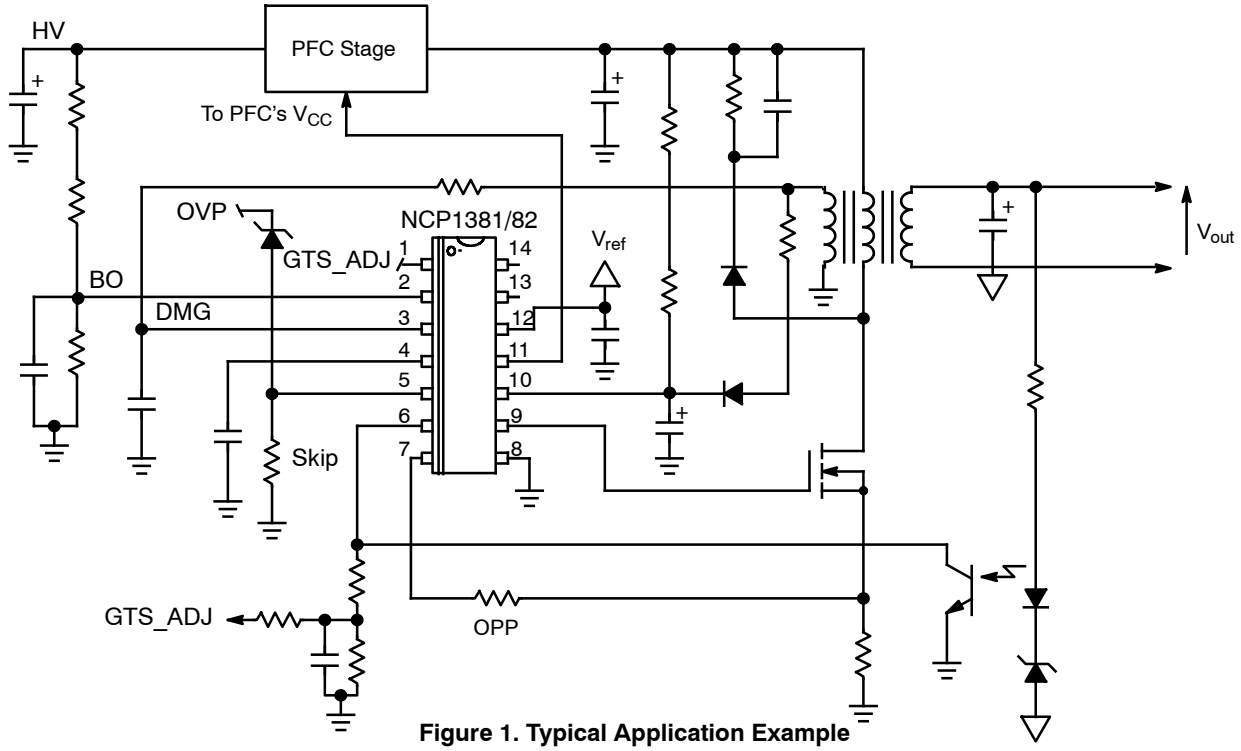


Figure 1. Typical Application Example

PIN FUNCTION DESCRIPTION

Pin#	Symbol		Description
1	GTS_ADJ	GTS Level Adjustment	An internal comparator senses the signal applied to this pin (typically a portion of F_B signal) to detect the standby condition for GTS.
2	BO	Brown−out	By connecting this pin to a resistive divider, the controller ensures operation at a safe mains level.
3	DMG	Detects the Zero Voltage Crossing Point	This pin detects the core reset event but also permanently senses the Flyback plateau, offering a clean OVP detection.
4	Timer	Fault Timer	Connecting a capacitor to this pin adjusts the fault timer.
5	Skip/OVP	Adjust the Skip Level	This pin alters the default skip cycle level and offers a mean to latchoff the controller when externally brought above 4 V.
6	FB	Feedback Signal	An optocoupler collector pulls this pin down to regulate. When the current setpoint falls below an adjustable level, the controller skips cycles.
7	CS	Current Sense Pin	This pin cumulates two different functions: the standard sense function plus an adjustable offset voltage providing the adequate level of Overpower Protection.
8	GND	The IC Ground	−
9	DRV	The Driver Output	With a drive capability of ±500 mA/800 mA, the NCP1381 can drive large Q_g MOSFETs.
10	V_{CC}	V_{CC} Input	The controller accepts voltages up to 20 V and features an UVLO of 10 V typical.
11	GTS	Directly Powers the PFC Frontend Stage	This pin directly powers the PFC controller by routing the PWM V_{CC} to the PFC V_{CC}. In standby (defined by GTS_ADJ), fault and BO conditions, this pin is open and the PFC is no longer supplied.
12	Reference	Reference Voltage	This pin offers a 5 V reference voltage sourcing up to 10 mA.
13	NC	−	Not Connected
14	NC	−	Not Connected

INTERNAL CIRCUIT ARCHITECTURE

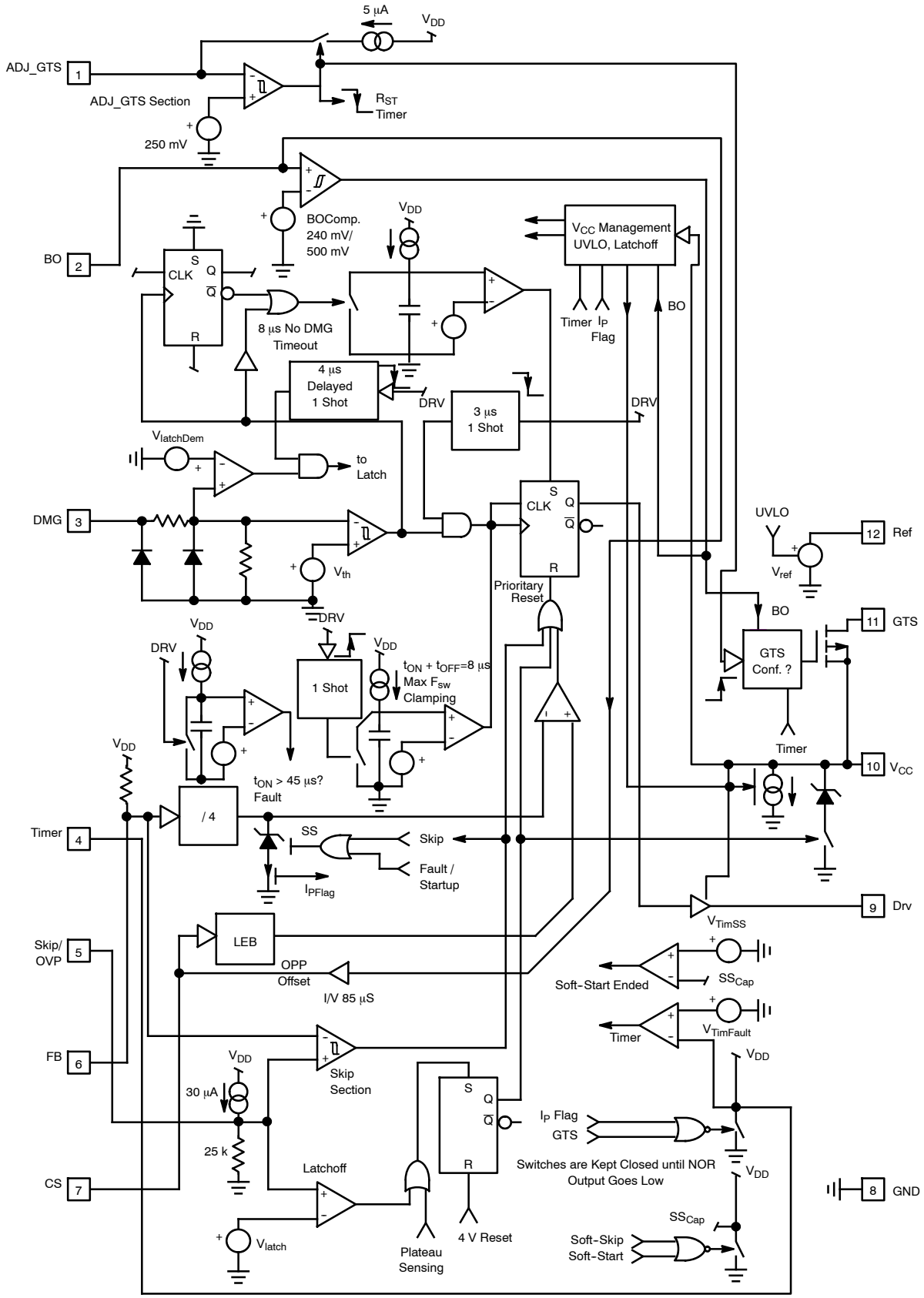


Figure 2. Internal Circuit Architecture

MAXIMUM RATINGS TABLE

Symbol	Rating	Value	Unit
V_{supply}	Maximum Power Supply Voltage on Pin 10 (V_{CC}), Pin 9 (DRV), and Pin 11 (GTS)	20	V
	Maximum Current in Pin 10 (V_{CC})	±30	mA
	Maximum Current in Pin 11 (GTS)	±20	mA
	Maximum Current in Pin 9 (DRV)	±1	A
	Power Supply Voltage on all Other Pins Except Pin 10 (V_{CC}), Pin 9 (DRV), Pin 3 (DMG) and Pin 11 (GTS)	−0.3 to 5	V
	Maximum Current Into All Other Pins Except Pin 10 (V_{CC}), Pin 9 (DRV) and Pin 11 (GTS)	±10	mA
I_{dem}	Maximum Current in Pin 3 (DMG), When 10 V ESD Zener is Activated	+3 / −3	mA
$R_{\theta J-A}$	Thermal Resistance Junction−to−Air, SO−14	150	°C/W
TJ_{MAX}	Maximum Junction Temperature	150	°C
	Storage Temperature Range	−60 to +150	°C
	ESD Capability, Human Body Model per MIL−STD−883, Method 3015 (All Pins Except Ref)	2	kV
	ESD Capability, Human Body Model per MIL−STD−883, Method 3015 (Ref Pin)	1.8	kV
	ESD Capability, Machine Model	200	V

NOTE: This device contains latchup protection and exceeds 100 mA per JEDEC standard JESD78.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = 0°C to +125°C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
SUPPLY SECTION						
VCC_{ON}	Turn−on Threshold Level, V_{CC} Going Up	10	13	15	17.9	V
VCC_{OFF}	Minimum Operating Voltage After Turn−on	10	9	10	11	V
VCC_{latch}	V_{CC} Decreasing Level at Which the Latchoff Phase Ends	10	−	7	−	V
VCC_{reset}	V_{CC} Level at Which the Internal Logic Gets Reset	10	−	4	−	V
$I_{startup}$	Startup Current (V_{CC} < VCC_{ON})	10	−	2	15	μA
I_{CC1}	Internal IC Consumption, No Output Load on Pin 9, F_{SW} = 60 kHz	10	−	1.4	1.8	mA
I_{CC2}	Internal IC Consumption, 1 nF Output Load on Pin 9, F_{SW} = 60 kHz	10	−	2.1	2.6	mA
I_{CC3}	Internal IC Consumption, Latchoff Phase	10	−	1.4	−	mA
DRIVE OUTPUT						
T_r	Output Voltage Rise−Time @ C_L = 1 nF, 10−90% of Output Signal	9	−	15	−	ns
T_f	Output Voltage Fall−Time @ C_L = 1 nF, 10−90% of Output Signal	9	−	15	−	ns
R_{OH}	Source Resistance	9	−	9	−	Ω
R_{OL}	Sink Resistance	9	−	8	−	Ω
CURRENT COMPARATOR						
I_{IB}	Input Bias Current @ 1 V Input Level on Pin 7	7	−	0.02	−	μA
I_{Limit}	Maximum Internal Current Setpoint at V_{BO} = 0	7	0.75	0.8	0.85	V
G_m	Transconductance Amplifier Offsetting CS at V_{BO} = 2 V	7	70	85	100	μS
T_{DELCS}	Propagation Delay from CS Detected to Gate Turned off (Pin 9 Loaded by 1 nF)	7	−	90	−	ns
T_{LEB}	Leading Edge Blanking Duration	7	300	370	−	ns
S_{Start}	Typical Internal Soft−start Period at Startup	−	2.5	4.0	6.0	ms
S_{skip}	Typical Internal Soft−start period when Leaving Skip	−	100	175	250	μs

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = 0°C to +125°C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
GO−TO−STANDBY						
R_{GTS}	Pin 11 Output Impedance (or R_{dson} between Pin 10 and Pin 11 when SW is Closed)	11	−	15	−	Ω
R_{skip}	Skip Adjustment Output Impedance	5	17	25	35	kΩ
V_{skip}	Default Skip Cycle Level	5	−	800	−	mV
Hyst_ratio	Ratio Between the Skip Level and the Skip Comparator Hysteresis	−	−	3.4	−	−
ADJ_GTS	Threshold of the ADJ_GTS Comparator	1	220	250	280	mV
I_{hyst}	Internal Current Source that Creates an Adjustable Hysteresis to the ADJ_GTS Comparator	1	4.0	5.0	6.0	μA
DEMAGNETIZATION DETECTION BLOCK						
V_{th}	Input Threshold Voltage (V_{pin} 3 Decreasing)	3	30	50	80	mV
V_H	Hysteresis (V_{pin} 3 Increasing)	3	−	30	−	mV
VC_H VC_L	Input Clamp Voltage High State (I_{pin} 3 = 3.0 mA) Low State (I_{pin} 3 = −3.0 mA)	 3 3	 9 −0.9	 10 −0.7	 12 −0.5	 V V
T_{dem}	DMG Propagation Delay	3	−	200	−	ns
C_{par}	Internal Input Capacitance at V_{pin} 3 = 1 V	3	−	10	−	pF
R_{down}	Internal Pulldown Resistor	3	20	30	45	kΩ
T_{blank}	Internal Blanking Delay after T_{ON}	3	−	3.5	−	μs
$T_{sw-(min)}$	Frequency Clamp, Minimum (T_{ON} + T_{OFF})	−	7.0	8.0	9.0	μs
FEEDBACK SECTION						
R_{up}	Internal Pullup Resistor	6	7.5	10	12.5	kΩ
I_{ratio}	Pin 6 to Current Setpoint Division Ratio (Maximum V_{FB} = 5 V)	−	−	4.0	−	
Ref	Voltage Reference, I_{load} = 1 mA	12	4.75	5.0	5.25	V
I_{ref}	Reference Maximum Output Current	12	10	−	−	mA
PROTECTIONS						
$V_{zenlatch}$	V_{CC} Limitation in Latched Fault Mode	10	−	6.0	−	V
Max_{tON}	Maximum On Time Duration	9	−	45	−	μs
I_{timer}	Timer Charging Current	4	7.0	10	13	μA
$V_{timfault}$	Timer Fault Validation Level	4	3.5	4.0	4.5	V
T_{delay}	Timeout Before Validating Short−circuit or GTS, C_t = 0.22 μF	−	−	90	−	ms
$V_{latchdem}$	Latching Level On the Demagnetization Input	3	3.7	4.1	4.5	V
T_{samp}	Sampling Time for $V_{latchdem}$ Detection after the End of the T_{ON}	3	−	4.0	−	μs
V_{latch}	Latchoff Level On the Skip Adjustment Pin NCP1381 NCP1382	5	3.15 2.25	3.5 2.5	3.85 2.75	V
$T_{DELLATCH}$	Propagation Delay from Latch Detected to Gate Turned Off (Pin 9 Loaded by 1 nF)	−	−	220	−	ns
VBO_{high}	Brown−out Level High	2	0.45	0.5	0.55	V
VBO_{low}	Brown−out Level Low	2	0.21	0.24	0.275	V
I_{BO}	Brown−out Pin Input Bias Current	2	−	0.04	−	μA
T_{SD}	Temperature Shutdown, Maximum Value	−	140	−	−	°C
TSD_{hyst}	Hysteresis While in Temperature Shutdown	−	−	30	−	°C

APPLICATION INFORMATION

The NCP1381/82 includes all necessary features to help building a rugged and safe switching power supply featuring an extremely low standby power. The below bullets detail the benefits brought by implementing the NCP1381/82 controller.

- *Current-mode operation with Quasi-Resonant Operation*: Implementing peak current mode control, the NCP1381/82 waits until the drain-source voltage crosses a minimum level. This is the quasi-resonance approach, minimizing both EMI radiations and capacitive losses.
- *Over Power Protection*: Using a voltage image of the bulk level, via the brown-out divider, the designer can select a resistor which, placed in series with the current sense information, provides an efficient line compensation method.
- *Frequency Clamp*: The controller monitors the sum of ton and toff, providing a real frequency clamp. Also the ton maximum duration is safely limited to 50 μs in case the peak current information is lost. If the maximum ton limit is reached, then the controller stops all pulses and enters a safe auto-recovery burst mode.
- *Blanking Time*: To prevent false tripping with energetic leakage spikes, the controllers includes a 3 μs blanking time after the toff event.
- *Go-to-Standby Signal for PFC Front Stage*: The NCP1381/82 includes an internal low impedance switch connected between Pin 10 (V_{CC}) and Pin 11 (GTS). The signal delivered by Pin 11 being of low impedance, it becomes possible to connect PFC's V_{CC} directly to this pin and thus avoid any complicated interface circuitry between the PWM controller and the PFC front-end section. In normal operation, Pin 11 routes the PWM auxiliary V_{CC} to the PFC circuit which is directly supplied by the auxiliary winding. When the SMPS enters skip-cycle at low output power levels, the controller detects and confirms the presence of the skip activity by monitoring the signal applied on its pin ADJ_GTS (typically F_B signal) and opens Pin 11, shutting down the front-end PFC stage. When this signal level increases, e.g. when the SMPS goes back to a normal output power, Pin 11 immediately (without delay) goes back to a low impedance state. Finally, in short-circuit conditions, the PFC is disabled to lower the stress applied to the PWM main switch.
- *Low Startup-Current*: Reaching a low no-load standby power represents a difficult exercise when the controller requires an external, lossy, resistor connected to the bulk capacitor. Due to a novel silicon architecture, the startup current is guaranteed to be less than 15 μA maximum, helping the designer to reach a low standby power level.
- *Skip-cycle Capability*: A continuous flow of pulses in not compatible with no-load standby power requirements. Slicing the switching pattern in bunch of pulses drastically reduces overall losses but can, in certain cases, bring acoustic noise in the transformer. Due to a skip operation taking place at low peak currents only, no mechanical noise appears in the transformer. This is further strengthened by ON Semiconductor's Soft-Skip technique, which forces the peak current in skip to gradually increase. In case the default skip value would be too large, connecting a resistor to the Pin 6 will reduce or increase the skip cycle level. Adjusting the skip level also adjusts the maximum switching frequency before skip occurs.
- *Soft-Start*: A circuitry provides a soft-start sequence which precludes the main power switch from being stressed upon startup. This soft-start is internal and reaches 5 ms typical.
- *Overvoltage Protection*: By sensing the plateau level after the power switch has opened, the controller can detect an overvoltage condition through the auxiliary reflection of the output voltage. If an OVP is sensed, the controller stops all pulses and permanently stays latched until the V_{CC} is cycled down below 4.0 V.
- *External Latch Input*: By permanently monitoring Pin 5, the controller detects when its level rises above 3.5 V, e.g. in presence of a fault condition like an OTP. This fault is permanently latched-off and needs the V_{CC} to go down below 4.0 V to reset, for instance when the user unplugs the SMPS.
- *Brown-out Detection*: By monitoring the level on Pin 2 during normal operation, the controller protects the SMPS against low mains condition. When the Pin 2 level falls below 240 mV, the controllers stops pulsing until this level goes back to 500 mV to prevent any instability. During brown-out conditions, the PFC is not activated.
- *Short-circuit Protection*: Short-circuit and especially overload protection are difficult to implement when a strong leakage inductance between auxiliary and power windings affects the transformer (the auxiliary winding level does not properly collapse in presence of an output short). Here, every time the internal 0.8 V maximum peak current limit is activated, an error flag is asserted and a time period starts, due to an external timing capacitor. If the voltage on the capacitor reaches 4.0 V (after 90 ms for a 220 nF capacitor) while the error flag is still present, the controller stops the pulses and goes into a latch-off phase, operating in a low-frequency burst-mode. As soon as the fault disappears, the SMPS resumes its operation. The latchoff phase can also be initiated, more classically, when V_{CC} drops below VCC_{OFF} (10 V typical).

Startup sequence

When the power supply is first connected to the mains outlet, the NCP1381/82 starts to consume current. However, due to a novel architecture, the internal startup current is kept very low, below 15 μA as a maximum value. The current delivered by the startup resistor also feeds the V_{CC} capacitor and its voltage rises. When the voltage on this capacitor reaches the VCC_{ON} level (typically 15 V), the controller delivers pulses and increases its consumption. At this time, the V_{CC} capacitor alone supplies the controller: the auxiliary supply is supposed to take over before V_{CC} collapses below VCC_{OFF}. Figure 3 shows the internal arrangement of this structure:

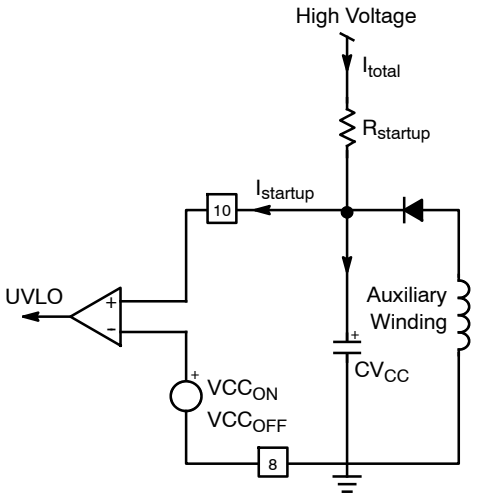


Figure 3. The Startup Resistor Brings V_{CC} Above 15 V

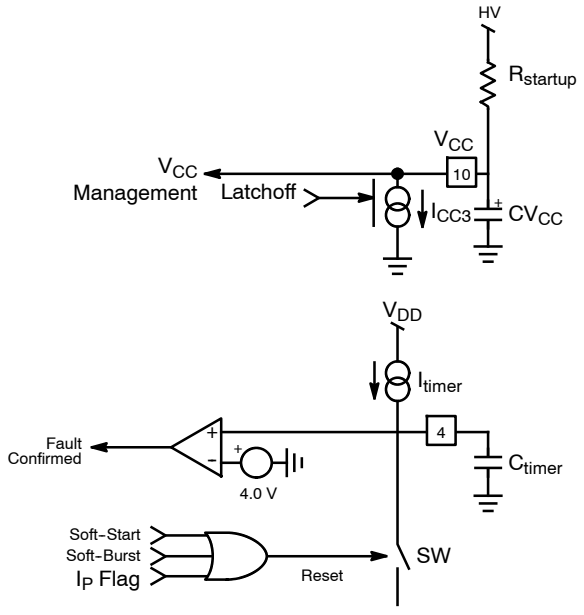


Figure 4. The Timer Section Uses a Current Source to Charge Up the Capacitor

As soon as V_{CC} reaches 15 V (VCC_{ON}), driving pulses are delivered on Pin 9 and the auxiliary winding grows up the V_{CC} pin. Because the output voltage is below the target (the SMPS is starting up), the controller smoothly pushes the peak current to I_{max} (0.8 V / R_{sense}) which is reached after 5 ms (typical internal soft-start period). After soft-start completion, the peak current setpoint reaches its maximum (during the startup period but also anytime a short-circuit occurs), an internal error flag is asserted, I_P Flag, testifying that the system is pushed to the maximum power (I_P = I_P maximum). This flag is used to detect a faulty condition, where the converter asks for the maximum peak capability longer than what has been programmed by the designer. The duration of the faulty condition is actually set up by a capacitor connected to Pin 4.

Figure 4 shows a portion of this internal arrangement. If the fault comparator acknowledges for a problem, the controller stops all driving pulses and turns-on the internal I_{CC3} current-source. This source serves for the latch-off phase creation, that is to say, forcing the V_{CC} to go down, despite the presence of the startup current still flowing via the startup resistor. Therefore, I_{CC3} should be greater than I_{total} to ensure proper operation. When V_{CC} reaches a level of 7 V, I_{CC3} turns to zero and the startup current can lift V_{CC} up again. When V_{CC} reaches 15 V, a new attempt is made. If the fault is still there, pulses last either the timer duration or are prematurely stopped if a VCC_{OFF} condition occurs sooner, and a new latchoff phase takes place. If the fault has gone, the converter resumes operation. Figure 5 portrays the waveforms obtained during a startup sequence followed by a fault. One can see the action of the I_{CC3} source which creates the latchoff phase and the various resets events on the timer capacitor in presence of the soft-start end or an aborted fault sequence.

Knowing that I_{timer} equals 10 μA, we can calculate the capacitor needed to reach 4 V in a typical time period. Suppose we would like a 100 ms fault duration, therefore: C_{timer} = 10 μ x 100 m / 4 = 250 nF, select a 0.22 μF.

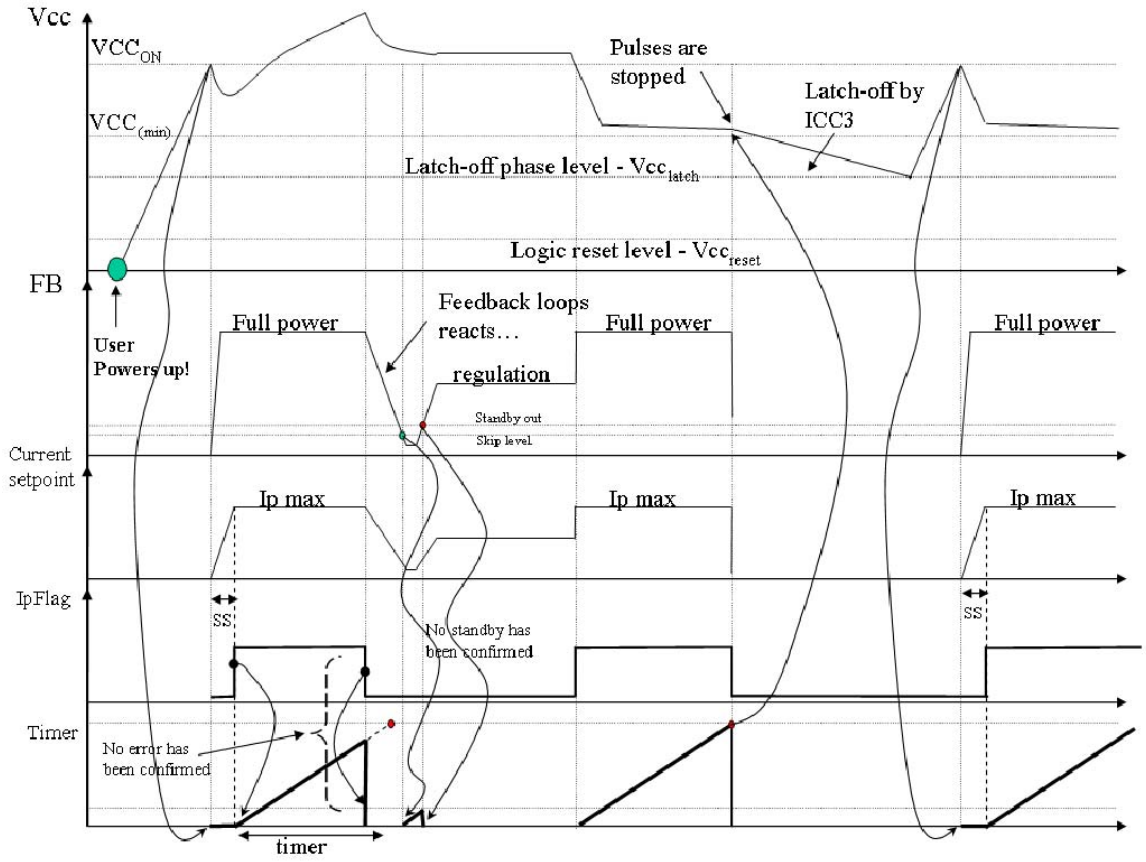


Figure 5. A Typical Startup Sequence Followed by a Faulty Condition

Startup Resistor Calculation

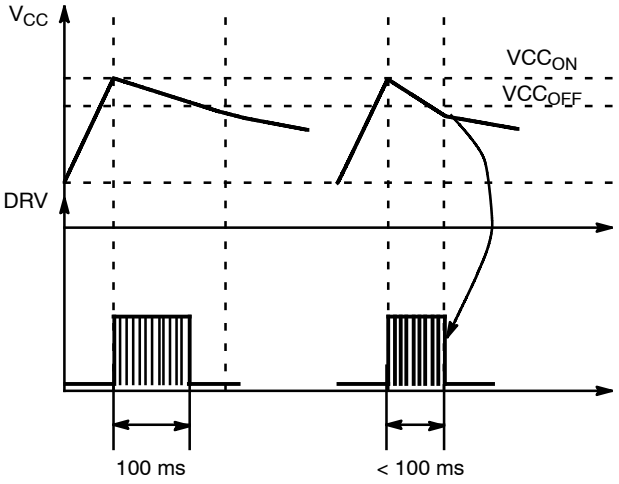
For the sake of the example, we will go through the calculation of the startup element. Suppose that we have the following information:

VCC_{ON} = 15 V.
VCC_{OFF} = 10 V.
I_{CC2} = 4 mA, given by the selected MOSFET Q_g.
Startup duration below 2 s at minimum input voltage.
Input voltage from 85 VAC to 265 VAC.
Standby power below 500 mW.

1. From a startup ΔV of 15 - 10 = 5 V and a 4 mA total consumption, we can obtain the necessary V_{CC} capacitor to keep enough voltage, assuming the feedback loop is closed within 10ms: CV_{CC} = 4 m x 10 m / 5 = 8 μF or 22 μF for the normalized value if we account for the natural dispersion.
2. If we want a startup below 2 s, then the charging current flowing inside the V_{CC} capacitor must be above: I_{charge} > 15 x 22 u / 2 > 165 μA. If we add the 15 μA of I_{CC1}, the total startup current shall be above 180 μA.
3. The minimum input voltage is 85 x 1.414 = 120 V. Then, $R_{startup}$ should be below (120 - 15) / 180 μ < 580 kΩ.
4. From this value, we can calculate the dissipated power at high line: $P_{startup} = (265 \times 1.414)^2 / 580$ k = 242 mW.

In latched mode, an internal zener diode is activated and clamps V_{CC} to around 6 V. When V_{CC} goes below 4 V, this zener is relaxed and the circuit can startup again.

Please note that in fault mode the V_{CC} comparator has the priority and stops the pulses anytime V_{CC} falls below its minimum operating level VCC_{OFF}.



If V_{CC} drops below VCC_{OFF} during a portion where the timer counts, pulses are immediately stopped and the latchoff phase is entered. Here, in this example, the timer was set to 100 ms.

Figure 6.

Quasi-Resonance Operation

Quasi-Resonance (QR) implies that the controller permanently monitors the transformer core flux activity and ensures Borderline Conduction Mode (BCM) operation. That is to say, when the switch closes, the current ramps up in the magnetizing inductance L_P until it reaches a setpoint imposed by the feedback loop. At this point, the power switch opens and the energy transfers from the primary side to the secondary (isolated) portion. The secondary diode is now biased and the output voltage "flies back" to the primary side, now demagnetizing the primary inductance L_P. When this current reaches zero, the transformer core is said to be "reset" ($\varphi = 0$). At this time, we can turn the MOSFET on again to create a new cycle. Figure 7 and 8 portray the typical waveforms with their associated captions. If a delay TW is introduced further to the core reset detection and before biasing the power MOSFET, the drain signal Vds(t) has the time to go through a minimum, also called valley. Therefore, when we will finally reactivate the power MOSFET, its drain-to-source voltage will be minimum, reducing capacitive losses but also its gate-charge value, since the Miller effect gets diminished at low Vds.

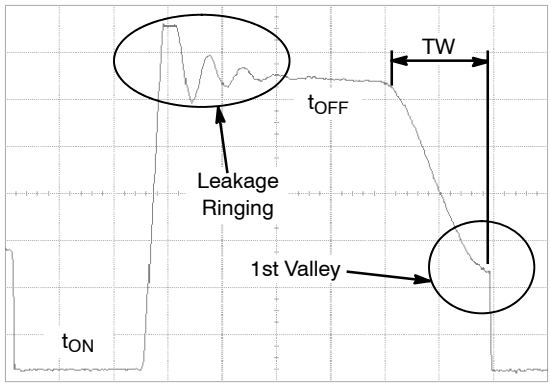


Figure 7. Typical Quasi-Resonance Waveform

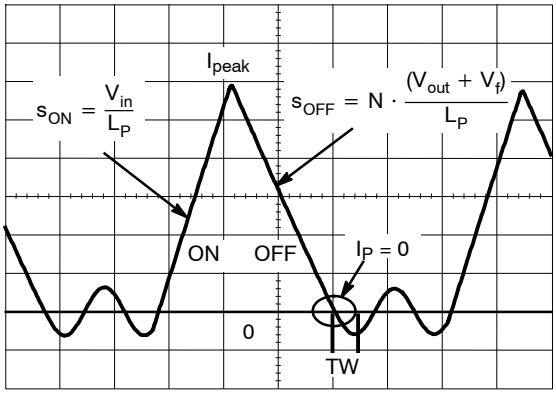


Figure 8. Magnetizing Inductance Current Waveforms

The flux activity monitoring is actually made via an auxiliary winding, obeying the law, $V_{aux} = N \cdot d\varphi / dt$. Figure 9 describes how the detection is made, since the signal obtained on the auxiliary winding is centered to zero. Let's split the events with their associated circuitry:

t_{ON}

The D flip-flop output is high, the MOSFET is enhanced and current grows-up in the primary winding. This is the *on* portion of Figure 8, left side of the triangle. When the driver output went high, its rising edge triggered a 8 μs timer. This 8 μs timer provides a true frequency clamp by driving the D-input of the flip-flop. Now, when the peak current reaches the level imposed by the feedback loop, a reset occurs and the flip-flop output comes low.

If for any reason the controller keeps the gate high (DRV_{out}) implying a t_{ON} longer than 50 μs, then all pulses are stopped and the controller enters a safe, autorecovery, restart mode. This condition can occur if the current sense pin does not receive any signal from the sense resistor or if a short-circuit brings the CS pin to ground for instance.

t_{OFF}

As one can see from Figure 7, a parasitic ringing takes place at the switch opening: this is the leakage inductance contribution. Unfortunately, this leakage can be detected as a core reset event if no precaution is taken. This explains the presence of the 3 μs blanking timer that prevents any restart before the completion of this circuit. After leakage, the voltage applied over the primary winding is an image of the output voltage: this is the flyback level, or plateau level, equal to $N(V_{out} + V_f)$, with N the turn ratio between the primary and the secondary, V_{out} the output voltage and V_f, the secondary diode forward drop. We are on the right portion of Figure 8, OFF portion, the secondary current ramping down. If we now observe the voltage on the auxiliary winding, we will see something like what Figure 10 shows where the plateau lasts until the core is reset. At this reset event, a natural ringing takes place whose amplitude depends on the ratio N and V_{out}. A comparator observes this activity and detects when the voltage drops below ground, actually below 45 mV typically. In Figure 9, one can see the ESD protection arrangement which introduces a small capacitive component to Pin 3 input. This capacitive component associated with the demagnetization resistor can thus realize the necessary above TW delay.

The comparator output now propagates to the clock input of a D flip-flop. Hence, the demagnetization is edge triggered. At the beginning of the cycle (the rising edge of the ON time), the 8 μs timer was started. The output of this timer goes to the D-input of the D flip-flop. Thus, if the demagnetization comparator attempts to trip the D flip-flop when the 8 μs timer has not been completed, the restart is ignored until a new demagnetization signal comes in. This offers the benefit to clamp the maximum switching frequency to 8 μs or 125 kHz. Please note that the 8 μs timer clamps $t_{ON} + t_{OFF}$.

If everything is met, then the flip-flop output goes high and a new switching cycle occurs. Several events can alter this behavior, as described below:

1. The converter is in light load conditions and the theoretical frequency is above 125 kHz. There, the D-input is not validated and the reset event is ignored. The flip-flop waits for another wave to appear. If outside of the 8 μs window, i.e. $F_{switching}$ below 125 kHz, the event is acknowledged and a new cycle occurs. Note that wave skipping will always occur in the drain-source valley.
2. We are skipping cycle at moderate power and the skip comparators dictates its law. In that case, if the flip-flop is permanently reset, it naturally ignores all demagnetization restart attempts, provided that the drain oscillations are still there. When the flip-flop reset is released, the controller acknowledges the incoming demagnetization order and drives the output high. Again, skip cycles events always take place in the valley.
3. The controller skips cycles at low power and the order appears in a fully damped drain-source portion. In that case, the 8 μs timeout generator will give the signal in place of the demagnetization comparator. This timeout generator is reset everytime waves appear but starts to count down when there is no sufficient amplitude on the drain. At the end of the 8 μs, if no wave has appeared, it goes high, indicating that the controller is ready to restart anytime a skip order takes place. See skip section for more details.

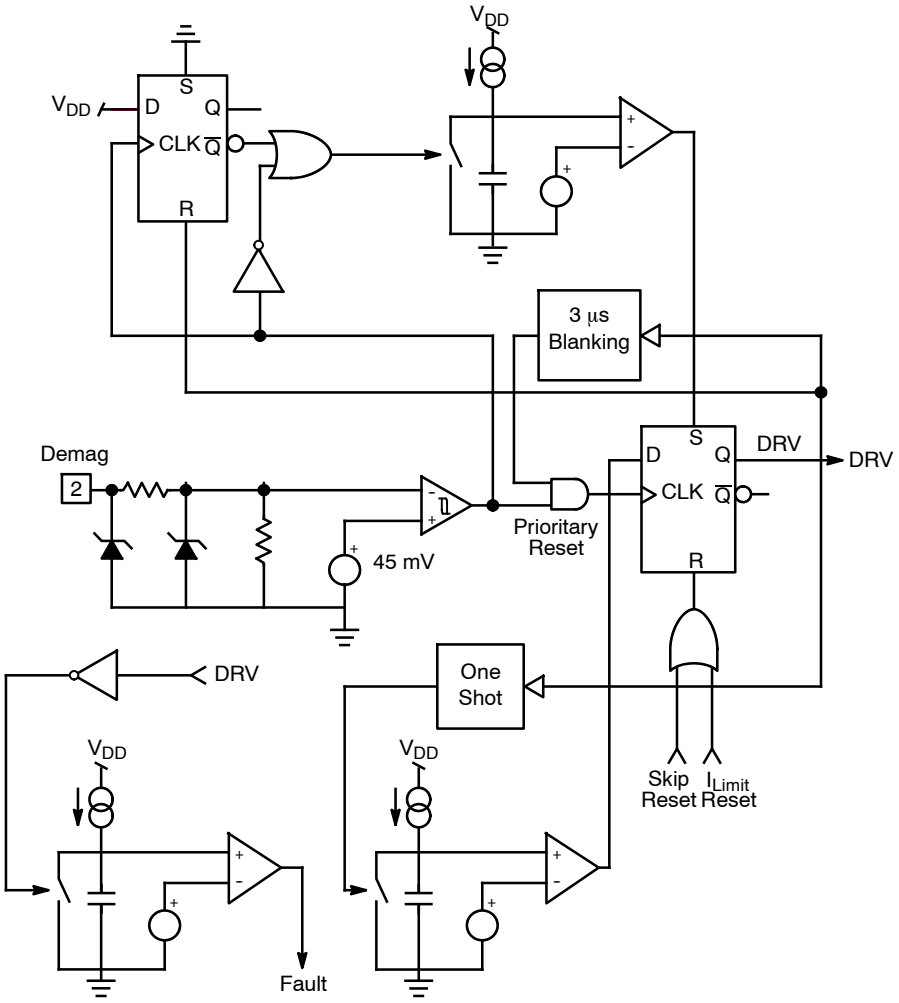


Figure 9. Internal QR Architecture

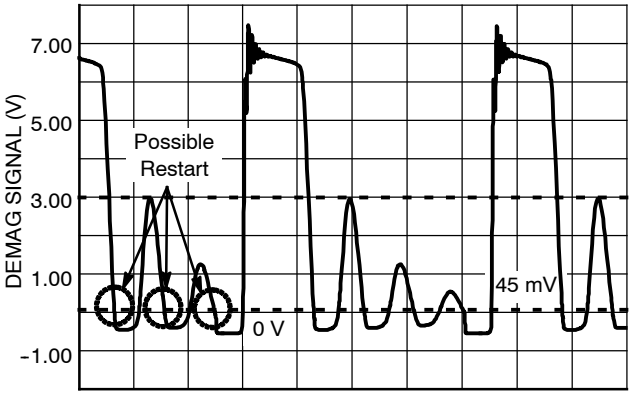


Figure 10. Core Reset Detection is Done Through the Monitoring of a Dedicated Auxiliary Winding

Skipping Cycle Mode

The NCP1381/82 automatically skips switching cycles when the output power demand drops below a given level. This is accomplished by monitoring the FB pin. In normal operation, pin 6 imposes a peak current accordingly to the load value. If the load demand decreases, the internal loop asks for less peak current. When this setpoint reaches a determined level, the IC prevents the current from decreasing further down and starts to blank the output pulses: the IC enters the so−called skip cycle mode, also named controlled burst operation. The power transfer now depends upon the width of the pulse bunches (Figure 11) and follows the following formula:

$$\frac{1}{2} \cdot L_P \cdot I_P^2 \cdot F_{sw} \cdot D_{burst} \quad \text{(eq. 1)}$$

with

L_P = Primary Inductance

F_{sw} = Switching Frequency Within the Burst

I_P = Peak Current at which Skip Cycle Occurs

D_{burst} = Burst Width/Burst Recurrence

Figure 12 depicts the internal comparator arrangement. The FB pin level is permanently compared to a fixed level, V_{skip}, also available on Pin 5 for adjustment. As a result, the user can wire a resistor to ground and alter the skip level in case of noise problems. When the FB pin is above V_{skip}, the comparator is transparent to the operation. When the load becomes lighter, the FB level goes down too. When it reaches V_{skip}, the comparator goes high and resets the internal flip−flop: the driving pulses are stopped. As a result, V_{out} starts to also decrease since no energy transfer is ensured. Detecting a decay in the output voltage, the FB loop will react by increasing its level. When the level crosses V_{skip} plus a slight hysteresis, pulses restart again: a ripple occurs on the FB pin. Please note that the soft−start will be activated every time the skip comparator asks to restart. Therefore, instead of having sharp skip transitions, a smooth current rampup can be observed on the current envelope. This option significantly decreases the acoustical noise. Figure 13 shows a typical shot and Figure 15 portrays several skip cycles.

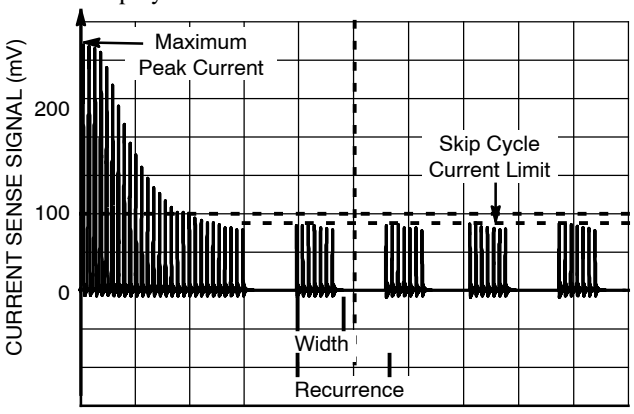


Figure 11. The Skip Cycle Takes Place at Low Peak Currents Which Guaranties Noise Free Operation

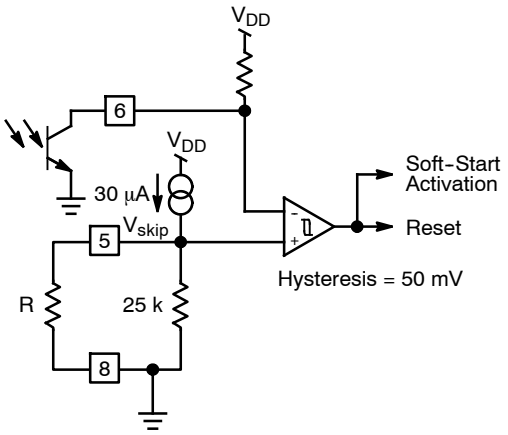


Figure 12. A Resistor to GND can Adjust the Skip Level

As soon as the feedback voltage goes up again, there can be two situations as we have seen before: in normal operating conditions, e.g. when the drain oscillations are generous, the demagnetization comparator can detect the 45 mV crossing and gives the “green light”, alone, to reactive the power switch. However, when skip cycle takes place (e.g. at low output power demands), the restart event slides along the drain ringing waveforms (actually the valley locations) which decays more or less quickly, depending on the $L_{primary}$−$C_{parasitic}$ network damping factor. The situation can thus quickly occur where the ringing becomes too weak to be detected by the demagnetization comparator: it then permanently stays locked in a given position and can no longer deliver the “green light” to the controller. To help in this situation, the NCP1381/82 implements a 8 μs timeout generator: each time the 45 mV crossing occurs, the timeout is reset. So, as long as the ringing becomes too low, the timeout generator starts to count and after 8 μs, it delivers its “green light”. If the skip signal is already present then the controller restarts; otherwise the logic waits for it to release the reset input and set the drive output high. Figure 14 depicts these two different situations:

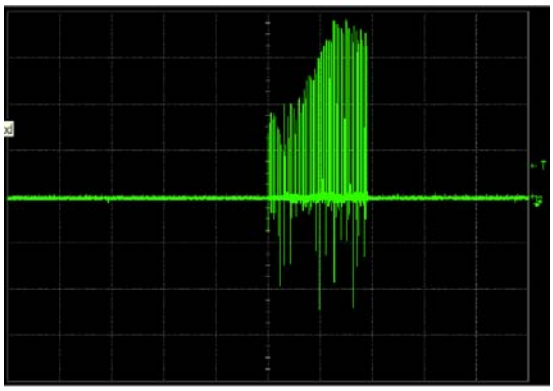


Figure 13. The Soft−start Starts During Skip Mode and Smooths the Current Signature

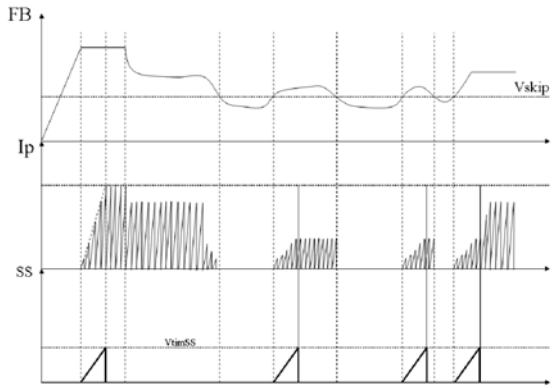


Figure 15. The Internal Soft−start is Activated During Each Skipped Cycles

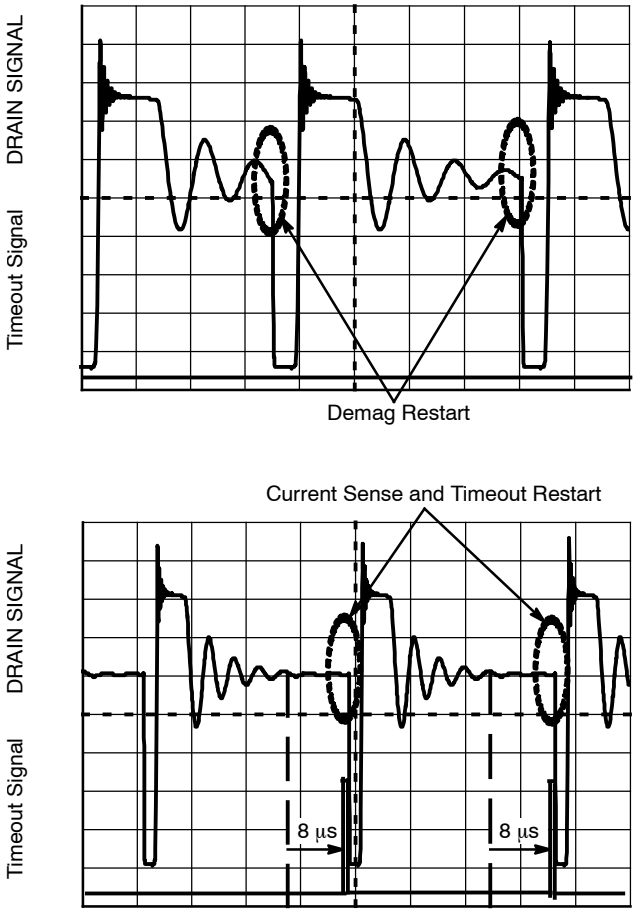


Figure 14. The 8 μs Timeout Helps to Restart the Controller

Overpower Compensation

A FLYBACK converter operating in Borderline Conduction Mode (BCM) transfers energy from primary to secondary according to the following law:

$$P_{in} = \frac{P_{out}}{\eta} = \frac{1}{2} \cdot L_P \cdot I_P^2 \cdot F_{SW} \quad \text{(eq. 2)}$$

Therefore, we can see that for various switching frequency values (dependent on the input condition if the output demand is fixed), the converter will permanently adjust the peak current I_P to keep the output power constant. By manipulating the slope definitions S_{ON} and S_{OFF} (see Figure 8), we can show that the peak current is defined by:

$$I_P = 2 \cdot P_{out} \cdot \frac{N \cdot (V_{out} + V_F) + V_{in}}{\eta \cdot V_{in} \cdot N \cdot (V_{out} + V_F)} \quad \text{(eq. 3)}$$

where η is the converter's efficiency, V_{in} the input voltage, V_{out} the output voltage. Feeding a math processor lets us graph the peak variation with the input voltage, as depicted by Figure 16 for a 90 W converter operating on universal mains and featuring the following parameters:

V_{out} = 19 V @ 4.7 A,
N_P:N_S = 1:0.166,
R_{sense} = 0.25 Ω, 200 VDC − 400 VDC Input Voltage,
t_P (Propagation Delay) = 100 ns,
L_P = 700 μH, η = 0.85 and V_F = 0.8 V
Note that these elements were selected to design for a 100 W value, giving us design margin.

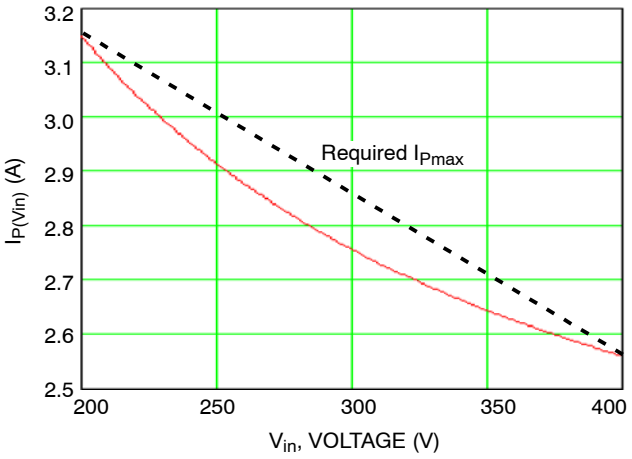


Figure 16. Peak Current Evolution with Input Voltage in a QR Converter at Constant Output Power (100 W)

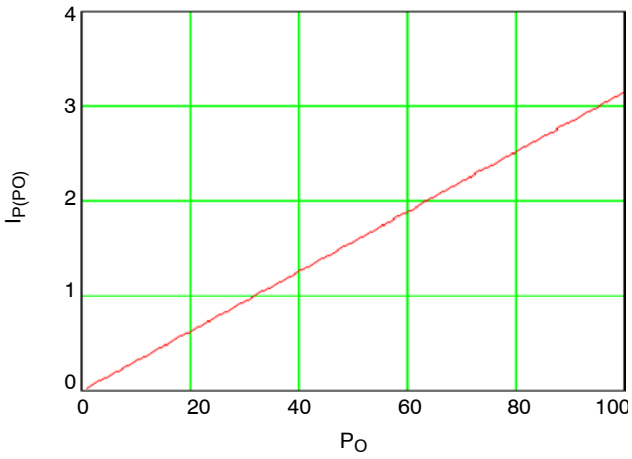


Figure 17. I_P Evolution with Output Power

As a result, we will probably calculate our sense resistor to let the converter bring the peak current up to 3.15 A at low mains (200 VDC in follower-boost configuration). Unfortunately, in high mains conditions, where the PFC delivers up to 400 VDC, the controller will also allow the same 3.15 A maximum peak current (even a little more with the propagation delay) and the power will dramatically increase. In these conditions, the maximum power shall absolutely be clamped in order to avoid lethal runaways in presence of a fault. If overpower compensation via a resistor to the bulk capacitor offers a possible way, it suffers from the lack of precision and good repeatability in production. It also degrades the standby consumption.

Since our controller integrates a brown-out (BO) protection that permanently senses the bulk capacitor, we naturally have a voltage image of the bulk voltage. By converting the BO level into a current, then routing this current in the current sense (CS) pin, we can easily create a variable offset that will compensate the maximum output power. This would result in a variable I_{Pmax} as exemplified by the dashed line on Figure 16.

From the peak current definition, we can extract the output power variation, with a fixed peak current (the maximum peak the controller will authorize is 0.8 / R_{sense}) and thus quantify the difference between low and high line:

$$P_{nc}(V_{in}) := \frac{\left(\frac{0.8}{R_S} + \frac{V_{in}}{L_P} \cdot t_P\right)}{\frac{2}{(\eta \cdot (V_{in} \cdot (V_{out} + V_F)))} \cdot \left(V_{out} + V_F + \frac{V_{in}}{N}\right)} \quad \text{(eq. 4)}$$

where

t_P is the propagation delay (100 ns typically).

If we enter our previous parameters into the noncompensated output power definition and plot the result versus the input voltage, then we obtain the following graph, Figure 18:

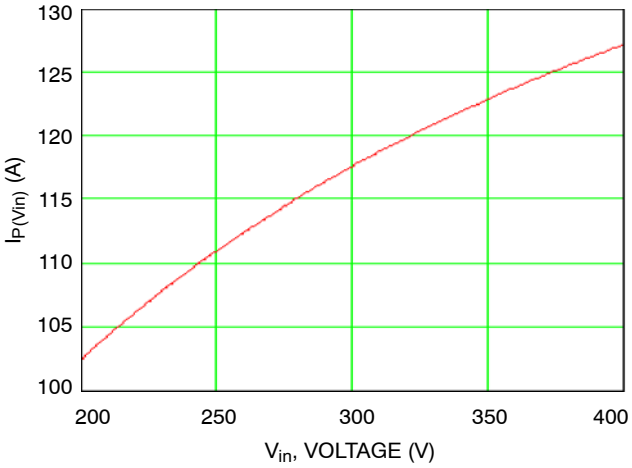


Figure 18. Output Power Evolution with the Input Voltage (No Compensation)

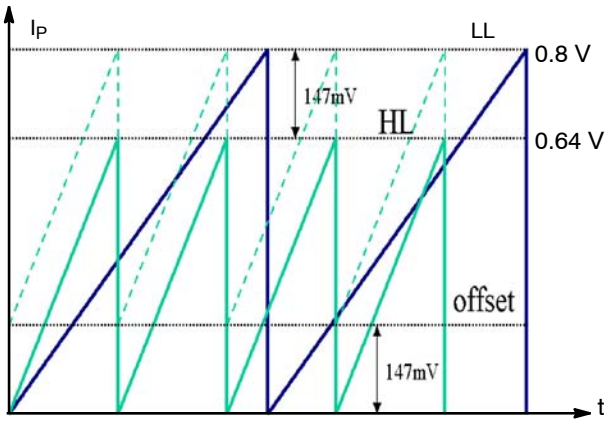


Figure 19. A Possible Way to Compensate the Current Excursion Lies in Offsetting the Current Floor

As one can observe, the output power runs out of the initial 100 W specification when we enter the high line region. To cope with this problem, we need to compensate the controller in such a way that its peak capability gets reduced at higher input voltages. How much do we need to compensate the peak excursion? We can find the answer by calculating $\Delta I_P = I_{PLL} - I_{PHL}$, with $V_{inLL} = 200$ V and $V_{inHL} = 400$ V. With our previous numbers, $\Delta I_P = 588$ mA. We therefore need to instruct the controller to reduce its peak excursion by 588 mA at high line. Otherwise speaking, if we think in voltages, the CS pin excursion shall drop from 0.8 V (at low line, the maximum peak is $0.8 / R_S$) to (3.2 - 0.588).

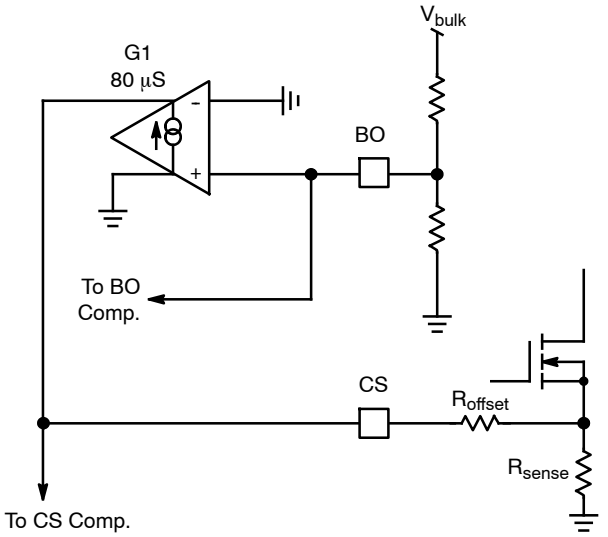


Figure 20. A Transconductance Amplifiers Transforms the BO Voltage into a Current

We can now calculate our R_{offset} resistor to generate the necessary static voltage. Suppose that the BO network divides the bulk voltage by 400 ($V_{BO} = \alpha \cdot V_{in} = 0.0025 \times V_{in}$). Therefore, in presence of a 400 V input voltage, we will have 1 V on the BO pin. due to the transconductance amplifier of a 80 µS gm, it will turn into a 80 µA offset current. To get our 147 mV, we just divide it by 80 µA: $R_{offset} = V_{offset} / V_{inHL} \times \alpha \cdot g_m = 1.8$ kΩ.

We can now update Equation 4 with Equation 5, where the peak current is affected by the variable offset:

$$P_O(V_{in}) := \frac{\left(\frac{0.8}{R_S} + \frac{V_{in}}{L_P} \cdot t_P - V_{in} \cdot \alpha \cdot g_m \cdot R_{offset}\right)}{\frac{2}{(\eta \cdot (V_{in} \cdot (V_{out} + V_F)))} \cdot \left(V_{out} + V_F + \frac{V_{in}}{N}\right)} \quad \text{(eq. 5)}$$

If we now plot the compensated curve, we obtain Figure 21 graph. The output power is slightly above what we

0.25 = 653 mV at high line. Figure 19 shows the situation at both line levels. A possible solution lies in offsetting the current floor by the necessary value, which is, in our case, 0.8 - 0.653 = 147 mV. The traditional way of doing this goes through the wiring of a high value resistor to the bulk capacitor. This unfortunately dissipates heat. The NCP1381/82 offers a more elegant option since it transforms the voltage available from the Brown-out pin into a fixed current, routed to the CS pin. That way, we can calculate a resistor value which, once inserted in series with current sense voltage image, will create our necessary offset. Figure 20 shows this internal connection:

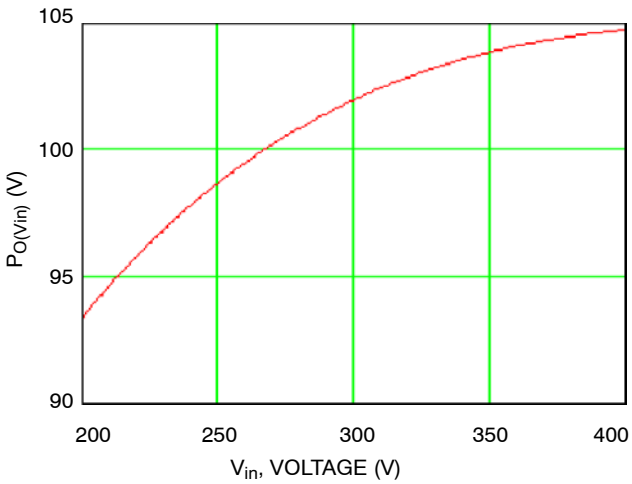


Figure 21. The Compensated Converter Output Power Response to Input Variations

were originally shooting for and the total power excursion is now kept within 15 W.

Overvoltage Protection

The NCP1381/82 features an overvoltage protection made by sensing the plateau voltage at the switch turn-off. However, a sampling delay is introduced to avoid considering the leakage inductance. When the demagnetization pin goes above $V_{demlatch}$, the comparator goes high. If this condition is maintained when the sampling pulse arrives, then a fault is latched. Figure 22 shows the arrangement and Figure 23 portrays a typical waveform. Once latched, the controller stops all driving pulses and V_{CC} is clamped to 6 V. Reset occurs when the user unplugs the converter from the mains and V_{CC} reduces below 4 V.

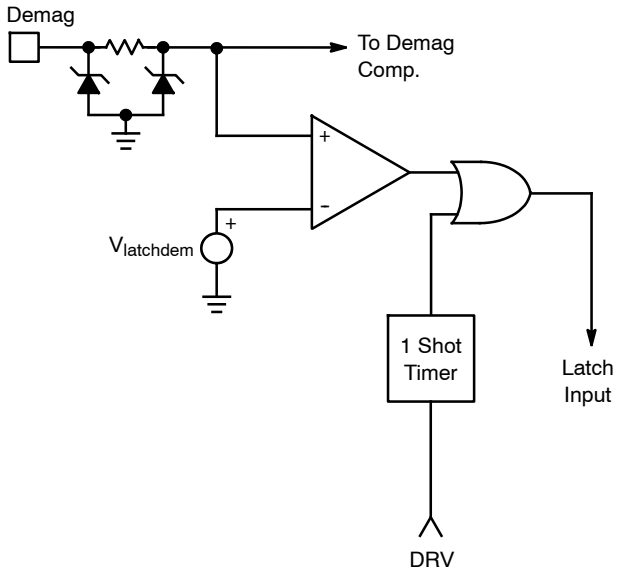


Figure 22. Plateau Sensing Overvoltage Protection

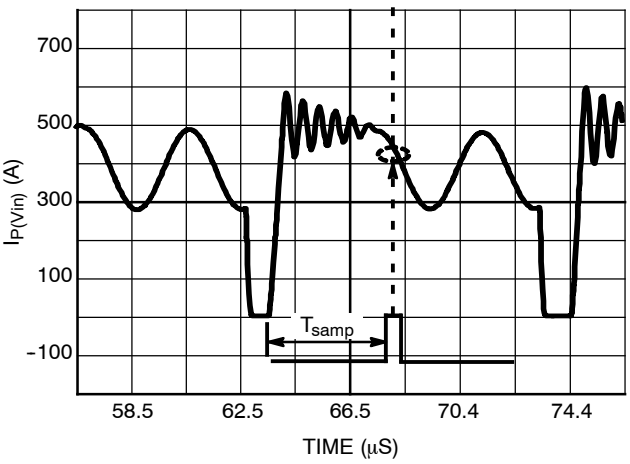


Figure 23. Typical Sensed Waveforms

External Latchoff

By lifting up Pin 5 above V_{latch} (3.5 V Typ - NCP1381, 2.5 V Typ - NCP1382), the circuit is permanently latched. That is to say, Pin 9 goes low, the GTS pin no longer supplies the PFC and the V_{CC} is clamped to 6 V. The latch reset occurs when V_{CC} falls below 4 V, e.g. when the user unplugs the converter from the mains. Figure 24 shows several options on how to connect a PNP to implement an OVP or Overtemperature Protection (OTP).

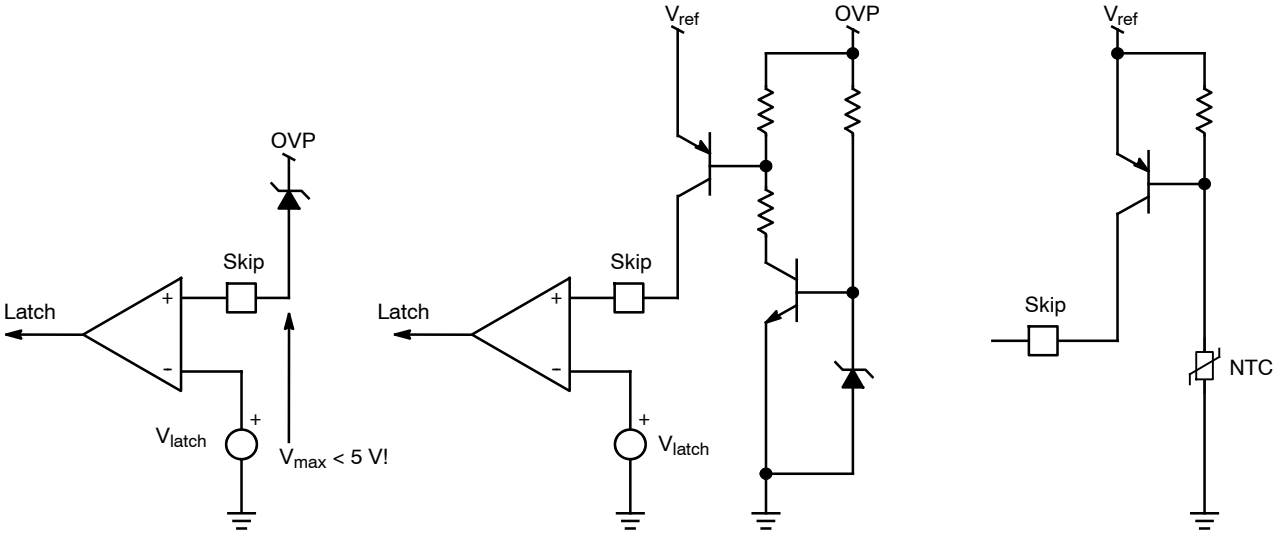


Figure 24. Wiring a PNP Transistor on the Skip Cycle Input Pin will Latch the Circuit.

Keep in mind that the 5 V maximum limit on all low voltage pins implies some precaution when triggering the latch voltage. The cheapest option is obtained when wiring a simple zener diode in series with the monitored line. Care must be taken to limit the excursion of the skip pin before fully latching the controller.

Go-To-Standby detection

The PFC front-end stage delivers an elevated voltage to the Flyback converter and keeps the mains power factor close to unity. However, in standby, this PFC stage is no longer needed and must be turned off to save watts and thus reduce the no-load standby power. To detect when the converter enters standby, the controller observes the voltage available on Pin 1: typically, a portion of the feedback voltage will be used. In higher power conditions, this level

is high, in low power conditions, this voltage is low. Unfortunately, the situation complicates with QR converters since the input voltage plays a significant role in the feedback voltage evolution. A case can happen where the converter is supplied by a 400 V rail and suddenly enters standby: the PFC turns off and the bulk voltage goes low, let's say 120 VDC (V_{in} = 85 VAC). At this time, the power transfer changes, the propagation delay plays a smaller role and the feedback voltage naturally goes up again. If a sufficient hysteresis is not built, there are possibilities to see hiccup on the PFC V_{CC}, which is not a desirable feature. Therefore, hysteresis is mandatory on top of the Go-To-Standby (GTS) detection level. For this reason it is possible to increase the hysteresis of the ADJ_GTS comparator due to an internal 5 μA current source that can create an offset to the input signal if a series resistor is inserted. The ADJ_GTS detection level is also adjustable by tuning the portion of the external signal applied to Pin 1 (the reference of the internal comparator is 250 mV).

Again, to check how we manage the feedback variations, we can plot these variations without compensation for a given power, and with the offset resistor connected to the CS pin. In the first case, the FB voltage dependency on V_{in} can be expressed by:

$$FB(V_{in}) := \left[2 \cdot P_O \cdot \frac{N \cdot (V_{out} + V_F) + V_{in}}{\eta \cdot V_{in} \cdot N \cdot (V_{out} + V_F)} - \frac{V_{in}}{L_P} \cdot t_P\right] \cdot R_S \cdot F_{BCS} \quad \text{(eq. 6)}$$

Where FB_{CS} is the ratio between the FB level and the current setpoint. In our controller, this ratio is 4. If we now incorporate our offset voltage generated by the R_{offset} resistor and the input voltage, the compensated FB variation expression becomes:

$$FB_{Comp}(V_{in}) := \left[\left[\left[2 \cdot P_O \cdot \frac{N \cdot (V_{out} + V_F) + V_{in}}{\eta \cdot V_{in} \cdot N \cdot (V_{out} \cdot V_F)}\right] - \frac{V_{in}}{L_P} \cdot t_P\right] \cdot R_S + V_{in} \cdot \alpha \cdot g_m \cdot R_{offset}\right] \cdot F_{BCS} \quad \text{(eq. 7)}$$

with α the BO divider ratio (0.00414 in our example), gm the transconductance slope of 80 μS and R_{offset}, the selected offset resistor.

If now plot Equation 6 and Equation 7 for a 8 W output power, we will obtain Figures 25 and 26:

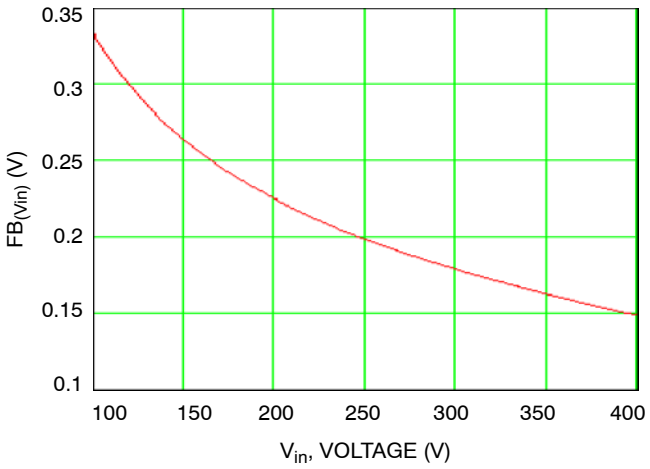


Figure 25. Uncompensated FB Variations for P_{out} = 8 W

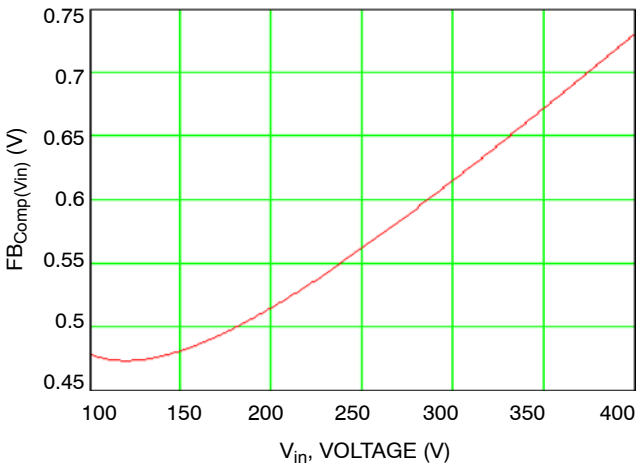


Figure 26. Compensated FB variations P_{out} = 8 W

As one can see on Figure 26, the FB level now falls down when the PFC is shut off. It now goes in the right direction (FB growing up with V_{in}) and this plays in our favor to not cross again the upper comparison level, as it could be the case in Figure 25. However, we must check that the offset programmed by R_{offset} (147 mV in our example) multiplied by 4, is still below our skip cycle level, otherwise the converter will never enter skip at high line (the permanent offset at high line will force a higher feedback):

$$0.147 \cdot 4 = 588 \text{ mV} < 0.75 \text{ V} \quad \text{(eq. 8)}$$

This is okay.

The drawback of Figure 26 is the higher forced level for lower power outputs. In our example, a 90 W adapter, the PFC will be shutdown at P_{out} = 8 W, or a bit less than 10% of the nominal power. If the designer needs to increase or decrease this value, it can adjust the ADJ_GTS level, still keeping in mind Equation 8 relationship.

To avoid a false tripping, the timer (90 ms with Pin 4 capacitor of 220 nF) will be started every time the GTS signal goes high. If at the end of the 90 ms the GTS signal is still high, the standby is confirmed and the SW switch between Pins 11 and 10 opens. To the opposite, when the output power is needed, there is no delay and the SW switch turns on immediately. Figure 27 zooms on the internal circuitry whereas Figure 28 shows typical signal evolutions:

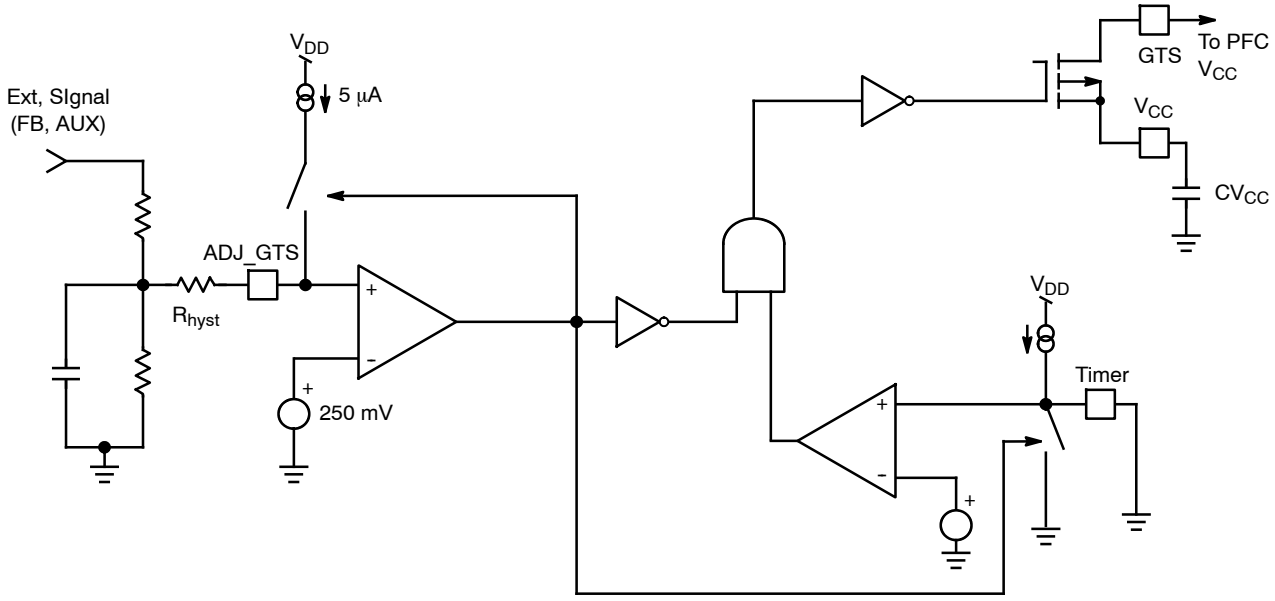
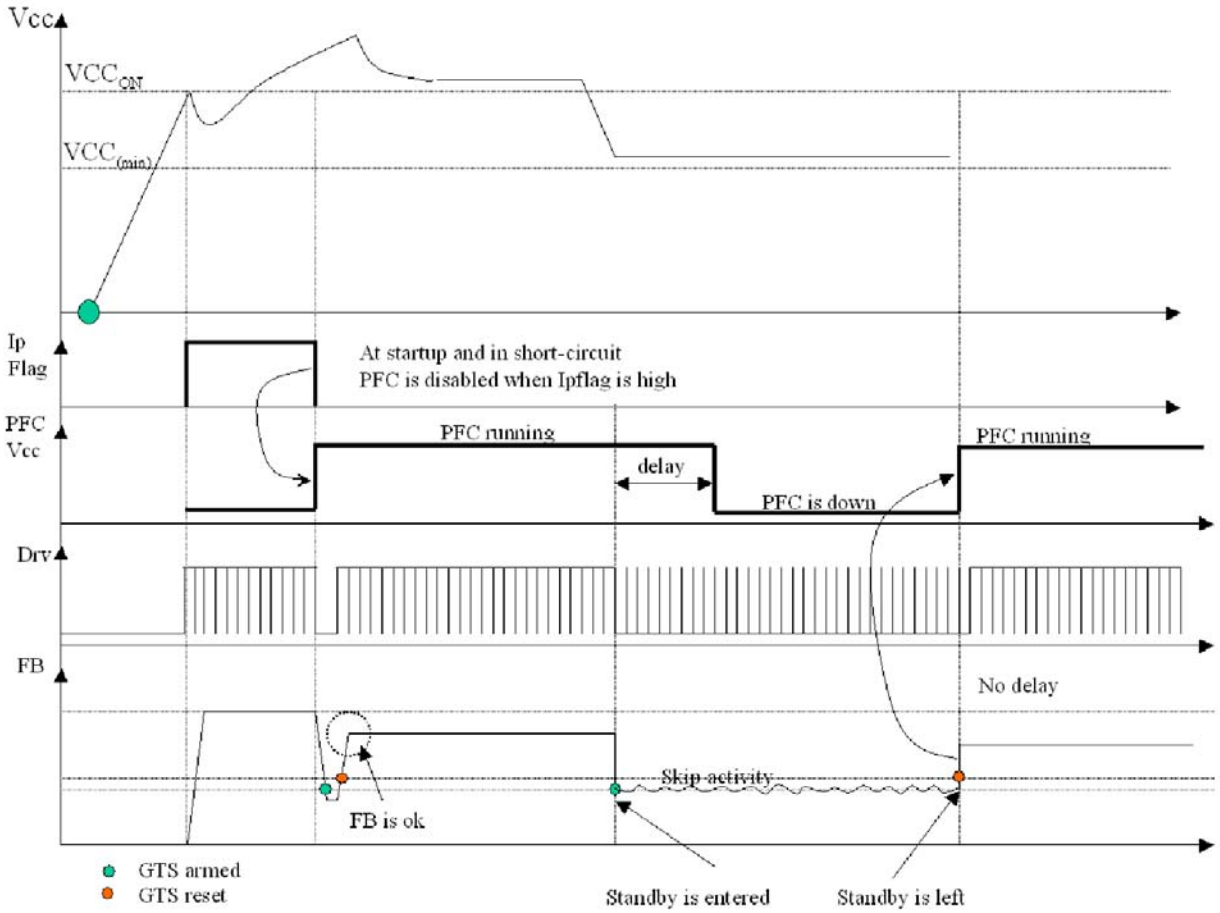


Figure 27. The SW Switch is Turned Off After the Timer Confirms the Presence of a Standby



During the startup sequence, the PFC is disabled (in short−circuits too) and runs as soon as the I_P Flag goes down. When the standby is detected, the timer runs and confirms the standby mode. When the mode is left, there is no delay and the PFC is turned−on immediately.

Figure 28.

During the startup sequence, the converter starts by itself, the PFC is in off mode (SW switch is open). However, when the I_P Flag is down, without delay, the PFC is turned on. In short−circuit mode, the I_P Flag is constantly high during startup attempts and the PFC never turns on. This option reduces the stress on all the elements. The PFC is also in off mode when in presence of a brown−out detection.

In brown−out conditions, the PFC is turned−off. When the level on Pin 2 is back to normal conditions, then a clean startup sequence takes place as Figure 28 depicts and the PFC turns on after the I_P Flag release. The bullets below summarize what we have described:

1. On startup, the PFC is turned on immediately after the I_P Flag has disappeared (converter is stabilized). There is no delay.
2. If a short−circuit occurs, a delay takes place before shutting off the driving pulses. When the delay is elapsed, pulses are turned off and the PFC goes in the off mode. The controller starts to hiccup.
3. In short−circuit hiccup mode, as I_P Flag always stays high (in short−circuit, there is no FB signal), the PFC is never activated.
4. if a VCC_{OFF} condition occurs, all pulses are immediately shutdown and the PFC V_{CC} goes low as well.
5. if a brown−out condition is sensed, all pulses are immediately shut down and the PFC V_{CC} goes low as well.

The freedom is given to the designer to use an other signal than the FB to detect the standby mode and shutdown the PFC (the voltage from the auxiliary winding, or the average of the DRV signal for instance).

Brown−Out Protection

Also called “Bulk OK” signal (B_{OK}), the brown−out (BO) protection prevents the power supply from being adversely destroyed in case the mains drops to a very low value. When this occurs, the controller no longer pulses and waits until the bulk voltage goes back to its normal level. A certain amount of hysteresis needs to be provided since the bulk capacitor is affected by some ripple, especially at low input levels. For that reason, when the BO comparator toggles, the internal reference voltage changes from 500 mV to 250 mV. This effect is not latched: that is to say, when the bulk capacitor is below the target, the controller does not deliver pulses. As soon as the input voltage grows−up and reaches the level imposed by the resistive divider, pulses are passed to the internal driver and activate the MOSFET. Figure 29 offers a way to connect the elements around Pin 2 to create a brown−out detection. Please note that this technique does not use a current source for the hysteresis but rather a capacitor. It offers a way to freely select the resistive bridge impedance.

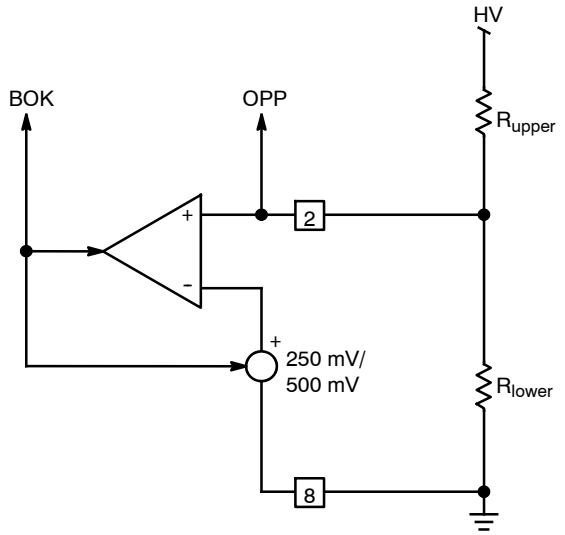


Figure 29. A Way to Implement a BOK Detector on Pin 2

The calculation procedure for R_{upper} and R_{lower} requires a few lines of algebra. In this configuration, the first level transition is always clean: the SMPS is not working during the startup sequence and no ripple exists superimposed on C_{bulk}. Supposed we want to start the operation at $V_{bulk} = V_{trip} = 120$ VDC ($V_{inAC} = 85$ V).

1. Fix a Bridge Current I_b Compatible with Your standby Requirements, for Instance an I_b of 50 μA
2. Then Evaluate R_{lower} by: $R_{lower} = 0.5 / I_b = 10\ k\Omega$
3. Calculate R_{upper} by:
   $(V_{trip} - 0.5\ V) / I_b = (120 - 0.5) / 50\ \mu = 2.39\ M\Omega$

The second threshold, the level at which the power supply stops (V_{stop}), depends on the capacitor C_{fil} but also on the selected bulk capacitor. Furthermore, when the load varies, the ripple also does and increases as V_{in} drops. If C_{fil} allows too much ripple, then chances exist to prematurely stop the converter. By increasing C_{fil}, you have the ability to select the amount of hysteresis you want to apply. The less ripple appears on Pin 2, the larger the gap between V_{trip} and V_{stop} (the maximum being $V_{stop} = V_{trip}/2$). The best way to assess the right value of C_{fil}, is to use a simple simulation sketch as the one depicted by Figure 30. A behavioral source loads the rectified DC line and adjusts itself to draw a given amount of power, actually the power of your converter (35 W in our example). The equation associated to B_{load} instructs the simulator to not draw current until the brown−out converter gives the order, just like what the real converter will do. As a result, V_{bulk} is free of ripple until the node CMP goes high, giving the green light to switch pulses. The input line is modulated by the “timing” node which ramps up and down to simulate a slow startup / turn−off sequence. Then, by adjusting the C_{fil} value, it becomes possible to select the right turn off AC voltage. Figure 31 portrays the typical signal you can expect from the simulator. We measured a turn on voltage of 85 VAC whereas the turn−off voltage is 72 VAC. Further increasing C_{fil} lowers this level (e.g. a 1 μF gives 65 VAC in the example).

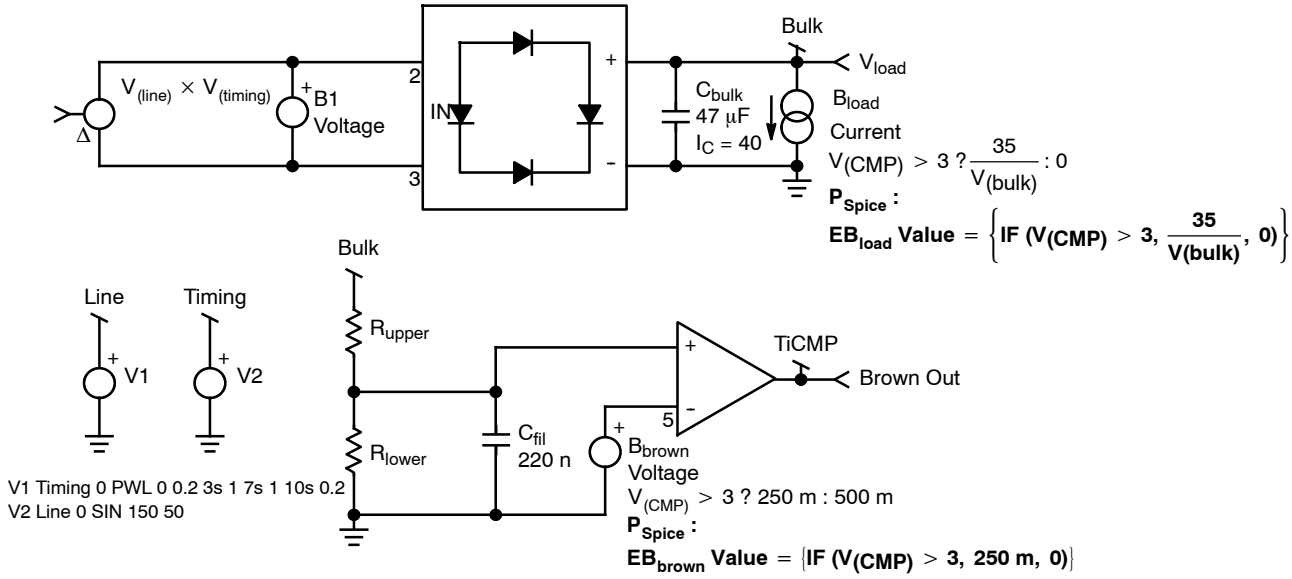


Figure 30. A Simple Simulation Configuration Helps to Tailor the Right Value for C_{fil}

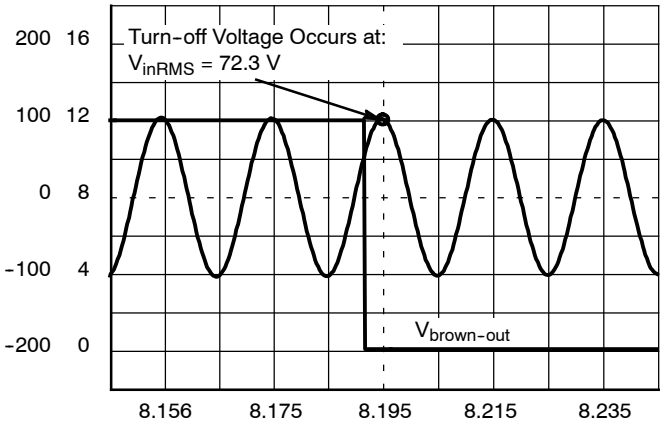


Figure 31. Typical Signals Obtained from the Simulator

Brown−out internal circuit

Given the low startup current and the weak overall consumption of the controller, a circuit needs to be found in order to create a hiccup mode when there is not enough mains detected on Pin 2. Figure 32 portrays the solution based on a 1mA current source, solely activated when the V_{CC} is going low and the BOK has not authorized the controller to pulse. This 1 mA actually discharges the V_{CC} capacitor to make V_{CC} reach 10 V. At this point, the source goes to zero and the startup resistor replenishes the V_{CC} capacitor. When we reach 15 V, the logic checks whether the BOK gives the green light. If not, V_{CC} goes low via the 1 mA. The logic arrangement is made in such a way that if the mains comes back asynchronously to V_{CC} (e.g. in the downslope or in the upslope), we always restart at V_{CC} = 15 V. Figure 33 shows a simulated behavior with a mains going up and down. Figure 34 and 35 confirm the good restart synchronization with the 15 V level.

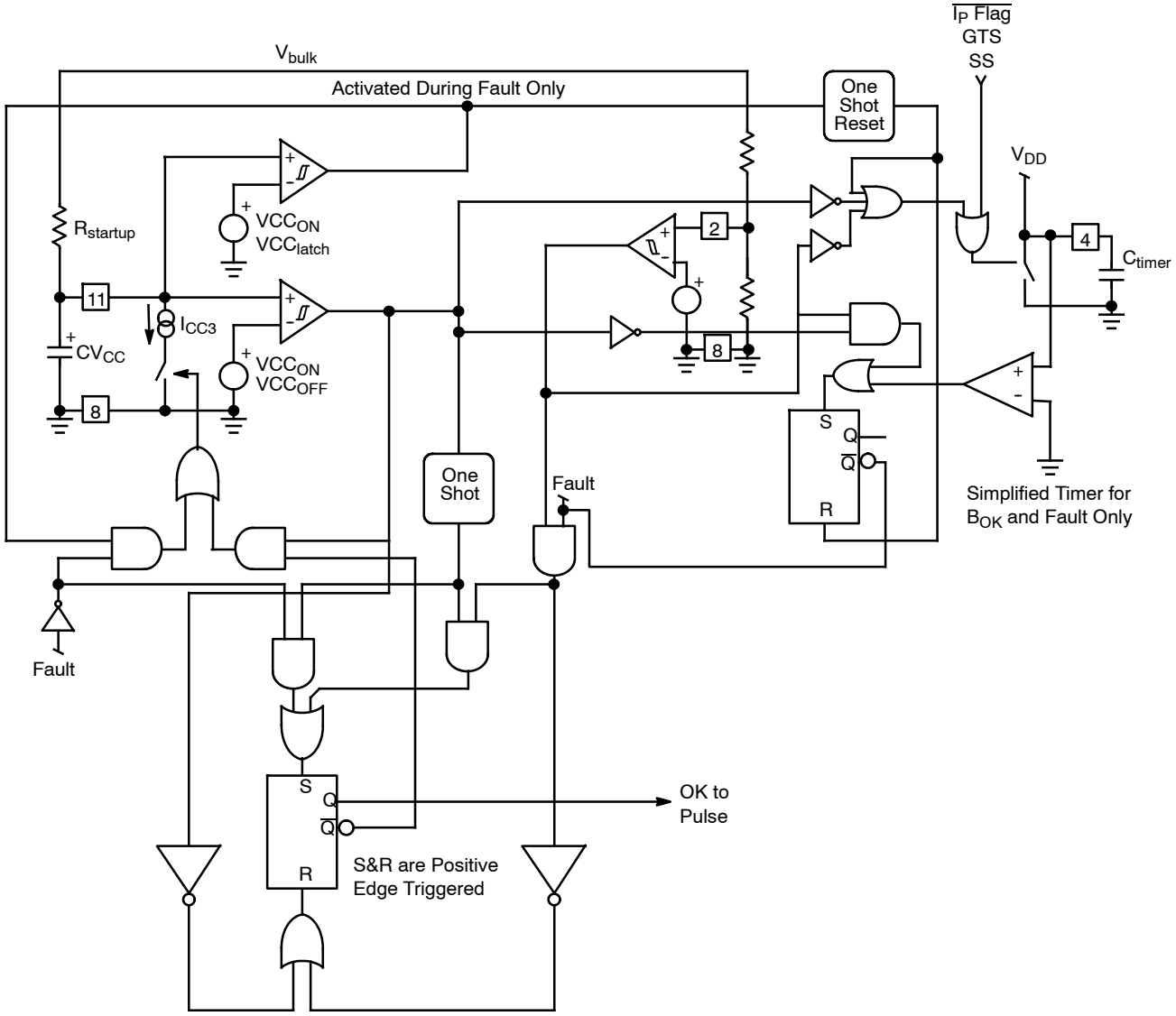
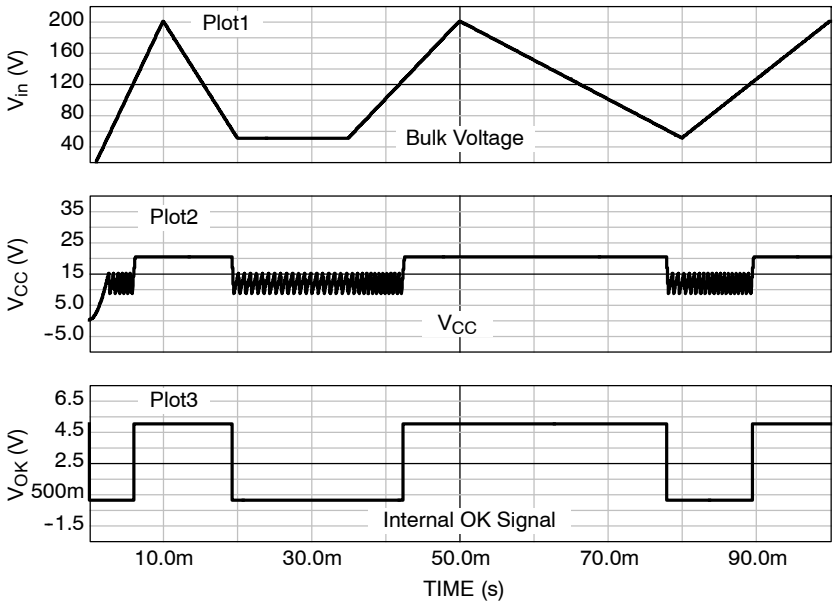


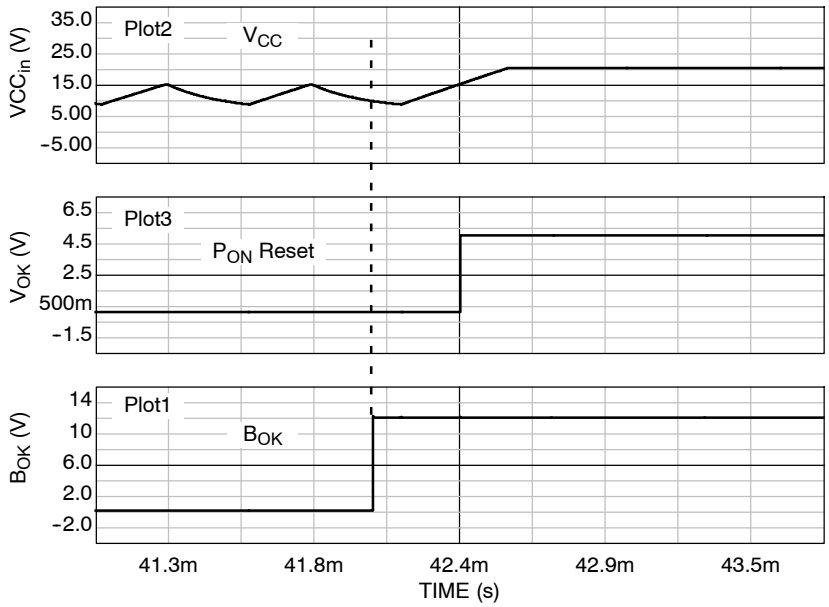
Figure 32. The Internal Brown−out Circuit

Figure 32 also includes the short−circuit latch−off phase generation. The difference between behaviors in BO or short−circuit, is the lack of latch−off phase in brown−out conditions: V_{CC} ramps up and down between VCC_{ON} and VCC_{OFF} in BO, whereas it goes down to 7 V and up to 15 V in short−circuit conditions. Figure 36 shows how V_{CC} moves when a short−circuit is detected. In BO conditions, the PFC is disabled as in UVLO conditions.



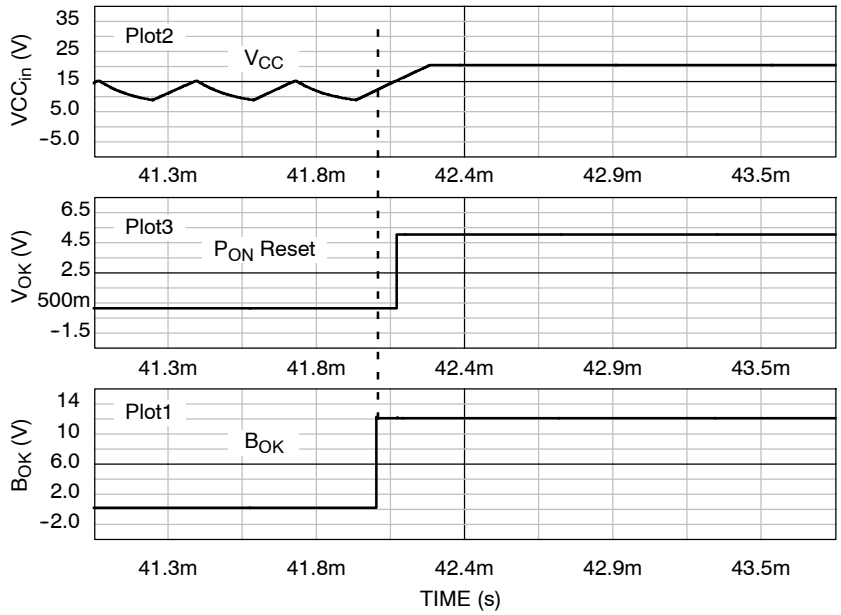
The mains goes up and down, the bottom signal stops pulses at low mains but reactivates them when V_{CC} = 15 V.

Figure 33.



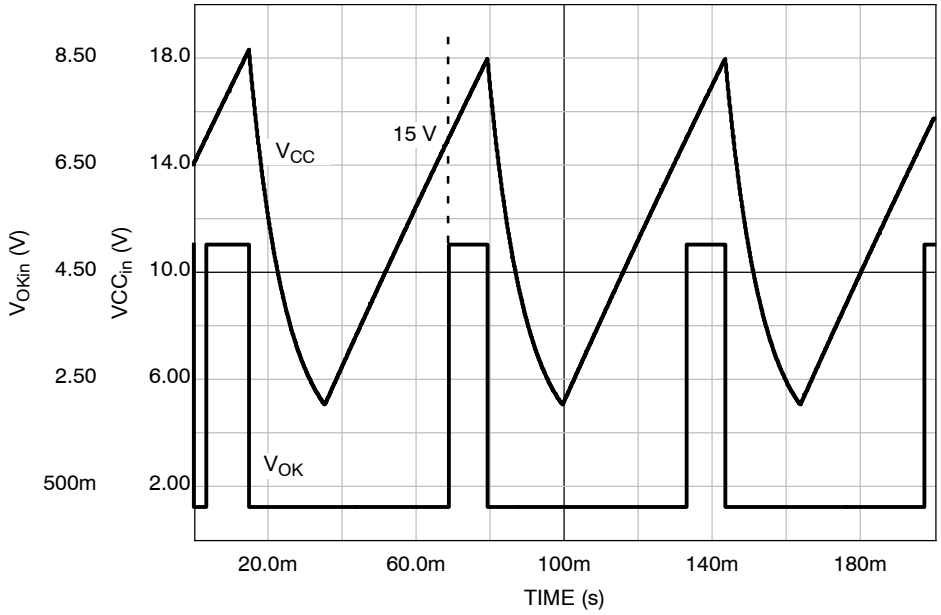
The B_{OK} comes back in the descent but the logic waits until the UVOL circuitry detects 15 V to restart the controller.

Figure 34.



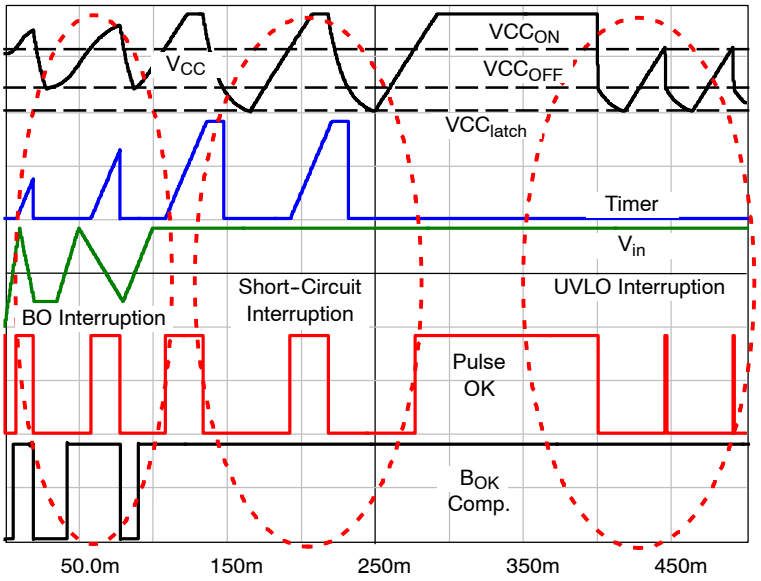
The B_{OK} comes back in the upslope but the logic 2 waits until UVOL circuitry detects 15 V to restart the Controller.

Figure 35.



In short−circuit, the V_{CC} drops to VCC_{latch} and goes up to 15 V. The blue trace corresponds to the “ok to pulse” signal whose duration is given by the fault timer (purposely reduced on this simulation). Should a VCC_{OFF} condition be detected, or a B_{OK} fault, the duration would be accordingly truncated.

Figure 36.



A mix of conditions, BO, short−circuit and UVLO fault are represented on this diagram. In BO, the pulses (pulse ok signal) are started at V_{CC} = 15 V and there is no latch−off phase. In short−circuit, pulses are stopped by the timer and finally, in a UVLO conditions (not a short−circuit), there is a latch−off phase but the timer is flat since there is no short−circuit.

Figure 37.

PFC Behavior During BO Conditions

During brown−out, the PFC is disabled; otherwise the PFC controller consumption would prevent the charging of the V_{CC} capacitor. The PFC will be shutdown until BO comes back and a clean startup sequence has properly ended.

Soft−start

The NCP1381/82 features a soft−start activated during the power on sequence (P_{ON}) and in short−circuit conditions to lower the acoustical noise in the transformer. As soon as V_{CC} reaches 15 V, the peak current is gradually increased from nearly zero up to the maximum clamping level (e.g. 0.8 V / R_{sense}). Every restart attempt is followed by a soft−start activation.

A shorter soft−start is also activated during the skip cycle condition to implement our soft−burst. This Soft−Skip is cancelled whenever a fault condition appears, in order not to degrade the transient behavior in case of load transients when the controller is initially in skip mode.

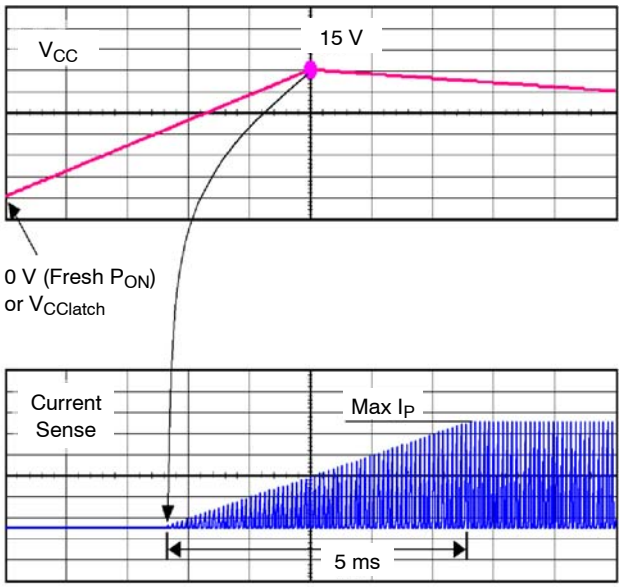
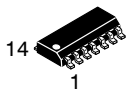


Figure 38. Soft−Start is Activated During a Startup Sequence or an OCP Condition

Soft−Skip is a trademark of Semiconductor Components Industries, LLC (SCILLC).

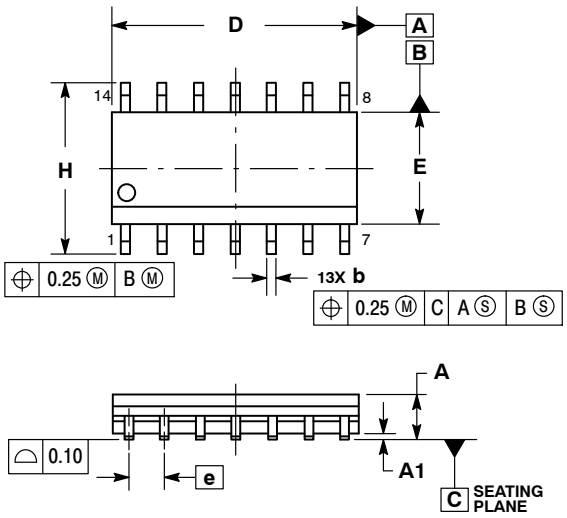
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

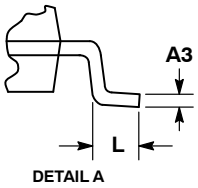


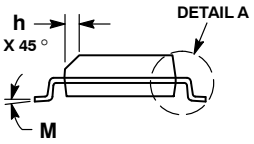
SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



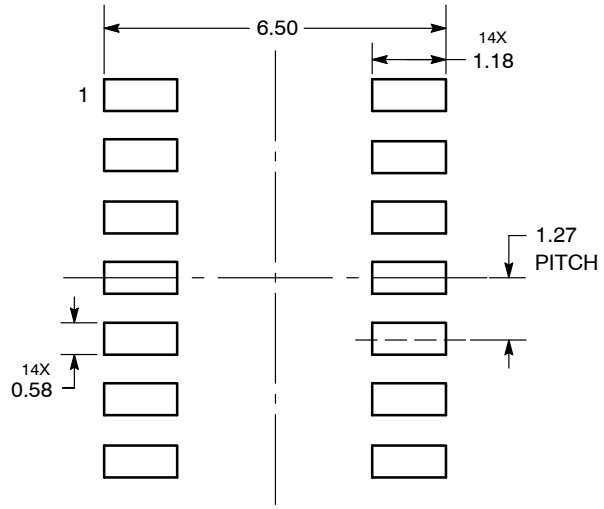




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

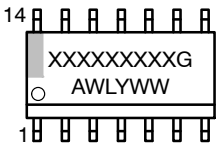
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−14 NB**		**PAGE 1 OF 2**

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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