NCP1850

Fully Integrated Li-Ion Switching Battery Charger with Power Path Management and USB On-The-Go Support

The NCP1850 is a fully programmable single cell Lithium−ion switching battery charger optimized for charging from a USB compliant input supply and AC adaptor power source. The device integrates a synchronous PWM controller, power MOSFETs, and the entire charge cycle monitoring including safety features under software supervision. An optional battery FET can be placed between the system and the battery in order to isolate and supply the system. The NCP1850 junction temperature and battery temperature are monitored during charge cycle, and both current and voltage can be modified accordingly through I^2C setting. The charger activity and status are reported through a dedicated pin to the system. The input pin is protected against overvoltages.

The NCP1850 also provides USB OTG support by boosting the battery voltage as well as providing overvoltage protected power supply for USB transceiver.

Features

- 1.5 A Buck Converter with Integrated Pass Devices
- Input Current Limiting to Comply to USB Standard
- Automatic Charge Current for AC Adaptor Charging
- High Accuracy Voltage and Current Regulation
- Input Overvoltage Protection up to +28 V
- Factory Mode
- 250 mA Boosted Supply for USB OTG Peripherals
- Reverse Leakage Protection Prevents Battery Discharge
- Protected USB Transceiver Supply Switch
- Dynamic Power Path with Optional Battery FET
- Battery Temperature Sensing for Safe Operation
- Silicon Temperature Supervision for Optimized Charge Cycle
- Safety Timers
- Flag Output for Charge Status and Interrupts
- INTB Output for Interrupts
- I^2C Control Bus up to 3.4 MHz
- Small Footprint 2.2 x 2.55 mm CSP Package
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Smart Phone
- Handheld Devices
- Tablets
- PDAs

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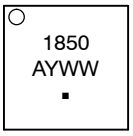
WLCSP25
CASE 567FZ

MARKING DIAGRAM



1850	= Specific Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
▪	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 29 of this data sheet.

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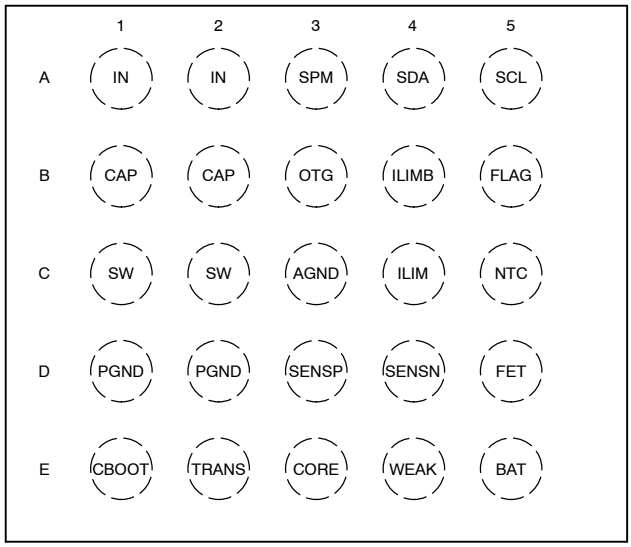
Publication Order Number:
NCP1850/D

PIN CONNECTIONS



(Top View)

Figure 1. Package Outline CSP

Table 1. PIN FUNCTION DESCRIPTION

Pin	Name	Type	Description
A1	IN	POWER	Battery Charger Input. These two pins must be decoupled by at least 1 μF capacitor and connected together.
A2	IN	POWER	
A3	SPM	DIGITAL INPUT	System Power Monitor input.
A4	SDA	DIGITAL BIDIRECTIONAL	I^2C data line
A5	SCL	DIGITAL INPUT	I^2C clock line
B1	CAP	POWER	CAP pin is the intermediate power supply input for all internal circuitry. Bypass with at least 4.7 μF capacitor. Must be tied together.
B2	CAP	POWER	
B3	OTG	DIGITAL INPUT	Enables OTG boost mode. OTG = 0, the boost is powered OFF OTG = 1 turns boost converter ON
B4	ILIMB	OPEN DRAIN OUTPUT	Connect to interrupt pin of the system, active low
B5	FLAG	OPEN DRAIN OUTPUT	Charging state active low. This is an open drain pin that can either drive a status LED or connect to interrupt pin of the system.
C1	SW	ANALOG OUTPUT	Connection from power MOSFET to the Inductor. These pins must be connected together.
C2	SW	ANALOG OUTPUT	
C3	AGND	ANALOG GROUND	Analog ground / reference. This pin should be connected to the ground plane and must be connected together.
C4	ILIM	DIGITAL INPUT	Input current limiter level selection (can be defeated by I^2C).
C5	NTC	ANALOG INPUT	Input for the battery NTC (10 KΩ / B = 3900) or (4.7 KΩ / B = 3900) If not used, this pin must be tied to GND to configure the NCP1850 and warn that NTC is not used.
D1	PGND	POWER GND	Power ground. These pins should be connected to the ground plane and must be connected together.
D2	PGND	POWER GND	
D3	SENSP	ANALOG INPUT	Current sense input. This pin is the positive current sense input. It should be connected to the R_{SENSE} resistor positive terminal.

Table 1. PIN FUNCTION DESCRIPTION

Pin	Name	Type	Description
D4	SENSN	ANALOG INPUT	Current sense input. This pin is the negative current sense input. It should be connected to the R_{SENSE} resistor negative terminal. This pin is also voltage sense input of the voltage regulation loop when the FET is present and open.
D5	FET	ANALOG OUTPUT	Battery FET driver output. When not used, this pin must be directly tied to ground.
E1	CBOOT	ANALOG IN/OUT	Floating Bootstrap connection. A 10 nF capacitor must be connected between CBOOT and SW.
E2	TRANS	ANALOG OUTPUT	Output supply to USB transceiver. This pin can source a maximum of 30 mA to the external USB PHY or any other IC that needs +5 V USB. This pin is Overvoltage protected and will never be higher than 5.5 V. This pin should be bypassed by a 100 nF ceramic capacitor.
E3	CORE	ANALOG OUTPUT	5 V reference voltage of the IC. This pin should be bypassed by a 2.2 μF capacitor. No load must be connected to this pin.
E4	WEAK	ANALOG OUTPUT	Weak battery charging current source input.
E5	BAT	ANALOG INPUT	Battery connection

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IN (Note 1)	V_{IN}	−0.3 to +28	V
CAP (Note 1)	V_{CAP}	−0.3 to +28	V
Power balls: SW, CBOOT (Note 1)	V_{PWR}	−0.3 to +24	V
IN pin with respect to VCAP	V_{IN_CAP}	−0.3 to +7.0	V
SW with respect to SW	V_{SW_CAP}	−0.3 to +7.0	V
Sense/Control balls: SENSP, SENSN, VBAT, FET, TRANS, CORE, NTC, FLAG, INTB and WEAK. (Note 1)	V_{CTRL}	−0.3 to +7.0	V
Digital Input: SCL, SDA, SPM, OTG, ILIM (Note 1) Input Voltage Input Current	 V_{DG} I_{DG}	 −0.3 to +7.0 V 20	 V mA
Human Body Model (HBM) ESD Rating are (Note 2)	ESD HBM	2000	V
Machine Model (MM) ESD Rating are (Note 2)	ESD MM	200	V
Latch up Current (Note 3): All Digital pins(V_{DG}), FET All others pins.	I_{LU}	 10 ±100	mA
Storage Temperature Range	T_{STG}	−65 to + 150	°C
Maximum Junction Temperature (Note 4)	T_J	−40 to + TSD	°C
Moisture Sensitivity (Note 5)	MSL	Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. With respect to PGND. According to JEDEC standard JESD22−A108
2. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114 for all pins.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115 for all pins.
3. Latch up Current Maximum Rating: ±100 mA or per ±10 mA JEDEC standard: JESD78 class II.
4. A thermal shutdown protection avoids irreversible damage on the device due to power dissipation. See Electrical Characteristics.
5. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020.

Table 3. OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Operational Power Supply (Note 6)		3		V_{INOV}	V
V_{DG}	Digital input voltage level		0		5.5	V
T_A	Ambient Temperature Range		−40	25	+85	°C
I_{SINK}	FLAG sink current				10	mA
C_{IN}	Decoupling input capacitor			1		μF
C_{CAP}	Decoupling Switcher capacitor			4.7		μF
C_{CORE}	Decoupling core supply capacitor			2.2		μF
C_{OUT}	Decoupling system capacitor			10		μF
L_X	Switcher Inductor			2.2		μH
R_{SNS}	Current sense resistor			68		mΩ
$R_{\theta JA}$	Thermal Resistance Junction−to−Air	(Notes 7 and 8)		60		°C/W
T_J	Junction Temperature Range		−40	25	+125	°C

6. OVLO is selectable per metal option (see ELECTRICAL CHARACTERISTICS table).
7. A thermal shutdown protection avoids irreversible damage on the device due to power dissipation. See Electrical Characteristics.
8. The $R_{\theta JA}$ is dependent on the PCB heat dissipation. Board used to drive this data was a 2s2p JEDEC PCB standard.

Table 4. ELECTRICAL CHARACTERISTICS
Min & Max Limits apply for T_A between −40°C to +85°C and T_J up to + 125°C for V_{IN} between 3.6 V to 7 V (Unless otherwise noted). Typical values are referenced to T_A = + 25°C and V_{IN} = 5 V (Unless otherwise noted).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
INPUT VOLTAGE							
V_{INDET}	Valid input detection threshold	V_{IN} rising		3.55	3.6	3.65	V
		V_{IN} falling		2.95	3.0	3.05	V
V_{BUSUV}	USB under voltage detection	V_{IN} falling		4.3	4.4	4.5	V
		Hysteresis		50	100	150	mV
V_{BUSOV}	USB over voltage detection	V_{IN} rising		5.55	5.65	5.75	V
		Hysteresis		25	75	125	mV
V_{INOV} V_{INOV}	Valid input high threshold	V_{IN} rising		7.1	7.2	7.3	V
		Hysteresis		200	300	400	mV
INPUT CURRENT LIMITING							
I_{INLIM}	Input current limit	V_{IN} = 5 V	I_{INLIM} set to 100 mA	70	85	100	mA
			I_{INLIM} set to 500 mA	425	460	500	mA
			I_{INLIM} set to 900 mA	800	850	900	mA
			I_{INLIM} set to 1500 mA	1.4	1.45	1.5	A
INPUT SUPPLY CURRENT							
I_{Q_SW}	VBUS supply current	No load, Charger active state			15		mA
I_{OFF}		Charger not active, NTC disable			500		μA
CHARGER DETECTION							
V_{CHGDET}	Charger detection threshold voltage	$V_{IN} - V_{SENSN}$, V_{IN} rising		50		200	mV
		$V_{IN} - V_{SENSN}$, V_{IN} falling		10		50	
REVERVE BLOCKING CURRENT							
I_{LEAK}	V_{BAT} leakage current	Battery leakage, V_{BAT} = 4.2 V V_{IN} = 0 V, SDA = SCL = 0 V			5	7	μA
R_{RBFET}	Input RBFET On resistance (Q1)	Charger active state, Measured between IN and CAP,V_{IN} = 5 V		–	45	90	mΩ
BATTERY AND SYSTEM VOLTAGE REGULATION							
V_{CHG}	Output voltage range	Programmable by I^2C		3.3		4.5	V
		Default value			3.6		
	Voltage regulation accuracy	Constant voltage mode, T_A = 25°C		−0.5		0.5	%
				−1		1	
	I2C Programmable granularity				25		mV
BATTERY VOLTAGE THRESHOLD							
V_{SAFE}	Safe charge threshold voltage	V_{BAT} rising		2.1	2.15	2.2	V
V_{PRE}	Conditioning charge threshold voltage	VFET = 3.1 V and 3.2 V		2.95	3	3.05	V
		VFET = 3.3 V, 3.4 V, 3.5 V and 3.6 V		3.15	3.2	3.25	

9. Minimum transition time from states to states.

Table 4. ELECTRICAL CHARACTERISTICS
Min & Max Limits apply for T_A between −40°C to +85°C and T_J up to + 125°C for V_{IN} between 3.6 V to 7 V (Unless otherwise noted). Typical values are referenced to T_A = + 25°C and V_{IN} = 5 V (Unless otherwise noted).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
BATTERY VOLTAGE THRESHOLD							
V_{FET}	End of weak charge threshold voltage	V_{BAT} rising	Voltage range	3.15	3.2	3.25	V
			Default value		3.4		
			Accuracy	−2		2	%
			I^2C Programmable granularity		100		mV
V_{RECHG}	Recharge threshold voltage	Relative to V_{CHG} setting register			97		%
V_{BUCKOV}	Overvoltage threshold voltage	V_{BAT} rising, relative to V_{CHG} setting register, measured on SENSN or SENSP, Q_{BAT} close or no Q_{BAT}			115		%
		Q_{BAT} open.			5		V
CHARGE CURRENT REGULATION							
I_{CHG}	Charge current range	Programmable by I^2C		400		1600	mA
		Default value		950	1000	1050	mA
	Charge current accuracy			−50		50	mA
	I^2C Programmable granularity				100		mA
I_{PRE}	Pre−charge current	$V_{BAT} < V_{PRE}$		405	450	495	mA
I_{SAFE}	Safe charge current	$V_{BAT} < V_{SAFE}$		8	10	12	mA
I_{WEAK}	Weak battery charge current	BATFET present, $V_{SAFE} < V_{BAT} < V_{FET}$		80	100	120	mA
CHARGE TERMINATION							
I_{EOC}	Charge current termination	$V_{BAT} \geq V_{RECHG}$	Current range	100		275	mA
			Default value		150		
			Accuracy, I_{EOC} < 200 mA	−25		25	
			I^2C Programmable granularity		25		
FLAG							
V_{FOL}	FLAG output low voltage	I_{FLAG} = 10 mA				0.5	V
I_{FLEAK}	Off−state leakage	V_{FLAG} = 5 V				1	μA
DIGITAL INPUT (V_{DG})							
V_{IH}	High−level input voltage			1.2			V
V_{IL}	Low−level input voltage					0.4	V
R_{DG}	Pull down resistor				500		kΩ
I_{DLEAKK}	Input current	V_{DG} = 0 V		−0.5		0.5	μA
I^2C							
V_{SYSUV}	CAP pin supply voltage	I^2C registers available		2.5			V
V_{I^2CINT}*	High level at SCL/SCA line			1.7		5	V
V_{I^2CIL}	SCL, SDA low input voltage					0.4	V
V_{I^2CIH}	SCL, SDA high input voltage			0.8 * V_{I^2CINT}			V

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I²C						
V_{I^2COL}	SCL, SDA low output voltage	I_{SINK} = 3 mA			0.3	V
F_{SCL}	I²C clock frequency				3400	kHz
JUNCTION THERMAL MANAGEMENT						
T_{SD}	Thermal shutdown	Rising	125	140	150	°C
		Falling		115		°C
T_{H2}	Hot temp threshold 2	Relative to T_{SD}		−7		°C
T_{H1}	Hot temp threshold 1	Relative to T_{SD}		−11		°C
T_{WARN}	Thermal warning	Relative to T_{SD}		−15		°C
BATTERY THERMAL MANAGEMENT						
V_{NTCRMV}	Battery removed threshold voltage	V_{NTC} Rising	2.3	2.325	2.4	V
V_{COLD}	Battery cold temperature corresponding voltage threshold	BATCOLD[1:0]:00	1.775	1.8	1.825	
		BATCOLD[1:0]:01	1.7	1.725	1.75	
		BATCOLD[1:0]:10	1.625	1.65	1.675	
		BATCOLD[1:0]:11	1.55	1.575	1.6	
V_{HOT}	Battery hot temperature corresponding voltage threshold	BATHOT[1:0]:00	800	825	850	mV
		BATHOT[1:0]:01	725	750	775	
		BATHOT[1:0]:10	650	675	700	
		BATHOT[1:0]:11	575	600	625	
V_{NTCDIS}	NTC disable corresponding voltage threshold	V_{NTC} Falling	50	75	100	mV
V_{REG}	Internal voltage reference		2.35	2.4	2.45	V
R_{NTCPU}	Internal resistor pull up		9.8	10	10.2	kΩ
BUCK CONVERTER						
F_{SWCHG}	Switching Frequency		–	3	–	MHz
	Switching Frequency Accuracy		−10		+10	%
T_{DTYC}	Max Duty Cycle	Average		99.5		%
I_{PKMAX}	Maximum peak inductor current			1.9		A
R_{ONLS}	Low side Buck MOSFET R_{DSON} (Q3)	Measured between PGND and SW, V_{IN} = 5 V	–	170	350	mΩ
R_{ONHS}	High side Buck MOSFET R_{DSON}(Q2)	Measured between CAP and SW, V_{IN} = 5 V	–	140	285	mΩ
PROTECTED TRANSCEIVER SUPPLY						
V_{TRANS}	Voltage on TRANS pin	$V_{IN} \geq 5$ V		5	5.5	V
I_{TRMAX}	TRANS current capability		30			mA
TIMING						
T_{WD}	Watchdog timer			32		s
T_{USB}	USB timer			2048		s

9. Minimum transition time from states to states.

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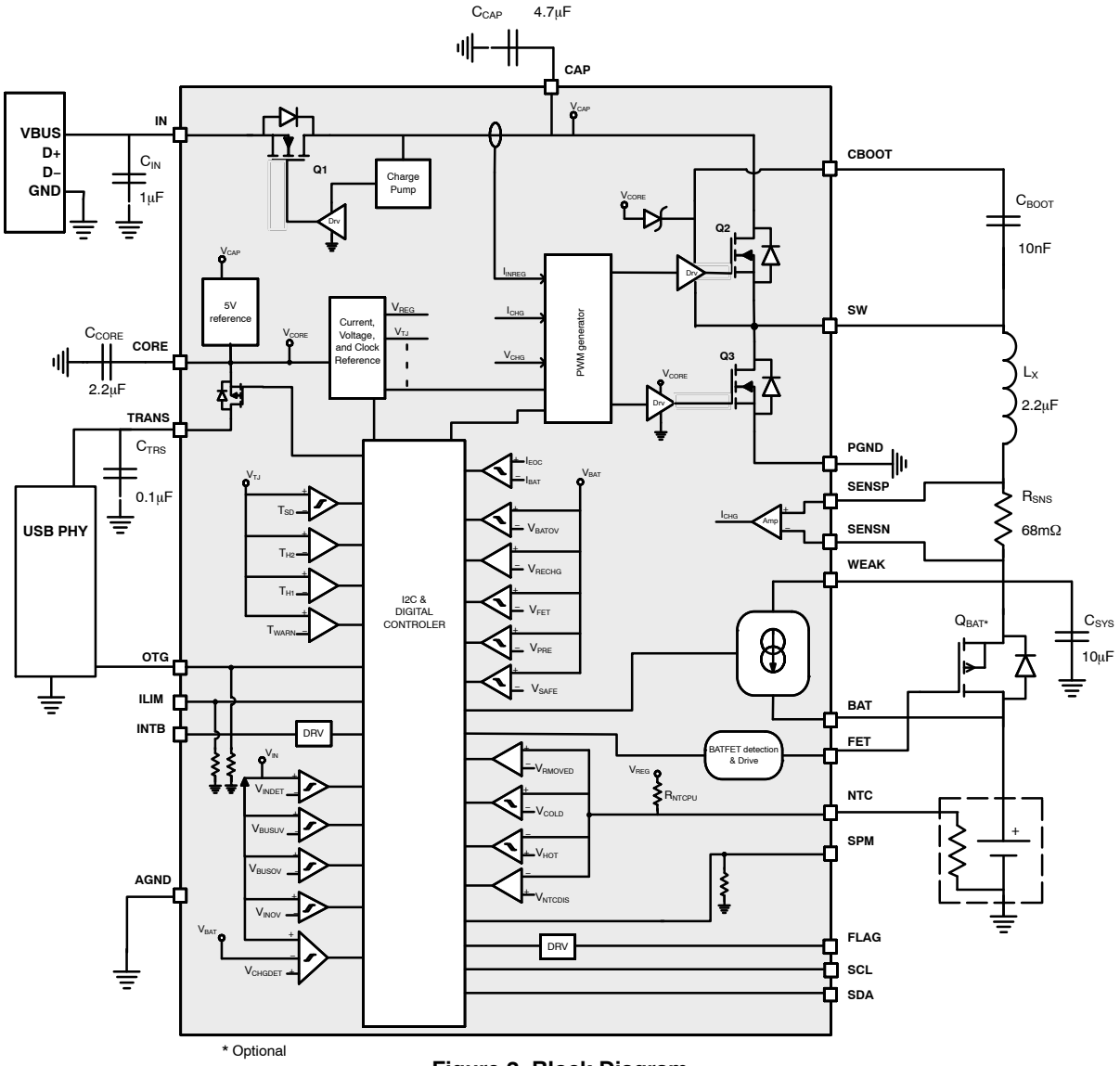
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TIMING							
T_{CHG1}	Charge timer	Safe−charge or pre−charge or weak−safe or weak− charge state.			3		h
T_{CHG2}		Full−charge state			2		h
T_{WU}	Wake−up timer				64		s
T_{VRCHR}	Deglitch time for end of charge voltage detection	V_{BAT} rising			15		ms
		V_{BAT} falling			127		ms
T_{INDET}	Deglitch time for input voltage detection	V_{IN} rising			15		ms
T_{DGS1}	Deglitch time for signal crossing I_{EOC}, V_{PRE}, V_{SAFE}, V_{CHGDET}, V_{INEXT} thresholds.	Rising and falling edge			15		ms
T_{DGS2}	Deglitch time for signal crossing V_{FET}, V_{BUSUV}, V_{BUSOV} thresholds.	Rising and falling edge			1		ms
T_{STWC}	Charger state timer (Note 9)	From Weak Charge to Full Charge State			32		s
T_{STW}		From Wait to Charger active state			128		ms
T_{ST}		From Weak Charge to Full Charge State, triggered on TST_SET level transition.	TST_SET = 0		32	24	s
			TST_SET = 1		16		ms
		All others states			16		ms
BOOST CONVERTER AND OTG MODE							
V_{IBSTL}	Boost minimum input operating range	Boost start−up		3.1	3.2	3.3	V
		Boost running		2.9	3	3.1	
V_{IBSTH}	Boost maximum input operating range			4.4	4.5	4.6	V
V_{OBST}	Boost Output Voltage	DC value measured on CAP pin, no load		5.00	5.1	5.15	V
V_{OBSTAC}	Boost Output Voltage accuracy	Measured on CAP pin Including line and load regulation		−3		3	%
I_{BSTMX}	Output current capability			250			mA
F_{SWBST}	Switching Frequency				1.5		MHz
	Switching Frequency Accuracy			−10		10	%
I_{BPKM}	Maximum peak inductor current				1.9		A
V_{OBSTOL}	Boost overload	Boost running, voltage on IN pin		4.3	4.4	4.5	V
T_{OBSTOL}		Maximum capacitance on IN pin during start−up			10		μF
R_{OBSTOL}		Maximum load on IN pin during start−up			50		Ω
V_{OBSTOV}	Overvoltage protection	V_{IN} rising		5.55	5.65	5.75	V
		Hysteresis		25	75	125	mV

9. Minimum transition time from states to states.

BLOCK DIAGRAM



* Optional

Figure 2. Block Diagram

TYPICAL APPLICATION CIRCUITS

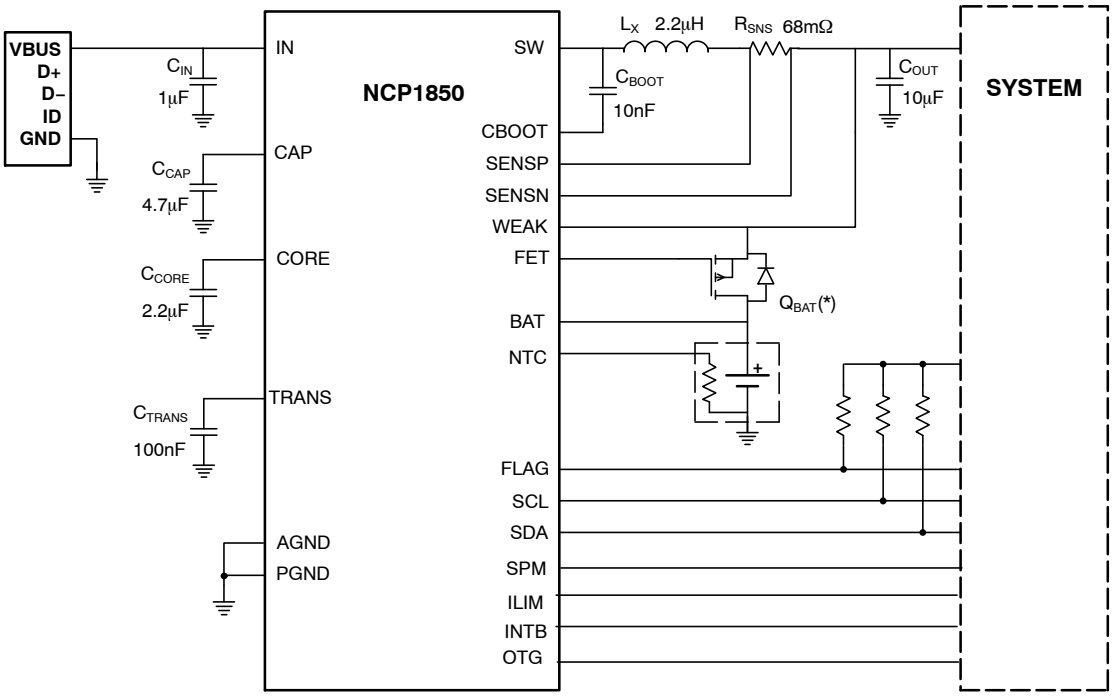


Figure 3. USB Charger with Battery External MOSFET

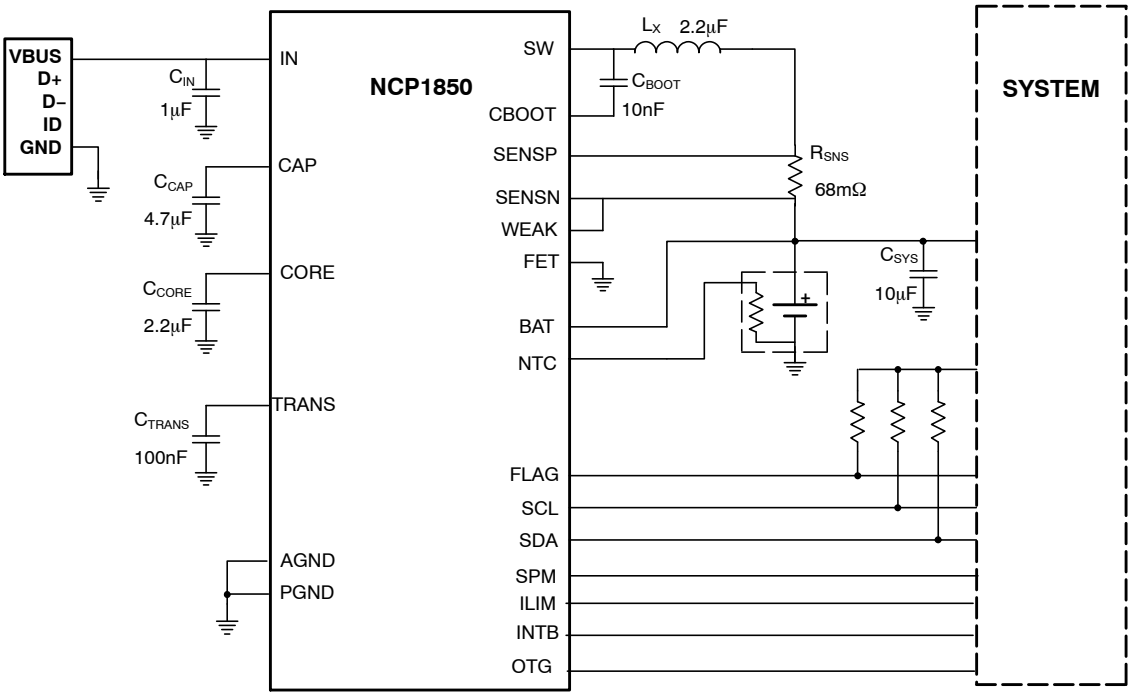


Figure 4. USB Charger without Battery External MOSFET

CHARGE MODE OPERATION

Overview

The NCP1850 is a fully programmable single cell Lithium−ion switching battery charger optimized for charging from a USB compliant input supply. The device integrates a synchronous PWM controller; power MOSFETs, and monitoring the entire charge cycle including safety features under software supervision. An optional battery FET can be placed between the system and the battery in order to isolate and supply the system in case of weak battery. The NCP1850 junction temperature and battery temperature are monitored during charge cycle and current and voltage can be modified accordingly through I^2C setting. The charger activity and status are reported through a dedicated pin to the system. The input pin is protected against overvoltages.

The NCP1850 is fully programmable through I^2C interface (see Registers Map section for more details). All registers can be programmed by the system controller at any time during the charge process. The charge current (I_{CHG}), charge voltage (V_{CHG}), and input current (I_{INLIM}) are controlled by a dynamic voltage and current scaling for disturbance reduction. Is typically 10 μs for each step.

NCP1850 also provides USB OTG support by boosting the battery voltage as well as an over voltage protected power supply for USB transceiver.

Charge Profile

In case of application without Q_{FET} (see Figure 4), the NCP1850 provides four main charging phases as described below. Unexpected behavior or limitations that can modify the charge sequence are described further (see Charging Process section).

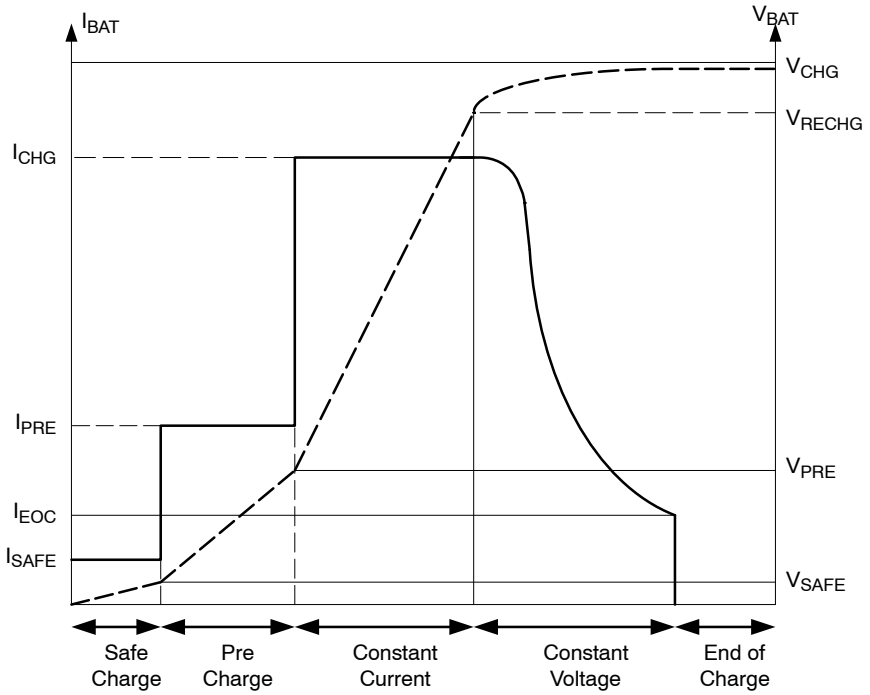


Figure 5. Typical Charging Profile of NCP1850

Safe Charge:

With a disconnected battery or completely empty battery, the charge process is in *safe charge* state, the charge current is set to I_{SAFE} in order to charge up the system's capacitors or the battery. When the battery voltage reaches V_{SAFE} threshold, the battery enters in pre−conditioning.

Pre Conditioning (pre−charge):

In preconditioning (pre *charge* state), the DC−DC convertor is enabled and an I_{PRE} current is delivered to the battery. This current is much lower than the full charge current. The battery stays in preconditioning until the V_{BAT} voltage is lower than V_{PRE} threshold.

Constant Current (full charge):

In the constant current phase (*full charge* state), the DC−DC convertor is enabled and an I_{CHG} current is delivered to the load. As battery voltage could be sufficient, the system may be awake and sink an amount of current. In this case the charger output load is composed of the battery and the system. Thus I_{CHG} current delivered by the NCP1850 is shared between the battery and the system: $I_{CHG} = I_{SYS} + I_{BAT}$.

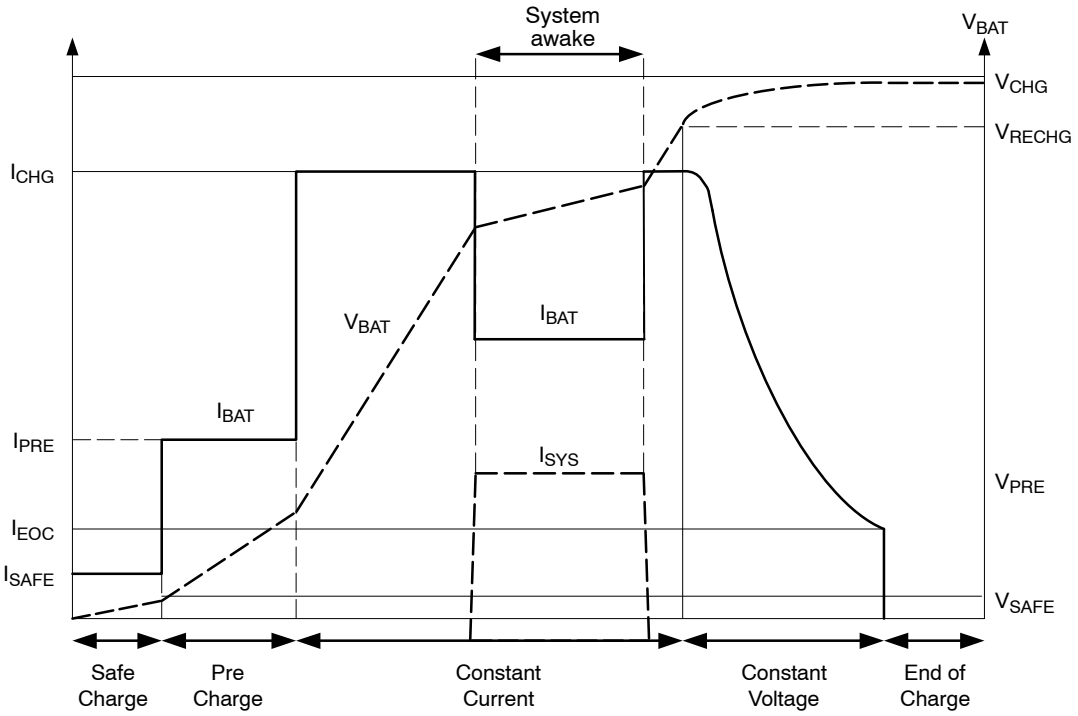


Figure 6. Typical Charging Profile of NCP1850 with System Awake

I_{CHG} current is programmable using I^2C interface (register IBAT_SET − bits ICHG[3:0]).

Constant Voltage (full charge):

The constant voltage phase is also a part of the *full charge* state. When the battery voltage is close to its maximum (V_{CHG}), the charge circuit will transition from a constant current to a constant voltage mode where the charge current will slowly decrease (taper off). The battery is now voltage controlled. V_{CHG} voltage is programmable using I^2C interface (register VBAT_SET− bits CTRL_VBAT[5:0]).

End of Charge:

The charge is completed (*end of charge* state) when the battery is above the V_{RECHG} threshold and the charge current below the I_{EOC} level. The battery is considered fully charged and the battery charge is halted. Charging is resumed in the constant current phase when the battery voltage drops below the V_{RECHG} threshold. I_{EOC} current is programmable using I^2C interface (register IBAT_SET− bits IEOC[2:0]).

The charge cycle can also be halted manually through I^2C (register CRTL2 bit CHG_HALT=1).

Power Stage Control

NCP1850 provides a fully−integrated 3 MHz step−down DC−DC converter for high efficiency. For an optimized charge control, three feedback signals controls the PWM duty cycle. These three loops are: maximum input current (I_{INLIM}), maximum charge current (I_{CHG}) and, maximum charge voltage (V_{CHG}). The switcher is regulated by the first loop that reaches its corresponding threshold. Typically during charge current phase ($V_{PRE} < V_{BAT} < V_{RECHG}$), the measured input current and output voltage are below the programmed limit and asking for more power. But in the same time, the measured output current is at the programmed limit and thus regulates the DC−DC converter.

In order to prevent battery discharge and overvoltage protection, Q1(reverse voltage protection) and Q2 (high side N−MOSFET of the DC−DC converter) are mounted in a back−to−back common drain structure while Q3 is the low side N MOSFET of the DC−DC converter. Q2 gate driver circuitry required an external bootstrap capacitor connected between CBOOT pin and SW pin.

An internal current sense monitors and limits the maximum allowable current in the inductor to I_{PEAK} value.

Charger Detection, Start−up Sequence and System Off

The start−up sequence begins upon an adaptor valid voltage plug in detection: $V_{IN} > V_{INDET}$ and $V_{IN} - V_{BAT} > V_{CHGDET}$ (*off* state).

Then, the internal circuitry is powered up and the presence of NTC and BATFET are reported (register STATUS – bit BATFET and NTC). When the power−up sequence is done, the charge cycle is automatically launched. At any time and any state, the user can holds the charge process and transit to *fault* state by setting CHG_EN to ‘0’ (register CTRL1) in the I^2C register. Furthermore, during *fault* state, NTC block can be disabled for power saving (bit NTC_EN register CTRL1)

The I2C registers are accessible without valid voltage on V_{IN} if $V_{CAP} > V_{SYSUV}$ (i.e. if V_{BAT} is higher than V_{SYSUV} + voltage drop across Q2 body diode).

At any time, the user can reset all register stack (register CTRL1 – bit REG_RST).

Weak Battery Support

An optional battery FET (Q_{BAT}) can be placed between the application and the battery. In this way, the battery can be isolated from the application and so−called weak battery operation is supported.

Typically, when the battery is fully discharged, also referred to as weak battery, its voltage is not sufficient to supply the application. When applying a charger, the battery first has to be pre−charged to a certain level before operation. During this time; the application is supplied by the DC−DC converter while integrated current sources will pre−charge the battery to the sufficient level before reconnecting.

The pin FET can drive a PMOS switch (Q_{BAT}) connected between BAT and WEAK pin. It is controlled by the charger state machine (Charging process section). The basic behavior of the FET pin is that it is always low. Thus the PMOS is conducting, except when the battery is too much discharged at the time a charger is inserted under the condition where the application is not powered on. The FET pin is always low for BAT above the V_{FET} threshold. Some exceptions exist which are described in the Charging Process and Power Path Management section. The V_{FET} threshold is programmable (register MISC_SET – bit CTRL_VFET).

Batfet Detection

The presence of a PMOS (Q_{BAT}) at the FET pin is verified by the charging process during its *config* state. To distinguish the two types of applications, in case of no battery FET the pin FET is to be tied to ground. In the *config* state an attempt will be made to raise the FET pin voltage slightly up to a detection threshold. If this is successful it is considered that a battery FET is present. The batfet detection is completed for the whole charge cycle and will be done again upon unplug condition ($V_{BAT} < V_{INDET}$ or $V_{IN} - V_{BAT} < V_{CHGDET}$) or register reset (register CTRL1– bit REG_RST).

Weak Wait

Weak wait state is entered from wait state (see *Charging process* section) in case of BATFET present, battery voltage lower than V_{FET} and host system in shutdown mode (SPM = 0). The DCDC converter from VIN to SW is enabled and set to V_{CHG} while the battery FET Q_{BAT} is opened. The system is now powered by the DC−DC. The internal current source to the battery is disabled. In weak wait state, the state machine verifies if the battery temperature is OK thanks to the NTC sensor. If NTC OK or if NTC is not present (NTC pin tied to 0), this state is left for weak safe state. In case of no battery, the NCP1850 stay in weak wait state (the system is powered by DC−DC).

Weak Safe

The voltage at V_{BAT}, is below the V_{SAFE} threshold. In *weak safe* state, the battery is charged with a linear current source at a current of I_{SAFE}. The DC−DC converter is enabled and set to V_{CHG} while the battery FET Q_{BAT} is opened. In case the ILIM pin is not made high or the input current limit defeated by I^2C before timer expiration, the state is left for the *safe charge* state after a certain amount of time (see Wake up Timer section). Otherwise, the state machine will transition to the *weak charge* state once the battery is above V_{SAFE}.

Weak Charge

The voltage at V_{BAT}, is above the V_{SAFE} threshold. The DC−DC converter is enabled and set to V_{CHG}. The battery is initially charged at a charge current of I_{WEAK} supplied by a linear current source from WEAK pin (i.e. DC−DC converter) to BAT pin. I_{WEAK} value is programmable (register MISC_SET bits IWEAK). The weak charge timer (see Wake up Timer section) is no longer running. When the battery is above the V_{FET} threshold (programmable), the state machine transitions to the *full charge* state thus BATFET Q_{BAT} is closed.

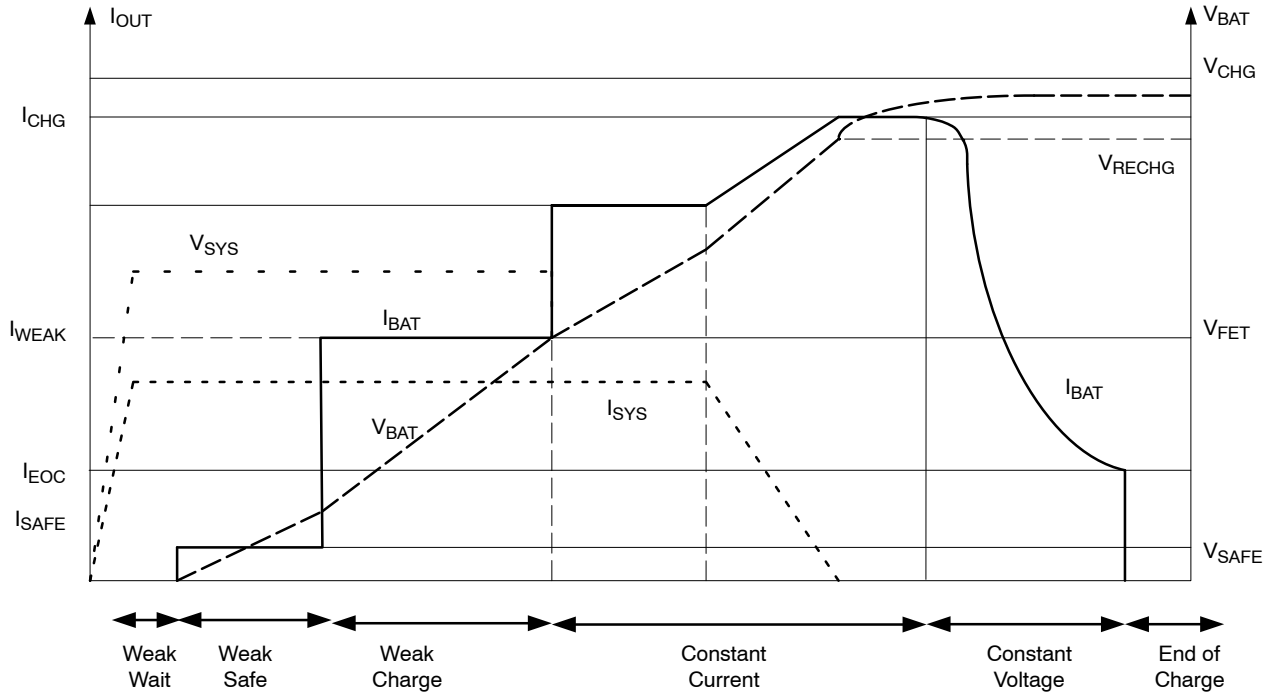


Figure 7. Weak Charge Profile

In some application cases, the system may not be able to start in *weak charge states* due to current capability limitation or/and configuration of the system. If so, in order to avoid unexpected "drop and retry" sequence of the buck output, the charge state machine allows only three system power−up sequences based on SPM pin level: If SPM pin level is toggled three times during *weak charge* states, the system goes directly to *safe charge* state and a *full charge mode* sequence is initiated ("Power fail" condition in Charging process section).

Power Path Management

Power path management can be supported when a battery FET (Q_{BAT}) is placed between the application and the battery. When the battery is fully charged (end of charge state), power path management disconnects the battery from the system by opening Q_{BAT}, while the DC−DC remains active. This will keep the battery in a fully charged state with the system being supplied from the DC−DC. If a load transient appears exceeding the DC−DC output current and thus causing V_{SENSEN} to fall below V_{RECHG}, the FET Q_{BAT} is instantaneously (Within T_{PPM}, see Electrical Characteristics) closed to reconnect the battery in order to provide enough current to the application. The FET Q_{BAT} remains closed until the end of charge state conditions are reached again or manually set through I^2C (register CRTL2 bit CHG_HALT = 1) . The power path management function is enabled through the I^2C interface (register CRTL2 bit PWR_PATH = 1).

Safety Timer Description

The safety timer ensures proper and safe operation during charge process. The set and reset condition of the different safety timer (Watchdog timer, Charge timer, Wakeup timer and USB timer) are detailed below. When a timer expires (condition "timeout" in Charging process section), the charge process is halted.

Watchdog Timer

Watchdog timer ensures software remains alive once it has programmed the IC. The watchdog timer is no longer running since I^2C interface is not available. Upon an I^2C write, automatically a watchdog timer T_{WD} is started. The watchdog timer is running during *charger active* states and *fault* state. Another I^2C write will reset the watchdog timer. When the watchdog times out, the state machine reverts to *fault* state and reported through I^2C interface (register CHINT2– bit WDTO). Also used to time out the *fault* state. This timer can be disabled (Register CTRL2 bit WDTO_DIS).

Charge Timer

A charge timer T_{CHG} is running that will make that the overall charge to the battery will not exceed a certain amount of energy. The charge timer is running during *charger active* states and halted during *charger not active* states (see Charging process section). The timer can also be cleared any time through I^2C (register CTRL1 – bit TCHG_RST). The state machine transitions to *fault* state when the timer expires. This timer can be disabled (Register CTRL2 bit CHGTO_DIS).

USB Timer

A USB charge timer T_{USB} is running in the *charger active* states while halted in the *charger non active* states. The timer keeps running as long as the lowest input current limit

remains selected either by ILIM pin or I²C (register I_SET – bit IINLIM and IINLIM_EN). This will avoid exceeding the maximum allowed USB charge time for un−configured connections. When expiring, the state machine will transition to *fault* state. The timer is cleared in the *off* state or by I²C command (register CTRL1 – bit TCHG_RST).

Wake up Timer

Before entering *weak charge* state, NCP1850 verifies if the input current available is enough to supply both the application and the charge of the battery. A wake−up timer T_{WU} verifies if ILIM pin is raised fast enough or application powered up (by monitoring register I_SET – bit IINLIM and IINLIM_EN level) after a USB attachment. The wake up timer is running in *weak wait* state and *weak safe* state and clears when the input current limit is higher than 100 mA.

Input current limitation

In order to be USB specification compliant, the input current at V_{IN} is monitored and could be limited to the I_{INLIM} threshold. The input current limit threshold is selectable through the ILIMx pin. When low, the one unit USB current is selected ($I_{IN} \leq 100$ mA), where when made high 5 units are selected ($I_{IN} \leq 500$ mA). In addition, this current limit can be programmed through I²C (register MISC_SET bits IINLIM) therefore defeating the state of the ILIMx pin. In case of non−limited input source, current limit can be disabled (register CTRL2 bit IINLIM_EN). The current limit is also disabled in case the input voltage exceeds the V_{BUSOV} threshold.

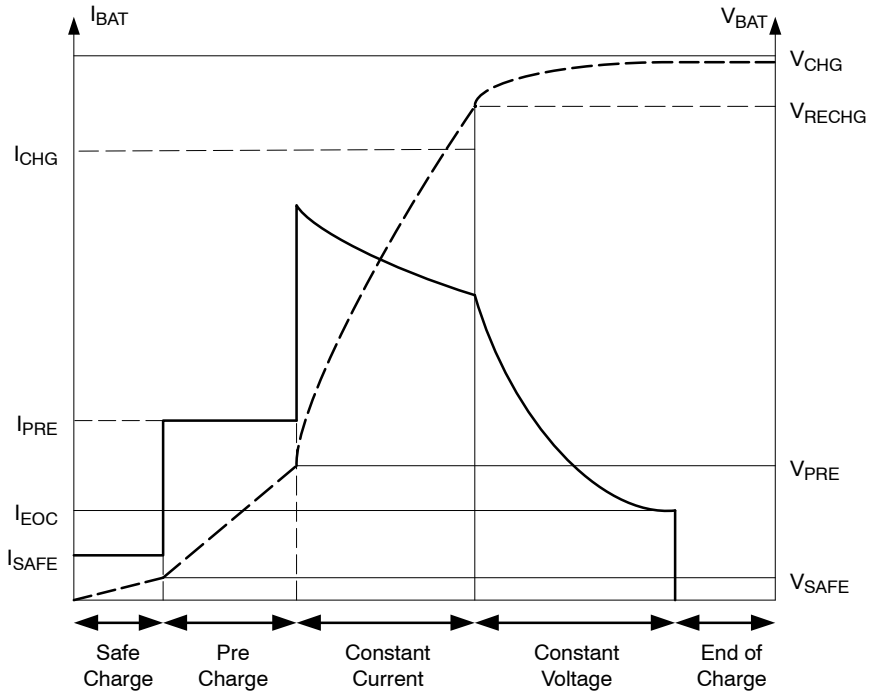


Figure 8. Typical Charging Profile of NCP1850 with Input Current Limit

Input Voltage Based Automatic Charge Current

If the input power source capability is unknown, automatic charge current will automatically increase the charge current step by step until the V_{IN} drops to V_{BUSUV}. Upon V_{BUSUV} being triggered, the charge current I_{CHG} is immediately reduced by 1 step and stays constant until V_{IN} drops again to V_{BUSUV}. The ICHG current is clamped to the I²C register value (register IBAT_SET, bits ICHG). This unique feature is enabled through I²C register (register CRTL2 bit AICL_EN).

Junction temperature management

During the charge process, NCP1850 monitors the temperature of the chip. If this temperature increases to T_{WARN}, an interrupt request (described in section Charge status reporting) is generated and bit TWARN_SNS is set to ‘1’ (register NTC_TH_SENSE). Knowing this, the user is free to halt the charge (register CTRL − bit CHG_EN) or reduce the charge current (register I_SET − bits ICHG). When chip temperature reaches T_{SD} value, the charge process is automatically halt.

Between T_{WARN} and T_{SD} threshold, a junction temperature management option is available by setting 1 to TJ_WARN_OPT bit (register CONTROL). In this case, if the die temperature hits T_{M1} threshold, an interrupt is generated again but NCP1850 will also reduce the charge current I_{CHG} by two steps or 200 mA. This should in most cases stabilize the die temperature because the power dissipation will be reduced by approximately 50 mW. If the die temperature increases further to hit T_{M2}, an interrupt is generated and the charge current is reduced to its lowest

level or 400mA. The initial charge current will be re−established when the die temperature falls below the T_{WARN} again.

If bit TJ_WARN_OPT = 0 (register CTRL1), the charge current is not automatically reduced, no current changes actions are taken by the chip until T_{SD}.

Battery Temperature Management

For battery safety, charging is not allowed for too cold or too hot batteries. The battery temperature is monitored through a negative temperature coefficient (NTC) thermistor mounted in the battery pack or on the phone PCB close to the battery pack. In some cases the NTC is handled by the platform and will not be connected to the charger IC.

NCP1850 provides a NTC pin for monitoring an external NTC thermistor. NTC pin is connected to an internal voltage V_{REG} through pull−up resistor (R_{NTCPU}). By connecting a NTC thermistor between NTC pin and GND, internal comparators can monitors voltage variation and provides temperature information to the state machine.

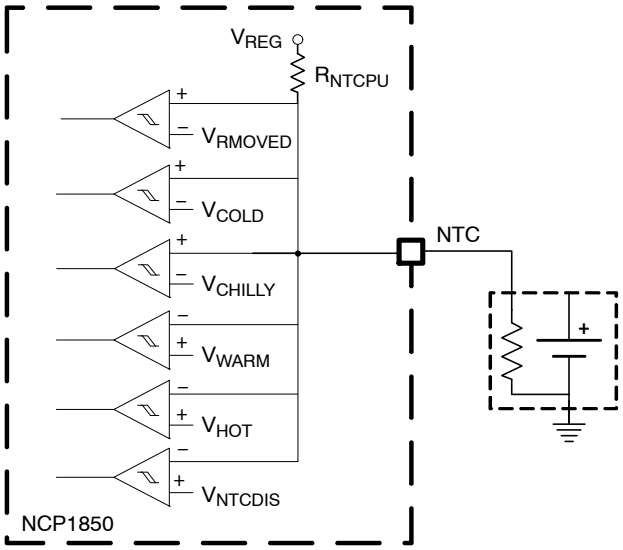


Figure 9. NTC Monitoring Circuit

Two thresholds ‘cold’ and ‘hot’ are provided those are programmable. The corresponding voltage levels of these thresholds are respectively V_{COLD} and V_{HOT}. Interrupts (describe in section Charge status reporting) are generated when crossing either threshold. The charge is halted outside the cold−hot window. In addition to the above, comparators monitor the NTC presence. When the NTC is removed ($V_{NTC} > V_{NTCRMV}$) , no more charge current is supplied to the battery and an interrupt is generated (describe in section Charge status reporting). This functionality can be disabled through programming (bit NTC_EN in register CTRL1). When the NTC is not used in the application the NTC pin can be tied to ground ($V_{NTC} < V_{NTCDIS}$) which will disable the battery temperature monitoring function.

Regulated Power Supply (Trans pin)

NCP1850 has embedded a linear voltage regulator (V_{TRANS}) able to supply up to I_{TRMAX} to external loads. This output can be used to power USB transceiver. Trans pin is enabled if a V_{BUS} valid is connected on input pin ($V_{BUSUV} < V_{IN} < V_{BUSOV}$) and can be disabled through I^2C (bit TRANS_EN_REG register CTRL2). A current limiter protects the IC in case of short circuit on TRANS pin.

Charge Status Reporting

Charge Status on FLAG Pin

FLAG pin is used to report charge status to the system processor and also for interruption request.

During *charger active* states and *wait* state, the pin FLAG is low in order to indicate that the charge of the battery is in progress. When charge is completed or disabled or a fault occurs, the FLAG pin is high as the charge is halted.

Interruption on FLAG pin

Upon any state or status change, the system controller can be informed by sensing FLAG pin. A T_{FLAGON} pulse is generated on this pin in order to signalize all events listed in the STAT_INT, CH1_INT, CH2_INT, BST_INT registers. All these bits are read to clear. The register map indicated the active transition of each bits (column “TYPE” Register Map section).

If more than 1 interrupt appears, only 1 pulse is generated while interrupt registers (STAT_INT, CH1_INT, CH2_INT, BST_INT) will not fully clear.

The level of this pulse depends on the state of the charger (see Charging process section):

- When charger in is charger active states and wait state the FLAG is low and consequently the pulse level on FLAG pin is high.
- In the others states, the pulse level is low as the FLAG stable level is high.

This Pulse can be globally masked due to the INT_FLG_MASK bit (Register CTRL1).

Interruption on INTB Pin

Upon any state or status change, the system controller can be informed by sensing INTB pin. This pin is tied low in order to signalize all events listed in the STAT_INT, CH1_INT, CH2_INT, BST_INT registers and can be individually masked with the corresponding mask bits in registers STAT_MSK, CH1_MSK, CH2_MSK and BST_MSK. All interrupt signals on INTB pin can be masked with the global interrupt mask bit (bit INT_MASK register CTRL1). All these bits are read to clear. The register indicated the active transition of each bits (column “TYPE” Register Map section).

If more than 1 interrupt appears, the INTB pin stay low while interrupt registers (STAT_INT, CH1_INT, CH2_INT, BST_INT) will not fully clear.

STATUS and CONTROL Registers

The status register contains the current charge state, NTC and BATFET connection as well as fault and status interrupt (bits INT_REG in register STATUS). The charge state (bits STATE in register STATUS) is updated on the fly and corresponds to the charging state describe in Charging Process section. An interruption (see description below) is generated upon a state change. In the config state, hardware detection is performed on BAFTET and NTC pins. From wait state, their statuses are available (bit BATFET and NTC in register STATUS). INT_REG bits are different to 0 if an interruption appears (see description below). Thanks to this register, the system controller knows the chip status with only one I^2C read operation. If a fault appears or a states change the controller can read corresponding registers for more details.

Sense and Status Registers

At any time the system processor can know the status of all the comparators inside the chip by reading VIN_SNS, VBAT_SNS, and TEMP_SNS registers (read only). These bits give to the system controller the real time values of all the corresponding comparators outputs (see BLOCK DIAGRAM).

Battery Removal and No Battery Operation

During normal charge operation the battery may bounce or be removed. The state transition of the state machine only occurs upon deglitched signals which allow bridging any battery bounce. True battery removal will last longer than the debounce times. The NCP1850 responses depend on NTC and BATFET presence:

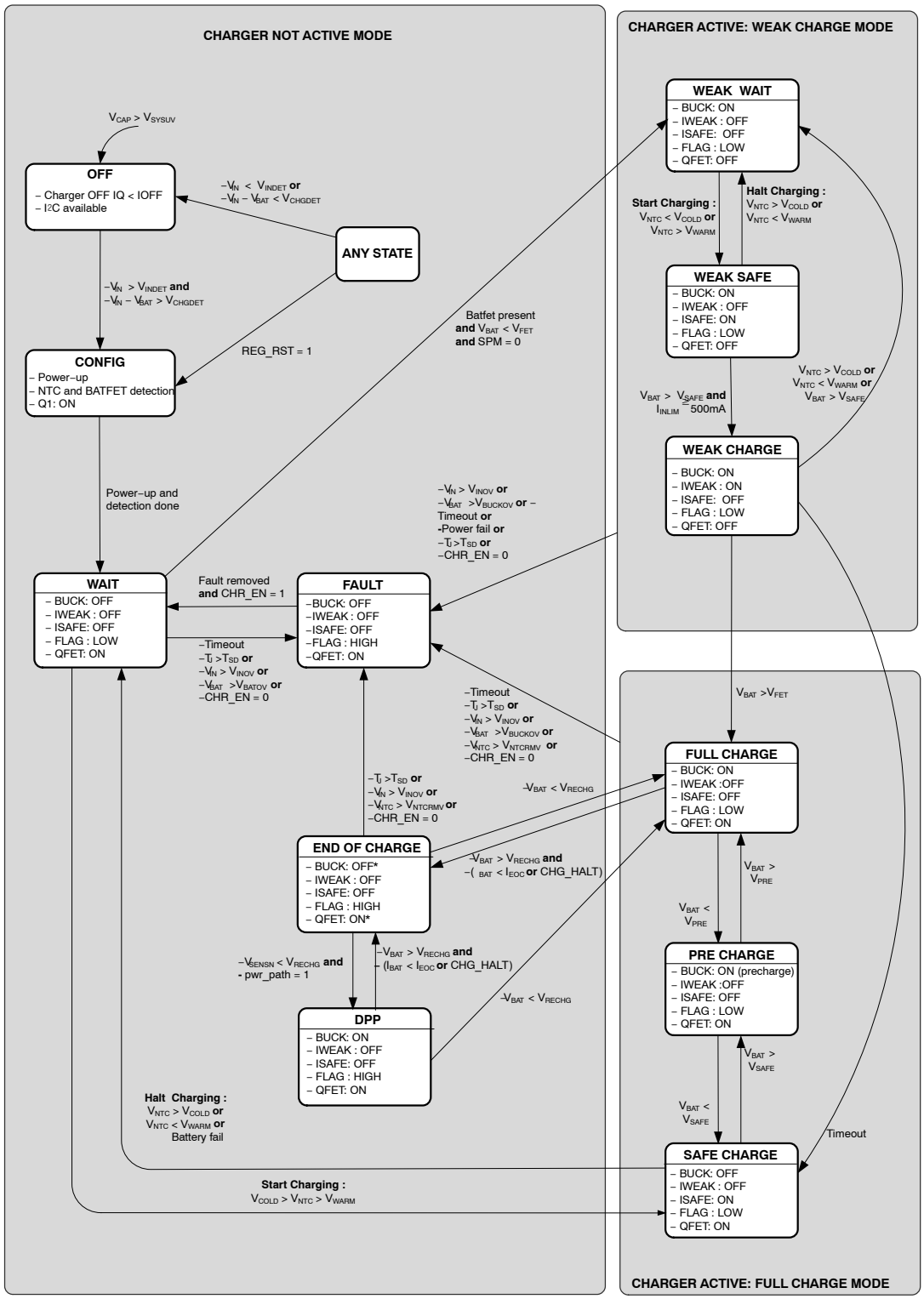
If the battery is equipped with an NTC its removal is detected ($V_{NTC} > V_{NTCRMV}$) and the state machine transits to *fault* state and an interrupt is generated (bit BATRMV register CH1_INT). Then, in case of applications with BATFET, the state machine will end up in *weak wait* state so the system is powered by the DC−DC converter (see Weak Wait section) without battery. In case of application without BATFET, the state machine will end up in *fault* state (DC−DC off) so the system is not powered.

With a battery pack without NTC support, the voltage at V_{BAT} will rapidly reach the DCDC converter setting V_{CHG} and then transition to *end of charge* state causing DC−DC off. Thus V_{BAT} falls (“Battery fail” condition in Charging Process section).

Factory Mode

During factory testing no battery is present in the application and a supply could be applied through the bottom connector to power the application. The state machine will support this mode of operation under the condition that the application includes a battery FET and uses batteries with NTC support (similar as no battery operation). In this case, the state machine will end up in *weak wait* state (see Weak Wait section). The application is supplied while the absence of the battery pack is interpreted as a battery pack out of temperature ($V_{NTC} > V_{COLD}$). Through I^2C the device is entirely programmable so the controller can configure appropriate current and voltage threshold for handle factory testing. Factory regulation mode (Register MISC_SET Bit FCTRY_MOD_REG) is accessible for factory testing purpose. In this mode, input and charge current loops are disabled, allowing full power to the system.

CHARGING PROCESS



* See Power Path Management section.

Figure 10. Detailed Charging Process

Boost Mode Operation

The DC−DC Converter can also be operated in a Boost mode where the application voltage is stepped up to the input V_{IN} for USB OTG supply. The converter operates in a 1.5 MHz fixed frequency PWM mode or in pulse skipping mode under low load condition. In this mode, where CAP is the regulated output voltage, Q3 is the main switch and Q2 is the synchronous rectifier switch. While the boost converter is running, the Q1 MOSFET is fully turned ON.

Boost Start−up

The boost mode is enabled through the OTG pin or I^2C (register CTRL1 – bit OTG_EN). Upon a turn on request, the converter regulates CAP pin, and the output voltage is present on IN pin through the Q1 MOSFET which is maintained close unless OVLO event. During start−up phase, if the IN pin cannot reach voltage higher than 4.65V within 16ms, then a fault is indicated to the system controller (bit VBUSILIM register BST_INT) and the boost is turns−off.

VIN Over−Voltage Protection

The NCP1850 contains integrated over−voltage protection on the V_{IN} line. During boost operation (V_{IN} supplied), if an over−voltage condition is detected ($V_{IN} > V_{BUSOV}$), the controller turns off the PWM converter. OTG_EN bit (register CTRL1) is set to 0 and a fault is indicated to the system controller (bit VBUSOV register BST_INT)

VIN Over−Current Protection

The NCP1850 contains over current protection to prevent the device and battery damage when V_{IN} is overloaded. When the IN voltage drops down to V_{BUSUV}, NCP1850 determine an over−current condition is met, so Q1 MOSFET and PWM converter are turned off. A fault is indicated to the system controller (bit VBUSILIM register BST_INT).

Battery Under−Voltage Protection

During boost mode, when the battery voltage is lower than the battery under voltage threshold ($V_{BAT} < V_{IBSTL}$), the IC turns off the PWM converter. A fault is indicated to the system controller (bit VBATLO register BST_INT)

A toggle on OTG pin or OTG_EN bit (register CTRL1) is needed to start again a boost operation.

Boost Status Reporting

STATUS and CTRL registers

The status register contains the boost status. Bits STATE in register STATUS gives the boost state to the system controller. Bits FAULTINT and STATINT in register STATUS are also available in boost mode. If a fault appears or a status changes (STATINT bits and FAULTINT) the processor can read corresponding registers for more details.

Interruption

In boost mode, valid interrupt registers are STAT_INT and BST_INT while CH1_INT and CH2_INT are tied to their reset value. Upon a state or status changes, the system controller is informed by sensing FLAG or INTB pins. Like in charge mode, T_{FLAGON} pulse is generated on FLAG pin and low level is applied on INTB pin in order to signalize the event. The pulse level is low as the FLAG level is high in boost mode. Charge state transition even and all signals of register BST_INT can generate an interrupt request on INTB pin and can be masked with the corresponding mask bits in register BST_MSK. All these bits are read to clear. The register map indicates the active transition of each bits (column “TYPE” in see Register Map section). If more than one interrupt appears, INTB stay low while interrupt registers (listed just above) will not fully clear.

Sense and status registers

At any time the system controller can know the status of all the comparator inside the chip by reading VIN_SNS and TEMP_SNS registers (read only). These bits give to the controller the real time values of all the corresponding comparators outputs (see BLOCK DIAGRAM).

I²C description

NCP1850 can support a subset of I²C protocol, below are detailed introduction for I²C programming.

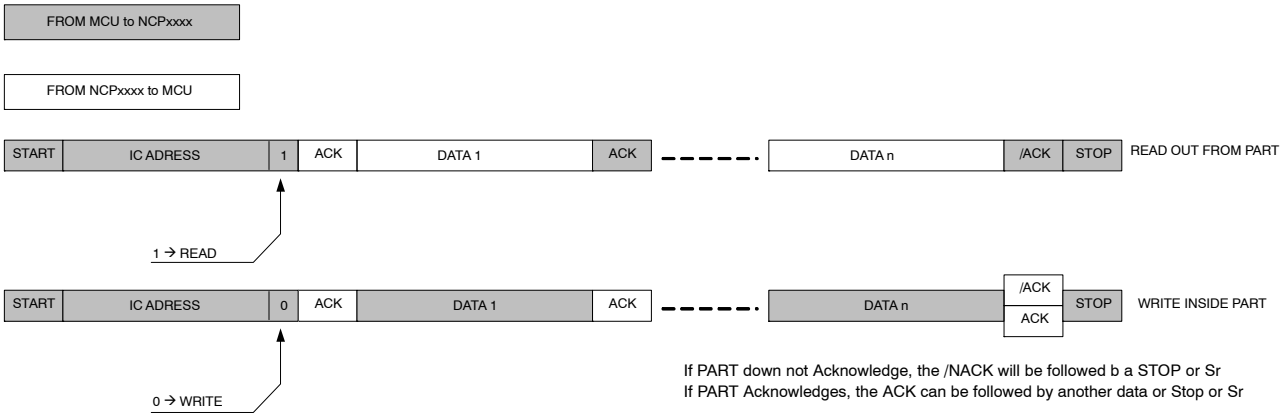


Figure 11. General Protocol Description

The first byte transmitted is the Chip address (with LSB bit sets to 1 for a read operation, or sets to 0 for a Write operation). Then the following data will be:

- In case of a Write operation, the register address (@REG) we want to write in followed by the data we will write in the chip. The writing process is incremental. So the first data will be written in @REG, the second one in @REG + 1 ¿. The data are optional.
- In case of read operation, the NCP1850 will output the data out from the last register that has been accessed by the last write operation. Like writing process, reading process is an incremental process.

Read Out from Part

The Master will first make a “Pseudo Write” transaction with no data to set the internal address register. Then, a stop then start or a Repeated Start will initiate the read transaction from the register address the initial write transaction has set:

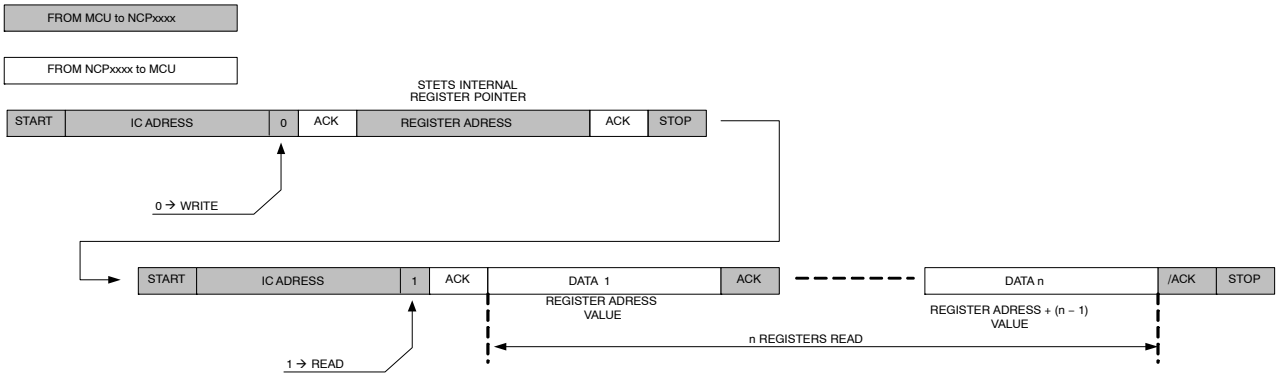


Figure 12. Read Out from Part

The first WRITE sequence will set the internal pointer on the register we want access to. Then the read transaction will start at the address the write transaction has initiated.

Write in Part:

Write operation will be achieved by only one transaction. After chip address, the MCU first data will be the internal register we want access to, then following data will be the data we want to write in Reg, Reg + 1, Reg + 2, ¿., Reg +n.

Write n Registers:

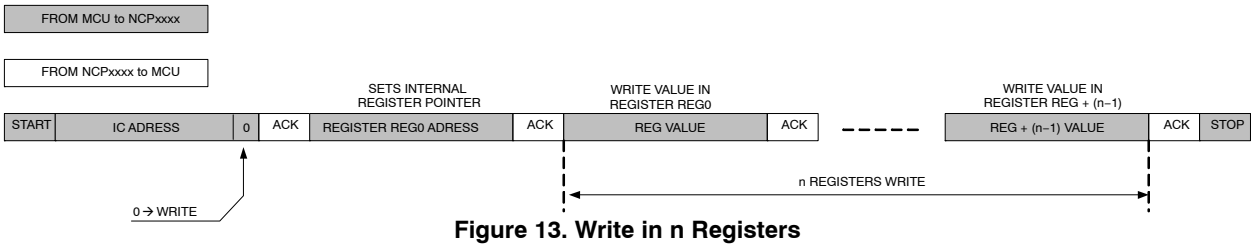


Figure 13. Write in n Registers

I²C Address

NCP1851 has fixed I²C but different I²C address (0$10, 7 bit address, see below table A7~A1), NCP1851 supports 7−bit address only.

Table 5. NCP1850 I²C ADDRESS

I²C Address (Note 10)	**Hex**	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
Default	$6C / $6D	0	1	1	0	1	1	0	X

10. Other addresses are available upon request.

Table 6. REGISTERS MAP

Bit	**Type**	**Reset**	**Name**	**RST Value**	**Function**
STATUS REGISTER − Memory Location: 00					
7 − 4	R	No_Reset	STATE[3:0]	0000	Charge mode: −0000: OFF −0001: WAIT + STBY −0010: SAFE CHARGE −0011: PRE CHARGE −0100: FULL CHARGE −0101: VOLTAGE CHARGE −0110: CHARGE DONE −0111: DPP −1000: WEAK WAIT −1001: WEAK SAFE −1010: WEAK CHARGE −1011: FAULT Boost mode: −1100: BOOST WAIT(s_WAIT) −1101: BOOST MODE (s_ON) −1110: BOOST FAULT(s_FAULT) −1111: BOOST OVER LOAD (s_OL))
3	R	No_Reset	BATFET	0	Indicate if a batfet is connected: 0: No BATFET is connected 1: BATFET is connected.
2	R	No_Reset	NTC	0	Indicate if a ntc resistor is present: 0: No NTC connected 1: NTC connected
1	R	No_Reset	STATINT	0	Status interrupt: 0: No status interrupt 1: Interruption flagged on STAT_INT register
0	R	No_Reset	FAULTINT	0	Fault interrupt: 0: No status interrupt 1: interruption flagged on CHRIN1, CHRIN2 or BST_INT register
CTRL1 REGISTER − Memory Location: 01					
7	RW	OFF STATE, POR, REG_RST	REG_RST	0	Reset: 0: No reset 1: Reset all registers

Table 6. REGISTERS MAP

Bit	Type	Reset	Name	RST Value	Function
CTRL1 REGISTER – Memory Location: 01					
6	RW	OFF STATE, POR, REG_RST	CHG_EN	1	Charge control: 0: Halt charging (go to fault state) or OTG operation 1: Charge enabled / Charge resume
5	RW	OFF STATE, POR, REG_RST, CHGMODE	OTG_EN	0	On the go enable: 0: no OTG operation 1: OTG operation (set by I2C or OTG pin)
4	RW	OFF STATE, POR, REG_RST	NTC_EN	1	ntc pin operation enable: 0:Battery temperature ignore, 1: Battery temperature modify the charge profile.
3	RW	OFF STATE, POR, REG_RST	TJ_WARN_OPT	0	Enable charge current vs Junction temperature 0: No current change versus junction temperature 1: Charge current is reduced when TJ is too high.
2	RW	OFF STATE, POR, REG_RST	CHG_HALT	0	Force End of Charge 0: Normal End of charge condition 1: Force EOC condition if VBAT > VRECHG
1	RW	OFF STATE, POR, REG_RST, TRM_RST	TCHG_RST	0	Charge timer reset: 0: no reset 1: Reset and resume charge timer (tchg timer)(self clearing)
0	RW	OFF STATE, POR, REG_RST	INT_MASK	1	INTB global interrupt mask 0: All Interrupts can be active. 1: All interrupts are not active
CTRL2 REGISTER – Memory Location: 02					
7	RW	OFF STATE, POR, REG_RST, OTGMODE	WDTO_DIS	0	Disable watchdog timer 0: Watchdog timer enable 1: Watchdog timer disable
6	RW	OFF STATE, POR, REG_RST, OTGMODE	CHGTO_DIS	0	Disable charge timer 0: Charge timer enable 1: Charge timer disable
5	RW	OFF STATE, POR, REG_RST, OTGMODE	PWR_PATH	0	Power Path Management: 0: Power Path disable 1: Power Path enable
4	RW	OFF STATE, POR, REG_RST	TRANS_EN_REG	1	Trans pin operation enable: 0 : Trans pin is still off 1 : Trans pin is supply
3	RW	OFF STATE, POR, REG_RST	INT_FLG_MASK	1	FLAG global interrupt mask 0 : All Interrupts are active. 1 : All interrupts are not active
2	RW	OFF STATE, POR, REG_RST, OTGMODE	IINSET_PIN_EN	1	Enable input current set pin: 0: Input current limit and AICL control by I^2C 1: Input current limit and AICL control by pins ILIMx
1	RW	OFF STATE, POR, REG_RST, OTGMODE	IINLIM_EN	1	Enable input current limit: 0: No input current limit 1: Input current limit is IINLIM[3:0]
0	RW	OFF STATE, POR, REG_RST, OTGMODE	AICL_EN	0	Enable automatic charge current: 0: No AICL 1: AICL
STAT_INT REGISTER – Memory Location: 03					
7–6	R	No_Reset	Reserved		
5	RCDual	OFF STATE, POR, REG_RST	TWARN	0	0: Silicon temperature is below TWARN threshold 1: Silicon temperature is above TWARN threshold

Table 6. REGISTERS MAP

Bit	Type	Reset	Name	RST Value	Function
STAT_INT REGISTER – Memory Location: 03					
4	RCDual	OFF STATE, POR, REG_RST	TM1	0	0: Silicon temperature is below T1 threshold 1: Silicon temperature is above T1 threshold
3	RCDual	OFF STATE, POR, REG_RST	TM2	0	0: Silicon temperature is below T2 threshold 1: Silicon temperature is above T2 threshold
2	RCDual	OFF STATE, POR, REG_RST	TSD	0	0: Silicon temperature is below TSD threshold 1: Silicon temperature is above TSD threshold
1	R	No_Reset	RESERVED	0	
0	RCDual	OFF STATE, REG_RST, POR, OTGMODE	VBUSOK	0	0: changer not in USB range 1: charger in USB charging range VBUSUV < VIN < VBUSOV
CH1_INT REGISTER – Memory Location: 04					
7–5	R	No_Reset	RESERVED	0	
4	RCDual	OFF STATE, REG_RST, POR, OTGMODE	VINLO	0	VIN changer detection interrupt: 1: VIN – VBAT > VCHGDET and VIN < VINDET
3	RCDual	OFF STATE, REG_RST, POR, OTGMODE	VINHI	0	VIN over voltage lock out interrupt: 1: VIN > VINOV
2	RCDual	OFF STATE, REG_RST, POR, OTGMODE	BATRMV	0	battery temp out of range interrupt: 1: VNTC > VNTCRMV
1	RCDual	OFF STATE, REG_RST, POR, OTGMODE	BUCKOVP	0	VBAT over voltage interrupt: 1: VBAT > VOVP
0	R	No_Reset	CHINT2	0	charger related interrupt (CH2_INT register)
CH2_INT REGISTER – Memory Location: 05					
7	RCDual	OFF STATE, REG_RST, POR, OTGMODE	NTCHOT	0	Battery Temperature exceeds NTC HOT threshold
5–6	R	No_Reset	RESERVED	00	
4	RCDual	OFF STATE, REG_RST, POR, OTGMODE	NTCCOLD	0	Battery Temperature is lower than NTC COLD threshold
3	RCSingle	OFF STATE, POR, REG_RST, TRM_RST, OTGMODE	WDTO	0	watchdog timeout expires interrupt: 1: 32s timer expired.
2	RCSingle	OFF STATE, POR, REG_RST, TRM_RST, OTGMODE	USBTO	0	usb timeout expires initerrupt: 1: 2048s timer expired
1	RCSingle	OFF STATE, POR, REG_RST, TRM_RST, OTGMODE	CHGTO	0	charge timeout expires interrupt: 1: 3600s timer expired
0	R	No_Reset	CHINT1	0	charger related interrupt (CH1_INT register)
BST_INT REGISTER – Memory Location: 06					
7–3	R	No_Reset	RESERVED	00000	
2	RCDual	OFF STATE, POR, REG_RST, CHGMODE	VBUSILIM	0	vbus overload interrupt: 1: Vbus voltage < VBUSUV

Table 6. REGISTERS MAP

Bit	Type	Reset	Name	RST Value	Function
BST_INT REGISTER – Memory Location: 06					
1	RCDual	OFF STATE, POR, REG_RST, CHGMODE	VBUSOV	0	vbus overvoltage interrupt: 1: Vbus voltage < VBUSOV
0	RCDual	OFF STATE, POR, REG_RST, CHGMODE	VBATLO	0	vbat overvoltage interrupt: 1: Vbat voltage < VIBSTL
VIN_SNS REGISTER – Memory Location: 07					
7	R	No_Reset	VINOVLO_SNS	0	VIN over voltage lock out comparator 1: VIN > VINOV
6	R	No_Reset	RESERVED	0	
5	R	No_Reset	VBUSOV_SNS	0	VIN not is USB range comparator 1: VIN > VBUSOV
4	R	No_Reset	VBUSUV_SNS	0	VIN not is USB range comparator 1: VIN < VBUSUV
3	R	No_Reset	VINDET_SNS	0	VIN voltage detection comparator 1: VIN > VINDET
2	R	No_Reset	VCHGDET_SNS	0	VIN changer detection comparator 1: VIN – VBAT > VCHGDET
1	R	No_Reset	VBOOST_UV_SNS	0	VIN OTG under voltage comparator 1: VIN < VBUSUV
0	R	No_Reset	RESERVED	0	
VBAT_SNS REGISTER – Memory Location: 08					
7	R	No_Reset	NTC_REMOVAL_SNS	0	NTC removal comparator : 1: Battery removal, VNTC > VNTCRMV
6	R	No_Reset	VBAT_OV_SNS	0	VBAT over voltage comparator 1: VBAT > VOVP
5	R	No_Reset	VRECHG_OK_SNS	0	VBAT recharge comparator 1: VBAT > VRECHG
4	R	No_Reset	VFET_OK_SNS	0	VBAT weak charge comparator 1: VBAT > VFET
3	R	No_Reset	VPRE_OK_SNS	0	VBAT precharge comparator 1: VBAT > VPRE
2	R	No_Reset	VSAFE_OK_SNS	0	VBAT safe comparator 1: VBAT > VSAFE
1	R	No_Reset	IEOC_OK_SNS	0	End of charge current comparator 1: ICHARGE > IEOC
0	R	No_Reset	RESERVED	0	
TEMP_SNS REGISTER – Memory Location: 09					
7	R	No_Reset	NTC_COLD_SNS	0	NTC cold comparator : 1: VNTC < VCOLD
5–6	R	No_Reset	RESERVED	00	
4	R	No_Reset	NTC_HOT_SNS	0	NTC disable comparator : 1: VNTC > VNTCDIS
3	R	No_Reset	TSD_SNS	0	Chip thermal shut down comparator 1: Chip Temp > TSD
2	R	No_Reset	TM2_SNS	0	Chip thermal shut down comparator 1: Chip Temp > tm2

Table 6. REGISTERS MAP

Bit	Type	Reset	Name	RST Value	Function
TEMP_SNS REGISTER – Memory Location: 09					
1	R	No_Reset	TM1_SNS	0	Chip thermal shut down comparator 1: Chip Temp > tm1
0	R	No_Reset	TWARN	0	Chip thermal shut down comparator 1: Chip Temp > twarn
STAT_MSK REGISTER – Memory Location: 0A					
7–6	R	No_Reset	RESERVED	00	
5	RW	OFF STATE, POR, REG_RST	TWARN_MASK	1	TWARN interruption mask bit.
4	RW	OFF STATE, POR, REG_RST	TM1_MASK	1	TM1 interruption mask bit.
3	RW	OFF STATE, POR, REG_RST	TM2_MASK	1	TM2 interruption mask bit.
2	RW	OFF STATE, POR, REG_RST	TSD_MASK	1	TSD interruption mask bit.
1	R	No_Reset	RESERVED	0	
0	RW	OFF STATE, POR, REG_RST, OTGMODE	VBUSOK_MASK	1	VBUSOK interruption mask bit.
CH1_MSK REGISTER – Memory Location: 0B					
7–5	R	No_Reset	RESERVED	000	
4	RW	OFF STATE, POR, REG_RST, OTGMODE	VINLO_MASK	1	VINLO interruption mask bit.
3	RW	OFF STATE, POR, REG_RST, OTGMODE	VINHI_MASK	1	VINHI interruption mask bit.
2	RW	OFF STATE, POR, REG_RST, OTGMODE	BATRMV_MASK	1	BATRMV interruption mask bit.
1	RW	OFF STATE, POR, REG_RST, OTGMODE	BUCKOVP_MASK	1	BUCKOVP interruption mask bit.
0	R	No_Reset	RESERVED	0	
CH2_MSK REGISTER – Memory Location: 0C					
7	RW	OFF STATE, POR, REG_RST, OTGMODE	NTCHOT_MASK	1	NTCHOT interruption mask bit.
5–6	R	No_Reset	RESERVED	0	
4	RW	OFF STATE, POR, REG_RST, OTGMODE	NTCCOLD_MASK	1	NTCCOLD interruption mask bit.
3	RW	OFF STATE, POR, REG_RST, OTGMODE	WDTO_MASK	0	WDTO interruption mask bit.
2	RW	OFF STATE, POR, REG_RST, OTGMODE	USBTO_MASK	0	USBTO interruption mask bit.
1	RW	OFF STATE, POR, REG_RST, OTGMODE	CHGTO_MASK	0	CHGTO interruption mask bit.

Table 6. REGISTERS MAP

Bit	Type	Reset	Name	RST Value	Function
CH2_MSK REGISTER – Memory Location: 0C					
0	R	No_Reset	RESERVED	0	
BST_MSK REGISTER – Memory Location: 0D					
7–4	R	No_Reset	RESERVED	0000	
3	RW	OFF STATE, POR, REG_RST, OTGMODE	VBUSILIM_MASK	1	VBUSILIM interruption mask bit.
2	RW	OFF STATE, POR, REG_RST, OTGMODE	VBUSOV_MASK	1	VBUSOV interruption mask bit.
1	RW	OFF STATE, POR, REG_RST, OTGMODE	VBATLO_MASK	1	VBATLO interruption mask bit.
0	RW	OFF STATE, POR, REG_RST, OTGMODE	STATEOTG_MASK	1	STATEOTG interruption mask bit.
VBAT_SET REGISTER – Memory Location: 0E					
7–6	R	No_Reset	RESERVED	00	
0–5	RW	OFF STATE, POR, REG_RST, OTGMODE	CTRL_VBAT [5:0]	001100	000000: 3.3 V 001100: 3.6 V 110000: 4.5 V Step: 0.025 V
IBAT_SET REGISTER – Memory Location: 0F					
7	R	No_Reset	RESERVED	0	
6–4	RW	OFF STATE, POR, REG_RST, OTGMODE	IEOC[2:0]	010	000: 100 mA 010: 150 mA 111: 275 mA Step: 25 mA
3–0	RW	OFF STATE, POR, REG_RST, OTGMODE	ICHG[3:0]	0110	Output range current programmable range: 0000: 400 mA 1011: 1.5 A Step : 100 mA
MISC_SET REGISTER – Memory Location: 10					
7	RW	OFF STATE, POR, REG_RST, OTGMODE	TST_SET	0	Minimum transition time from Weak Charge to Full Charge State 0 : 32 s 1 : 16 ms
6	RW	OFF STATE, POR, REG_RST, OTGMODE	FCTRY_MOD_REG	0	Factory mode : 0: Factory mode disable 1: Enable factory mode.
5	RW	OFF STATE, POR, REG_RST, OTGMODE	IWEAK_EN	1	Charge current during weak battery states: 0: Disable 1: 100 mA
4–2	RW	OFF STATE, POR, REG_RST, OTGMODE	CTRL_VFET[2:0]	011	Battery to system re–connection threshold: 000: 3.1 V 001: 3.2 V 010: 3.3 V 011: 3.4 V 100: 3.5 V 101: 3.6 V
1–0	RW	OFF STATE, POR, REG_RST, OTGMODE	IINLIM[1:0]	00	Input current limit range: 00: 100 mA 01: 500 mA 10: 900 mA 11: 1500 mA

Table 6. REGISTERS MAP

Bit	Type	Reset	Name	RST Value	Function	
NTC_SET REGISTER – Memory Location: 11						
7–4	R	No_Reset	RESERVED	0000		
2–3	RW	OFF STATE, POR, REG_RST, OTGMODE	BATCOLD[1:0]	01	R0 = 10 kΩ, T0= 25°C	
					B = 3380 00: –1°C 01: 2°C 10: 5°C 11: 9°C	B = 3400 00: 1°C 01: 5°C 10: 8°C 11: 11°C
0–1	RW	OFF STATE, POR, REG_RST, OTGMODE	BATHOT[1:0]	10	R0 = 10 kΩ,T0= 25°C	
					B = 3380 |00: 43°C 01: 47°C 10: 52°C 11: 57°C	B = 3400 00: 40°C 01: 44°C 10: 48°C 11: 52°C

APPLICATION INFORMATION

Components Selection

Inductor L1

NCP1851 is recommended to be used with 2.2 μH inductor. Below will give inductor ripple and maximum current for two different application cases knowing the following relation:

$$\Delta I_L = V_{BAT} \times \left(1 - \frac{V_{BAT}}{V_{IN}}\right) \times \frac{1}{L1 \times F_{SWCHG}}$$

The worst case is when $V_{BAT} - \frac{V_{BAT}^2}{V_{IN}}$ is maximum

so when $V_{BAT} = \frac{V_{IN}}{2}$

$$\Delta I_{LMAX} = \frac{V_{IN}}{4} \cdot \frac{1}{L1 \cdot F_{SWCHG}}; I_{PEAKMAX} = I_{CHG} + \frac{\Delta I_{LMAX}}{2}$$

Capacitor C6

A 10 μF output capacitor is recommended for proper operation and design stability. The bandwidth of the system is defined by the following relation:

$$F_{BW} = \frac{1}{2\pi \times \sqrt{L_1 \times C_6}} = 33\ \text{kHz}$$

The bandwidth is recommended to be high enough in case of application with a BATFET because the system can be directly connected to the buck output. And in this case, the battery does not play any role upon a load transient as it's disconnected from the buck converter.

USB dedicated charge

V_{IN} = 5 V
V_{CHG} = 4.2 V
I_{CHG} = 1.5 A
L1 = 2.2 μH
Δ_{IL1} = 0.189 A
$I_{PEAKMAX}$ = 1.59 A

AC adaptor charge

V_{IN} = 16 V
V_{CHG} = 4.2 V
I_{CHG} = 1.5 A
L1 = 2.2 μH
Δ_{IL1} = 0.6 A
$I_{PEAKMAX}$ = 1.8 A

Resistance R1

R_1 (charge current sense resistor) resistor is determined by considering thermal constrain as its value is 68 mΩ typical. The power dissipation is given by:

$$P_{R1} = R_1 \times (I_{CHG})^2$$

The worst case is I_{CHG} = 1.5 A so P_{R1} = 0.153 W.

BILL OF MATERIAL

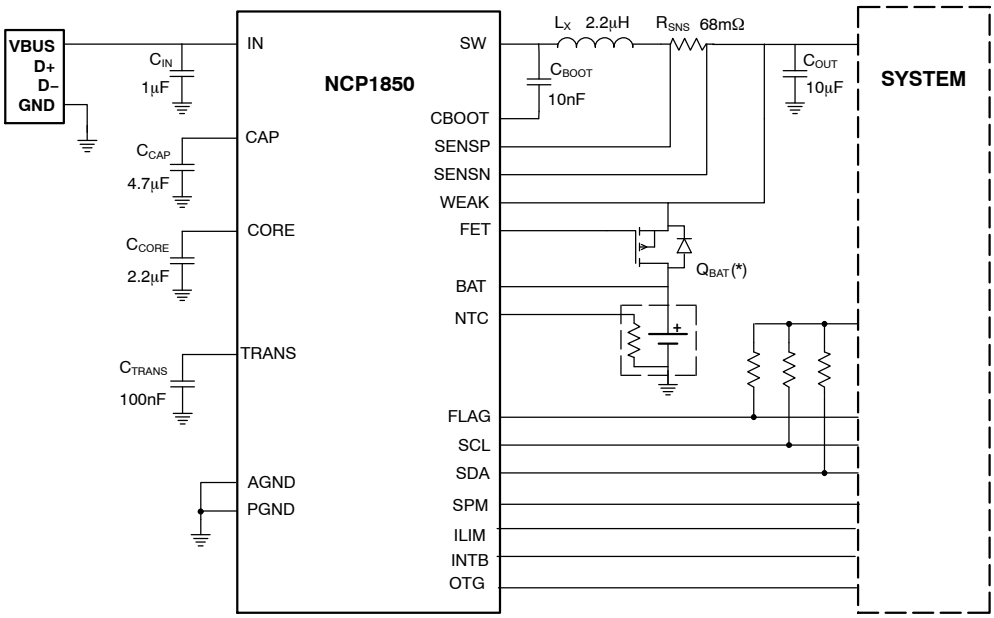


Figure 14. NCP1850 Typical Application Example

Item	Part Description	Ref	Value	PCB Footprint	Manufacturer	Manufacturer Reference
1	Ceramic Capacitor 25 V X5R	C_{IN}	1 μF	0603	MURATA	GRM188R61E105K
2	Ceramic Capacitor 25 V X5R	C_{CAP}	4.7 μF	0805	MURATA	GRM21BR61E475KA12L
3	Ceramic Capacitor 6.3 V X5R	C_{CORE}	2.2 μF	0402	MURATA	GRM155R60J225M
4	Ceramic Capacitor 6.3 V X5R	C_{TRS}	0.1 μF	0402	MURATA	GRM155R60J104K
5	Ceramic Capacitor 10 V X5R	C_{BOOT}	10 nF	0402	MURATA	GRM155R60J103K
6	Ceramic Capacitor 6.3 V X5R	C_{OUT}	10 μF	0603	MURATA	GRM188R60J106M
7	SMD Inductor	L_X	2.2μH	3012	TDK	VLS3012T−2R2M1R5
8	SMD Resistor 0.25 W, 1%	R_{SNS}	68 mΩ	0603	PANASONIC	ERJ3BWFR068V
9	Power channel P−MOSFET	Q_{BAT}	30 mΩ	UDFN 2 * 2 mm	ON Semiconductor	NTLUS3A40PZ

PCB Layout Consideration

Particular attention must be paid with C_{CORE} capacitor as it's decoupling the supply of internal circuitry including gate driver. This capacitor must be placed between CORE pin and PGND pin with a minimum track length.

The high speed operation of the NCP1850 demands careful attention to board layout and component placement. To prevent electromagnetic interference (EMI) problems, attention should be paid specially with components C_{IN}, L_X, C_{CAP}, and C_{OUT} as they constitute a high frequency current loop area. The power input capacitor C_{IN}, connected from IN to PGND, should be placed as close as possible to the NCP1850. The output inductor L_X and the output capacitor C_{OUT} connected between R_{SNS} and PGND should be placed close to the IC. C_{CAP} capacitor should also be place as close as possible to CAP and PGND pin.

The high current charge path through IN, CAP, SW, inductor L1, Resistor R1, optional BAFTET, and battery pack must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces. An IWEAK current can flow through WEAK and BAT traces witch defines the appropriate track width.

It's suggested to keep as complete ground plane under NCP1850 as possible. PGND and AGND pin connection must be connected to the ground plane.

Care should be taken to avoid noise interference between PGND and AGND. Finally it is always good practice to keep the sensitive tracks such as feedbacks connections (SENSP, SENSN, BAT) away from switching signal connections by laying the tracks on the other side or inner layer of PCB.

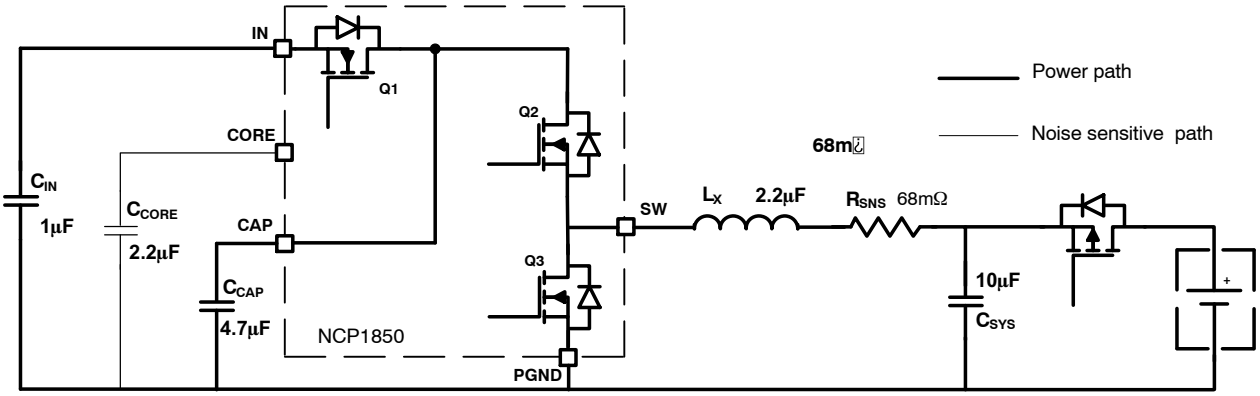


Figure 15. NCP1850 Power Path

ORDERING INFORMATION

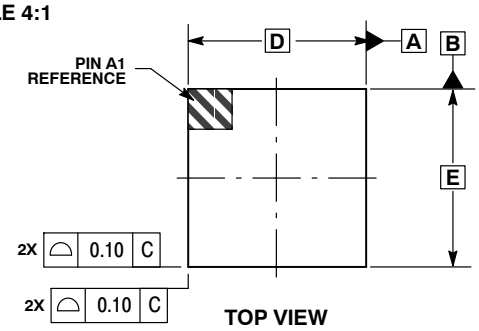
Part Number	I²C Address	Package	Shipping†
NCP1850FCCT1G	$6C	WLCSP25 (Pb−Free)	TBD

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

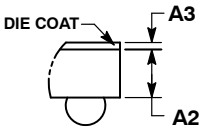
WLCSP25, 2.06x2.06
CASE 567FZ
ISSUE O

DATE 17 JUL 2012

SCALE 4:1



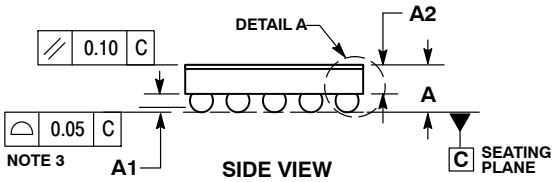
TOP VIEW



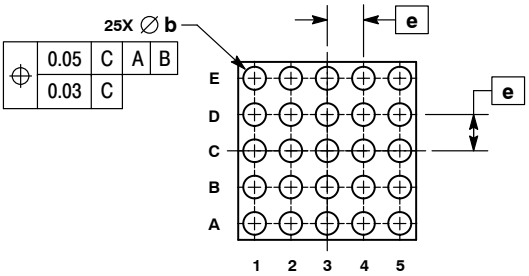
DETAIL A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.60
A1	0.17	0.23
A2	0.36 REF	
A3	0.04 REF	
b	0.24	0.29
D	2.06 BSC	
E	2.06 BSC	
e	0.40 BSC	

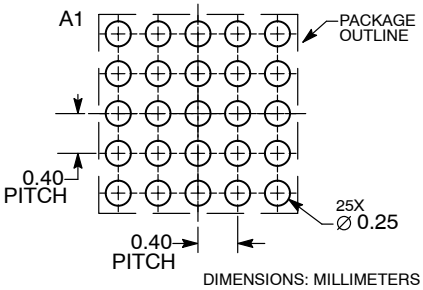


SIDE VIEW



BOTTOM VIEW

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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