NCV7340

CAN Transceiver, High Speed, Low Power

ON Semiconductor®

http://onsemi.com

Description

The NCV7340 CAN transceiver is the interface between a controller area network (CAN) protocol controller and the physical bus and may be used in both 12 V and 24 V systems. The transceiver provides differential transmit capability to the bus and differential receive capability to the CAN controller.

The NCV7340 is a new addition to the CAN high−speed transceiver family and is an improved drop−in replacement for the AMIS−42665.

Due to the wide common−mode voltage range of the receiver inputs, the NCV7340 is able to reach outstanding levels of electromagnetic susceptibility (EMS). Similarly, extremely low electromagnetic emission (EME) is achieved by the excellent matching of the output signals.

Features

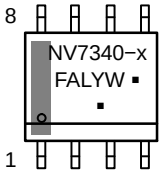
- Compatible with the ISO 11898 Standard (ISO 11898−2, ISO 11898−5 and SAE J2284)
- Low Quiescent Current
- High Speed (up to 1 Mbps)
- Ideally Suited for 12 V and 24 V Industrial and Automotive Applications
- Extremely Low Current Standby Mode with Wakeup via the Bus
- Low EME Common−Mode Choke is No Longer Required
- Voltage Source via V_{SPLIT} Pin for Stabilizing the Recessive Bus Level (Further EMC Improvement)
- No Disturbance of the Bus Lines with an Un−powered Node
- Transmit Data (TxD) Dominant Time−out Function
- Thermal Protection
- Bus Pins Protected Against Transients in an Automotive Environment
- Bus and V_{SPLIT} Pins Short−Circuit Proof to Supply Voltage and Ground
- Logic Level Inputs Compatible with 3.3 V Devices
- Up to 110 Nodes can be Connected to the Same Bus in Function of Topology
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices

Typical Applications

- Automotive
- Industrial Networks

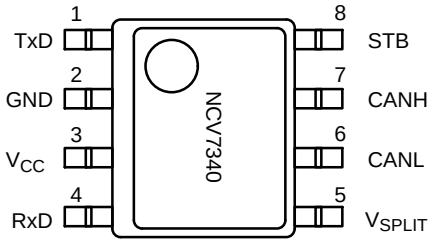
MARKING DIAGRAM

SOIC−8
CASE 751AZ



NV7340−		= Specific Device Code
	x	= 3 (NCV7340D13R2G)
		= 2 (NCV7340D12R2G)
		= 4 (NCV7340D14R2G)
F		= Fab Location Code*
		*For NCV7340D14R2G only
A		= Assembly Location
L		= Wafer Lot
Y		= Year
W		= Work Week
▪		= Pb−Free Package

PIN ASSIGNMENT



NCV7340DxxR2G
(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

Table 1. KEY TECHNICAL CHARACTERISTICS AND OPERATING RANGES

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Power supply voltage		4.75	5.25	V
V_{STB}	DC voltage at pin STB		0	V_{CC}	V
V_{TxD}	DC voltage at pin TxD		0	V_{CC}	V
V_{RxD}	DC voltage at pin RxD		0	V_{CC}	V
V_{CANH}	DC voltage at pin CANH	$0 < V_{CC} < 5.25$ V; no time limit	−50	+50	V
V_{CANL}	DC voltage at pin CANL	$0 < V_{CC} < 5.25$ V; no time limit	−50	+50	V
V_{SPLIT}	DC voltage at pin V_{SPLIT}	$0 < V_{CC} < 5.25$ V; no time limit	−40	+40	V
$V_{O(dif)(bus\_dom)}$	Differential bus output voltage in dominant state	$42.5\ \Omega < R_{LT} < 60\ \Omega$	1.5	3	V
CM−range	Input common−mode range for comparator	Guaranteed differential receiver threshold and leakage current	−35	+35	V
C_{load}	Load capacitance on IC outputs			15	pF
$t_{pd(rec-dom)}$	Propagation delay TxD to RxD	See Figure 7	60	230	ns
$t_{pd(dom-rec)}$	Propagation delay TxD to RxD	See Figure 7	60	245	ns
T_J	Junction temperature		−40	150	°C

BLOCK DIAGRAM

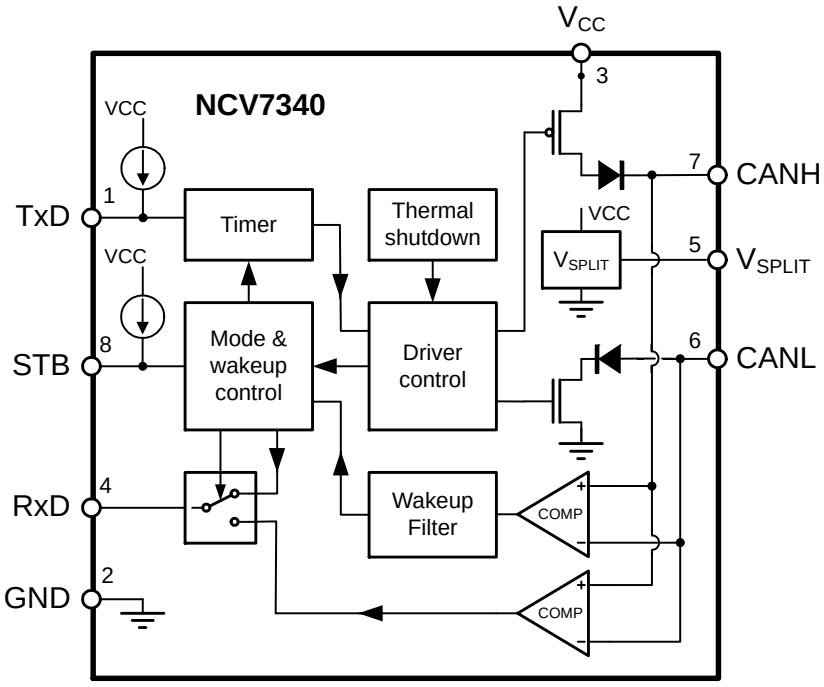


Figure 1. Block Diagram

TYPICAL APPLICATION

Application Schematics

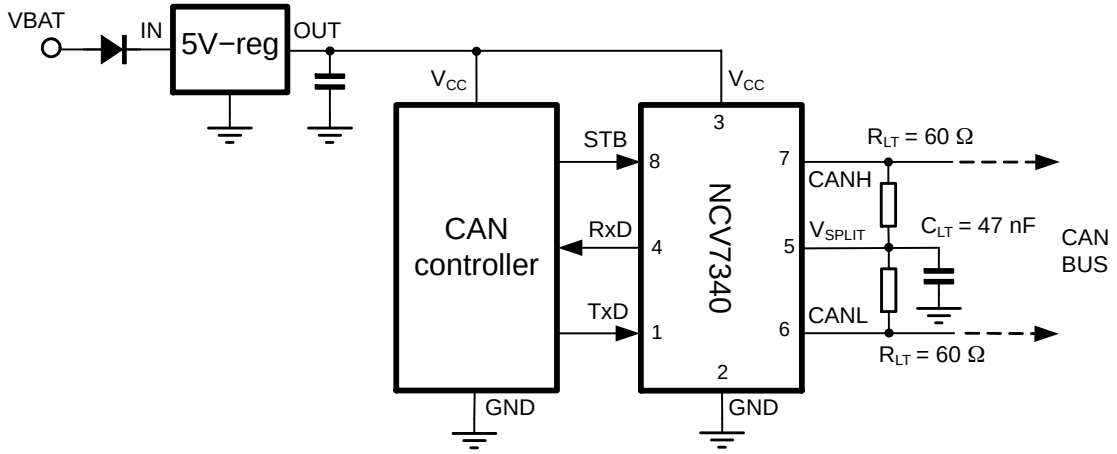


Figure 2. Application Diagram

Pin Description

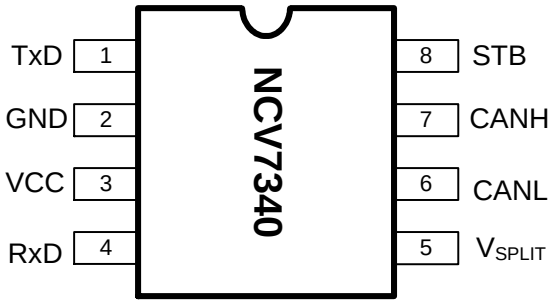


Figure 3. NCV7340 Pin Assignment

Table 2. PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	TxD	Transmit data input; low input → dominant driver; internal pullup current
2	GND	Ground
3	VCC	Supply voltage
4	RxD	Receive data output; dominant transmitter → low output
5	V_{SPLIT}	Common−mode stabilization output
6	CANL	Low−level CAN bus line (low in dominant mode)
7	CANH	High−level CAN bus line (high in dominant mode)
8	STB	Standby mode control input

FUNCTIONAL DESCRIPTION

Operating Modes

NCV7340 provides two modes of operation as illustrated in Table 3. These modes are selectable through pin STB.

Table 3. OPERATING MODES

Pin STB	Mode	Pin RXD	
		Low	High
Low	Normal	Bus dominant	Bus recessive
High	Standby	Wakeup request detected	No wakeup request detected

Normal Mode

In the normal mode, the transceiver is able to communicate via the bus lines. The signals are transmitted and received to the CAN controller via the pins TxD and RxD. The slopes on the bus lines outputs are optimized to give extremely low EME.

Standby Mode

In standby mode both the transmitter and receiver are disabled and a very low−power differential receiver monitors the bus lines for CAN bus activity. The bus lines are terminated to ground and supply current is reduced to a minimum, typically 10 μA. When a wake−up request is detected by the low−power differential receiver, the signal is first filtered and then verified as a valid wake signal after a time period of $t_{dwakerd}$, the RxD pin is driven low by the transceiver to inform the controller of the wake−up request.

Split Circuit

The V_{SPLIT} pin is operational only in normal mode. In standby mode this pin is floating. The V_{SPLIT} can be connected as shown in Figure 2 or, if it's not used, can be left floating. Its purpose is to provide a stabilized DC voltage of 0.5 x V_{CC} to the bus avoiding possible steps in the common−mode signal therefore reducing EME. These unwanted steps could be caused by an un−powered node on the network with excessive leakage current from the bus that shifts the recessive voltage from its nominal 0.5 x V_{CC} voltage.

Wakeup

When a valid wakeup (dominant state longer than t_{Wake}) is received during the standby mode the RxD pin is driven low. The wakeup detection is not latched: RxD returns to High state after t_{wakedr} when the bus signal is released back to recessive – see Figure 4. Wake−up behavior in case of a permanent dominant − due to, for example, a bus short − represents the only difference between the circuit functional sub−versions listed in the Ordering Information table. When the standby mode is entered while a dominant is present on the bus, the "unconditioned bus wake−up" versions will signal a bus−wakeup immediately after the state transition (signal RxD_1 in Figure 4). The other version will signal bus−wakeup only after the initial dominant is released (signal RxD_2 in Figure 4). In this way it's ensured, that a CAN bus can be put to a low−power mode even if the nodes have a level sensitivity to RxD pin and a permanent dominant is present on the bus.

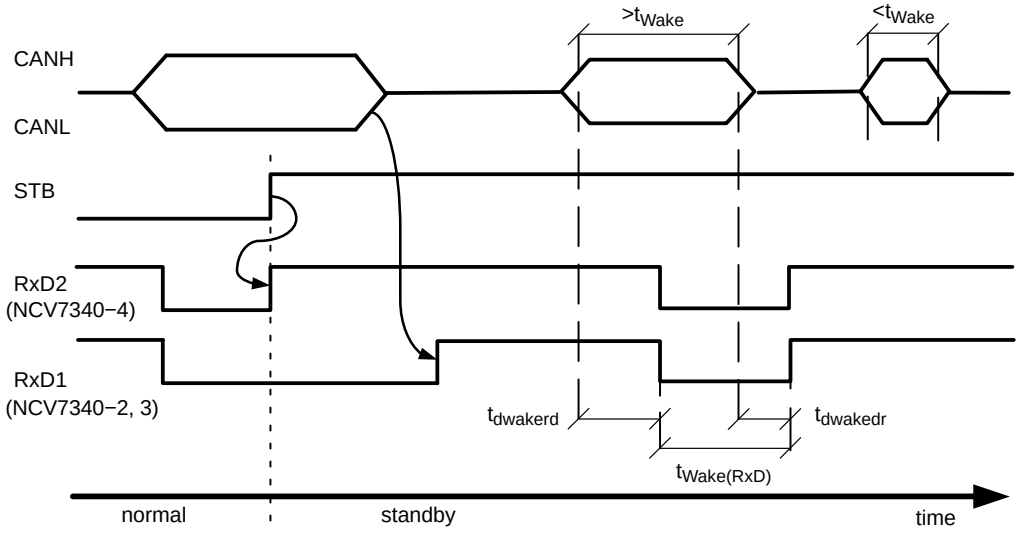


Figure 4. NCV7340 Wakeup Behavior

Overtemperature Detection

A thermal protection circuit protects the IC from damage by switching off the transmitter if the junction temperature exceeds a value of approximately 160°C. Because the transmitter dissipates most of the power, the power dissipation and temperature of the IC is reduced. All other IC functions continue to operate. The transmitter off−state resets when the temperature decreases below the shutdown threshold and pin TxD goes high. The thermal protection circuit is particularly needed when a bus line short circuits.

TxD Dominant Time−out Function

A TxD dominant time−out timer circuit prevents the bus lines being driven to a permanent dominant state (blocking all network communication) if pin TxD is forced permanently low by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TxD. If the duration of the low−level on pin TxD exceeds the internal timer value $t_{dom(TxD)}$, the transmitter is disabled, driving the bus into a recessive state. The timer is reset by a positive edge on pin TxD.

This TxD dominant time−out time ($t_{dom(TxD)}$) defines the minimum possible bit rate to 40 kbps.

Fail Safe Features

A current−limiting circuit protects the transmitter output stage from damage caused by accidental short circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

The pins CANH and CANL are protected from automotive electrical transients (according to ISO 7637; see Figure 5). Pins TxD and STB are pulled high internally should the input become disconnected. Pins TxD, STB and RxD will be floating, preventing reverse supply should the V_{CC} supply be removed.

ELECTRICAL CHARACTERISTICS

Definitions

All voltages are referenced to GND (Pin 2). Positive currents flow into the IC. Sinking current means the current is flowing into the pin; sourcing current means the current is flowing out of the pin.

Table 4. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		−0.3	+6	V
V_{CANH}	DC voltage at pin CANH	$0 < V_{CC} < 5.25$ V; no time limit	−50	+50	V
V_{CANL}	DC voltage at pin CANL	$0 < V_{CC} < 5.25$ V; no time limit	−50	+50	V
V_{SPLIT}	DC voltage at pin V_{SPLIT}	$0 < V_{CC} < 5.25$ V; no time limit	−40	+40	V
V_{TxD}	DC voltage at pin TxD		−0.3	6	V
V_{RxD}	DC voltage at pin RxD		−0.3	6	V
V_{STB}	DC voltage at pin STB		−0.3	6	V
V_{esd}	Electrostatic discharge voltage at all pins	Note 1 Note 2	−6 −500	6 500	kV V
	Electrostatic discharge voltage at CANH and CANL pins	Note 3	−12	12	kV
V_{schaff}	Transient voltage, see Figure 5	Note 5	−150	100	V
Latchup	Static latchup at all pins	Note 4		120	mA
T_{stg}	Storage temperature		−55	+150	°C
T_A	Ambient temperature		−40	+125	°C
T_J	Maximum junction temperature		−40	+170	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Standardized human body model electrostatic discharge (ESD) pulses in accordance to EIA−JESD22. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
2. Standardized charged device model ESD pulses when tested according to ESD−STM5.3.1−1999.
3. System human body model electrostatic discharge (ESD) pulses. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor.
4. Static latchup immunity: Static latchup protection level when tested according to EIA/JESD78.
5. Pulses 1, 2a, 3a and 3b according to ISO 7637 part 3. Verification by external test house.

Table 5. THERMAL CHARACTERISTICS

Symbol	Parameter	Conditions	Value	Unit
$R_{\theta JA\_1}$	Thermal Resistance Junction−to−Air, 1S0P PCB (Note 6)	Free air	125	K/W
$R_{\theta JA\_2}$	Thermal Resistance Junction−to−Air, 2S2P PCB (Note 7)	Free air	75	K/W

6. Test board according to EIA/JEDEC Standard JESD51−3, signal layer with 10% trace coverage.
7. Test board according to EIA/JEDEC Standard JESD51−7, signal layers with 10% trace coverage.

Table 6. CHARACTERISTICS V_{CC} = 4.75 V to 5.25 V; T_J = −40 to +150°C; R_{LT} = 60 Ω unless specified otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY (Pin V_{CC})						
I_{CC}	Supply current in normal mode	Dominant; V_{TxD} = 0 V Recessive; V_{TxD} = V_{CC}		57 7.5	75 10	mA
I_{CCS}	Supply current in standby mode	$T_{J,max}$ = 100°C		10	15	μA
TRANSMITTER DATA INPUT (Pin TxD)						
V_{IH}	High−level input voltage	Output recessive	2.0	−	V_{CC}	V
V_{IL}	Low−level input voltage	Output dominant	−0.3	−	+0.8	V
I_{IH}	High−level input current	V_{TxD} = V_{CC}	−5	0	+5	μA
I_{IL}	Low−level input current	V_{TxD} = 0 V	−350	−200	−75	μA
C_i	Input capacitance	Not tested	−	5.0	10	pF
TRANSMITTER MODE SELECT (Pin STB)						
V_{IH}	High−level input voltage	Standby mode	2.0	−	V_{CC}	V
V_{IL}	Low−level input voltage	Normal mode	−0.3	−	+0.8	V
I_{IH}	High−level input current	V_{STB} = V_{CC}	−5	0	+5	μA
I_{IL}	Low−level input current	V_{STB} = 0 V	−10	−4	−1	μA
C_i	Input capacitance	Not tested	−	5.0	10	pF
RECEIVER DATA OUTPUT (Pin RxD)						
I_{oh}	High−level output current	normal mode V_{RxD} = V_{CC} – 0.4 V	−1	−0.4	−0.1	mA
I_{ol}	Low−level output current	V_{RxD} = 0.4 V	2	6	12	mA
V_{oh}	High−level output voltage	standby mode I_{RxD} = −100 μA	V_{CC} – 1.1	V_{CC} – 0.7	V_{CC} – 0.4	V
BUS LINES (Pins CANH and CANL)						
$V_{o(reces)\ (norm)}$	Recessive bus voltage on pins CANH and CANL	V_{TxD} = V_{CC}; no load normal mode	2.0	2.5	3.0	V
$V_{o(reces)\ (stby)}$	Recessive bus voltage on pins CANH and CANL	V_{TxD} = V_{CC}; no load standby mode	−100	0	100	mV
$I_{o(reces)\ (CANH)}$	Recessive output current at pin CANH	−35 V < V_{CANH} < +35 V; 0 V < V_{CC} < 5.25 V	−2.5	−	+2.5	mA
$I_{o(reces)\ (CANL)}$	Recessive output current at pin CANL	−35 V < V_{CANL} < +35 V; 0 V < V_{CC} < 5.25 V	−2.5	−	+2.5	mA
$I_{LI(CANH)}$	Input leakage current to pin CANH	V_{CC} = 0 V V_{CANL} = V_{CANH} = 5 V	−10	0	10	μA
$I_{LI(CANL)}$	Input leakage current to pin CANL	V_{CC} = 0 V V_{CANL} = V_{CANH} = 5 V	−10	0	10	μA
$V_{o(dom)\ (CANH)}$	Dominant output voltage at pin CANH	V_{TxD} = 0 V	3.0	3.6	4.25	V
$V_{o(dom)\ (CANL)}$	Dominant output voltage at pin CANL	V_{TxD} = 0 V	0. 5	1.4	1.75	V
$V_{o(dif)\ (bus\_dom)}$	Differential bus output voltage (V_{CANH} − V_{CANL})	V_{TxD} = 0 V; dominant; 42.5 Ω < R_{LT} < 60 Ω	1.5	2.25	3.0	V
$V_{o(dif)\ (bus\_rec)}$	Differential bus output voltage (V_{CANH} − V_{CANL})	V_{TxD} = V_{CC}; recessive; no load	−120	0	+50	mV
$I_{o(sc)\ (CANH)}$	Short circuit output current at pin CANH for the NCV7340D13(R2)G	V_{CANH} = 0 V; V_{TxD} = 0 V	−100	−70	−45	mA
	Short circuit output current at pin CANH for NCV7340D12(R2)G & NCV7340D14(R2)G	V_{CANH} = 0 V; V_{TxD} = 0 V	−120	−70	−45	mA

Table 6. CHARACTERISTICS V_{CC} = 4.75 V to 5.25 V; T_J = −40 to +150°C; R_{LT} = 60 Ω unless specified otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BUS LINES (Pins CANH and CANL)						
$I_{o(sc)\ (CANL)}$	Short circuit output current at pin CANL for the NCV7340D13(R2)G	V_{CANL} = 36 V; V_{TxD} = 0 V	45	70	100	mA
	Short circuit output current at pin CANL for NCV7340D12(R2)G & NCV7340D14(R2)G	V_{CANL} = 36 V; V_{TxD} = 0 V	45	70	120	mA
$V_{i(dif)\ (th)}$	Differential receiver threshold voltage (see Figure 6)	−5 V < V_{CANL} < +12 V; −5 V < V_{CANH} < +12 V;	0.5	0.7	0.9	V
$V_{ihcm(dif)\ (th)}$	Differential receiver threshold voltage for high common−mode (see Figure 6)	−35 V < V_{CANL} < +35 V; −35 V < V_{CANH} < +35 V;	0.40	0.7	1.0	V
$V_{i(dif)\ (th)\_STDBY}$	Differential receiver threshold voltage in standby mode (see Figure 6)	−12 V < V_{CANL} < +12 V; −12 V < V_{CANH} < +12 V;	0.4	0.8	1.15	V
$R_{i(cm)\ (CANH)}$	Common−mode input resistance at pin CANH		15	26	37	kΩ
$R_{i(cm)\ (CANL)}$	Common−mode input resistance at pin CANL		15	26	37	kΩ
$R_{i(cm)\ (m)}$	Matching between pin CANH and pin CANL common mode input resistance	V_{CANH} = V_{CANL}	−0.8	0	+0.8	%
$R_{i(dif)}$	Differential input resistance		25	50	75	kΩ
$C_{i(CANH)}$	Input capacitance at pin CANH	V_{TxD} = V_{CC}; not tested		7.5	20	pF
$C_{i(CANL)}$	Input capacitance at pin CANL	V_{TxD} = V_{CC}; not tested		7.5	20	pF
$C_{i(dif)}$	Differential input capacitance	V_{TxD} = V_{CC}; not tested		3.75	10	pF
COMMON−MODE STABILIZATION (Pin V_{SPLIT})						
V_{SPLIT}	Reference output voltage at pin V_{SPLIT}	Normal mode; −500 μA < I_{SPLIT} < 500 μA	0.3 x V_{CC}	−	0.7 x V_{CC}	
$I_{SPLIT(i)}$	V_{SPLIT} leakage current	Standby mode	−5		+5	μA
$I_{SPLIT(lim)}$	V_{SPLIT} limitation current	Normal mode	1.3		5.0	mA
THERMAL SHUTDOWN						
$T_{J(sd)}$	Shutdown junction temperature	junction temperature rising	150	160	185	°C
TIMING CHARACTERISTICS (see Figures 7 and 8)						
$t_{d(TxD−BUSon)}$	Delay TxD to bus active	C_l = 100 pF between CANH to CANL	20	85	135	ns
$t_{d(TxD−BUSoff)}$	Delay TxD to bus inactive	C_l = 100 pF between CANH to CANL	5.0	60	105	ns
$t_{d(BUSon−RXD)}$	Delay bus active to RxD	C_{rxd} = 15 pF	25	55	105	ns
$t_{d(BUSoff−RXD)}$	Delay bus inactive to RxD	C_{rxd} = 15 pF	30	100	105	ns
$t_{pd(rec−dom)}$	Propagation delay TxD to RxD from recessive to dominant	C_l = 100 pF between CANH to CANL	60		230	ns
$t_{d(dom−rec)}$	Propagation delay TxD to RxD from dominant to recessive	C_l = 100 pF between CANH to CANL	60		245	ns
$t_{d(stb−nm)}$	Delay standby mode to normal mode		5.0	7.5	10	μs
t_{Wake}	Dominant time for wake−up via bus	$V_{dif(dom)}$ > 1.4 V	0.75	2.5	5.0	μs
		$V_{dif(dom)}$ > 1.2 V	0.75	3	5.8	μs
$t_{dwakerd}$	Delay to flag wake event (recessive to dominant transitions) (See Figure 4)	Valid bus wake up event, C_{RxD} = 15 pF	1.0	3.4	10	μs
$t_{dwakedr}$	Delay to flag end of wake event (dominant to recessive transition) (See Figure 4)	Valid bus wake up event, C_{RxD} = 15 pF	0.5	2.9	6.0	μs
$t_{Wake(RxD)}$	Minimum pulse width on RxD (See Figure 4)	5 μs t_{wake}, C_{RxD} = 15 pF	0.5			μs
$t_{dom(TxD)}$	TxD dominant time for time out	V_{TxD} = 0 V	300	650	1000	μs

MEASUREMENT SETUPS AND DEFINITIONS

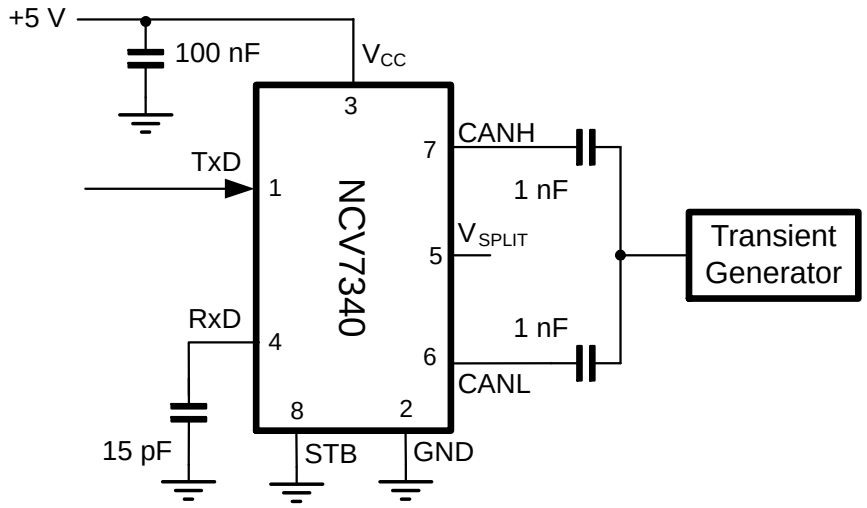


Figure 5. Test Circuit for Automotive Transients

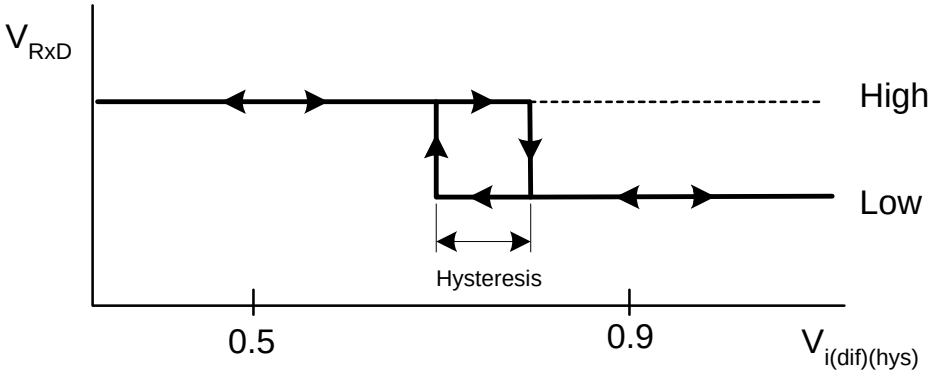


Figure 6. Hysteresis of the Receiver

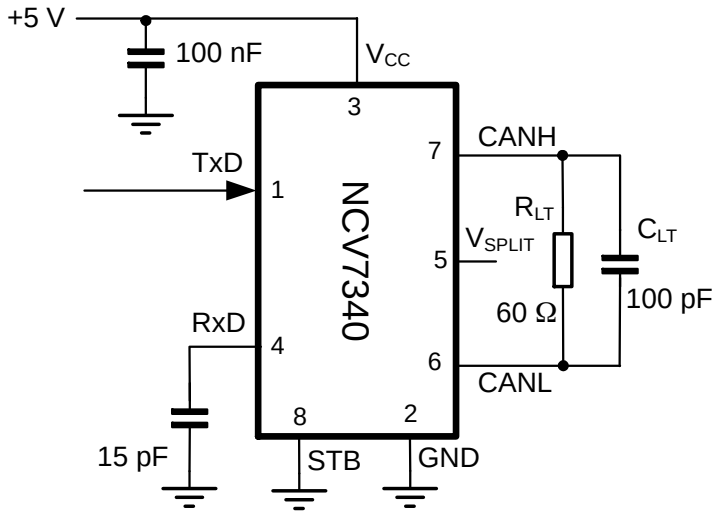


Figure 7. Test Circuit for Timing Characteristics

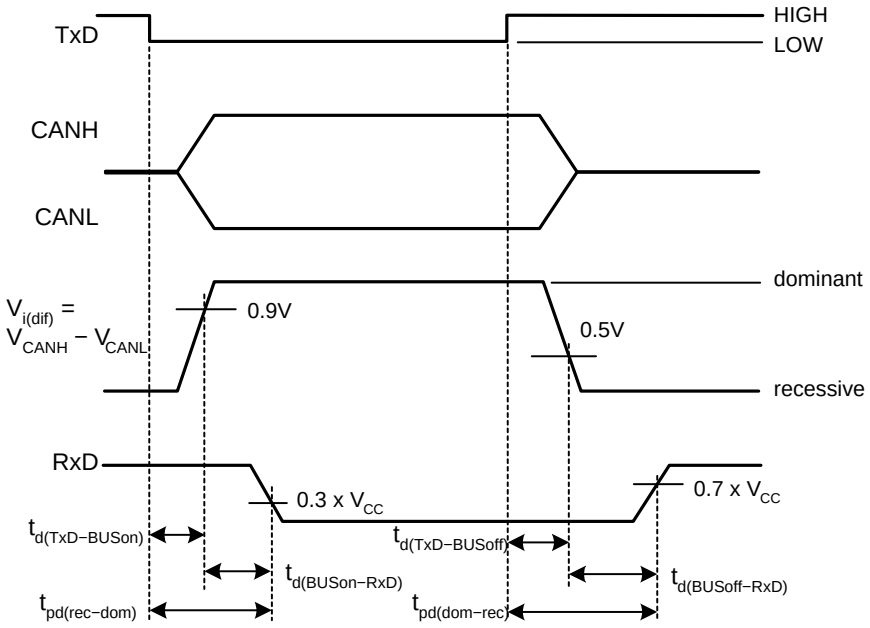


Figure 8. Timing Diagram for AC Characteristics

DEVICE ORDERING INFORMATION

Part Number	Description	Temperature Range	Package Type	Shipping†
NCV7340D12G	HS LP CAN Transceiver (Unconditioned Bus Wakeup)	−40°C to +125°C	SOIC 150 8 (Mate Sn, JEDEC MS−012) (Pb−Free)	96 Tube / Tray
NCV7340D12R2G				3000 / Tape & Reel
NCV7340D13G	EMC Improved HS LP CAN Transceiver (Unconditioned Bus Wakeup)			96 Tube / Tray
NCV7340D13R2G				3000 / Tape & Reel
NCV7340D14G	HS LP CAN Transceiver (Bus Wakeup Inactive in Case of Bus Fault)			96 Tube / Tray
NCV7340D14R2G				3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

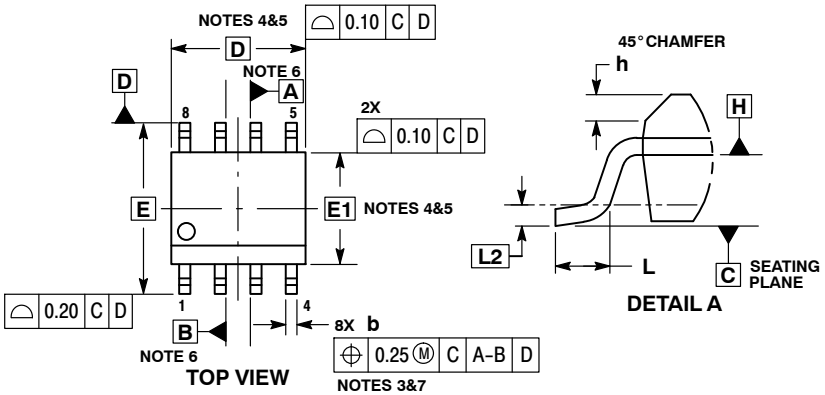
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

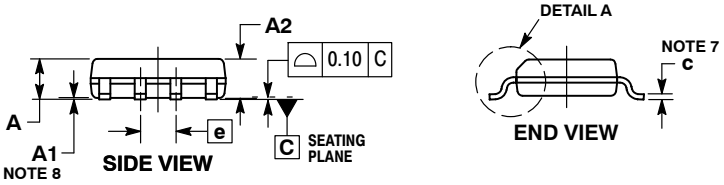
ON Semiconductor®

SCALE 1:1

SOIC−8
CASE 751AZ
ISSUE B

DATE 18 MAY 2015

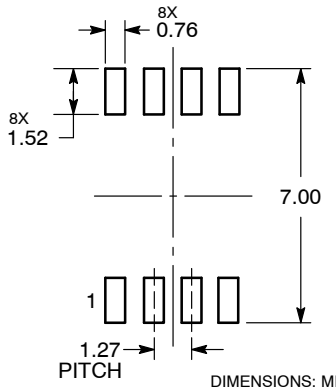




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006 mm PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.75
A1	0.10	0.25
A2	1.25	---
b	0.31	0.51
c	0.10	0.25
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
h	0.25	0.41
L	0.40	1.27
L2	0.25 BSC	

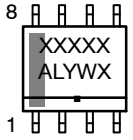
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

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