

NCV7341

High Speed Low Power CAN Transceiver

The NCV7341 CAN transceiver is the interface between a controller area network (CAN) protocol controller and the physical bus and may be used in both 12 V and 24 V systems. The transceiver provides differential transmit capability to the bus and differential receive capability to the CAN controller.

Due to the wide common-mode voltage range of the receiver inputs, the NCV7341 is able to reach outstanding levels of electromagnetic susceptibility (EMS). Similarly, extremely low electromagnetic emission (EME) is achieved by the excellent matching of the output signals.

The NCV7341 is a new addition to the ON Semiconductor CAN high-speed transceiver family and offers the following additional features:

Features

- Ideal Passive Behavior when Supply Voltage is Removed
- Separate V_{IO} Supply for Digital Interface Allowing Communication to CAN Controllers and Microcontrollers with Different Supply Levels
- Fully Compatible with the ISO 11898 Standard
- High Speed (up to 1 Mb)
- Very Low Electromagnetic Emission (EME)
- V_{SPLIT} Voltage Source for Stabilizing the Recessive Bus Level if Split Termination is Used (Further Improvement of EME)
- Differential Receiver with High Common-Mode Range for Electromagnetic Immunity (EMI)
- Up to 110 Nodes can be Connected in Function of the Bus Topology
- Transmit Data (TxD) Dominant Time-out Function
- Bus Error Detection with Version NCV7341D20
- Bus Pins Protected Against Transients in Automotive Environments
- Bus Pins and Pin V_{SPLIT} Short-Circuit Proof to Battery and Ground
- Thermally Protected
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Controls
- These are Pb-Free Devices*

Typical Applications

- Automotive
- Industrial Networks

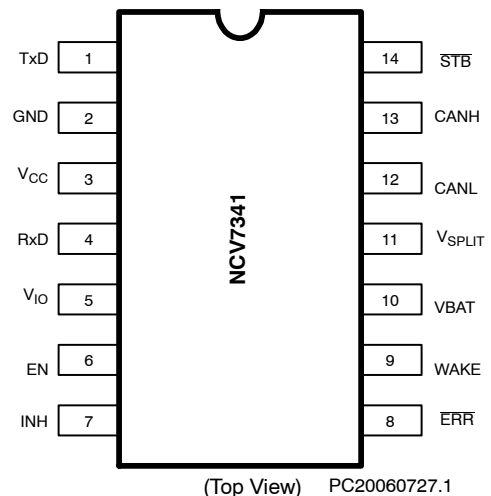
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 17 of this data sheet.

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Table 1. TECHNICAL CHARACTERISTICS

| Symbol | Parameter | Condition | Max | Max | Unit |
|------------------------|---|--|----------|----------------|------|
| V_{CC} | Supply Voltage for the Core Circuitry | | 4.75 | 5.25 | V |
| V_{IO} | Supply Voltage for the Digital Interface | | 2.8 | 5.25 | V |
| V_{EN} | DC Voltage at Pin EN | | -0.3 | $V_{IO} + 0.3$ | V |
| $\overline{V_{STB}}$ | DC Voltage at Pin \overline{STB} | | -0.3 | $V_{IO} + 0.3$ | V |
| V_{TxD} | DC Voltage at Pin TxD | | -0.3 | $V_{IO} + 0.3$ | V |
| V_{RxD} | DC Voltage at Pin RxD | | -0.3 | $V_{IO} + 0.3$ | V |
| $\overline{V_{ERR}}$ | DC Voltage at Pin \overline{ERR} | | -0.3 | $V_{IO} + 0.3$ | V |
| V_{CANH} | DC Voltage at Pin CANH | $0 < V_{CC} < 5.25$ V; No Time Limit | -58 | +58 | V |
| V_{CANL} | DC Voltage at Pin CANL | $0 < V_{CC} < 5.25$ V; No Time Limit | -58 | +58 | V |
| V_{SPLIT} | DC Voltage at Pin V_{SPLIT} | $0 < V_{CC} < 5.25$ V; No time Limit | -58 | +58 | V |
| $V_{O(dif)(bus_dom)}$ | Differential Bus Output Voltage in Dominant State | $42.5 \Omega < R_{LT} < 60 \Omega$ | 1.5 | 3 | V |
| CM_{range} | Input Common-Mode Range for Comparator | Guaranteed Differential Receiver Threshold and Leakage Current | -35 | +35 | V |
| C_{load} | Load Capacitance on IC Outputs | | | 15 | pF |
| $t_{pd(rec-dom)}$ | Propagation Delay TxD to RxD | See Figure 6 | 90 | 230 | ns |
| $t_{pd(dom-rec)}$ | Propagation Delay TxD to RxD | See Figure 6 | 90 | 245 | ns |
| T_J | Junction Temperature | | -40 | 150 | °C |
| ESD_{HBM} | ESD Level, Human Body Model | Pins CANH, CANL, V_{SPLIT} , WAKE, V_{BAT} other Pins | -4 -3 | 4 3 | kV |

NCV7341

BLOCK DIAGRAM

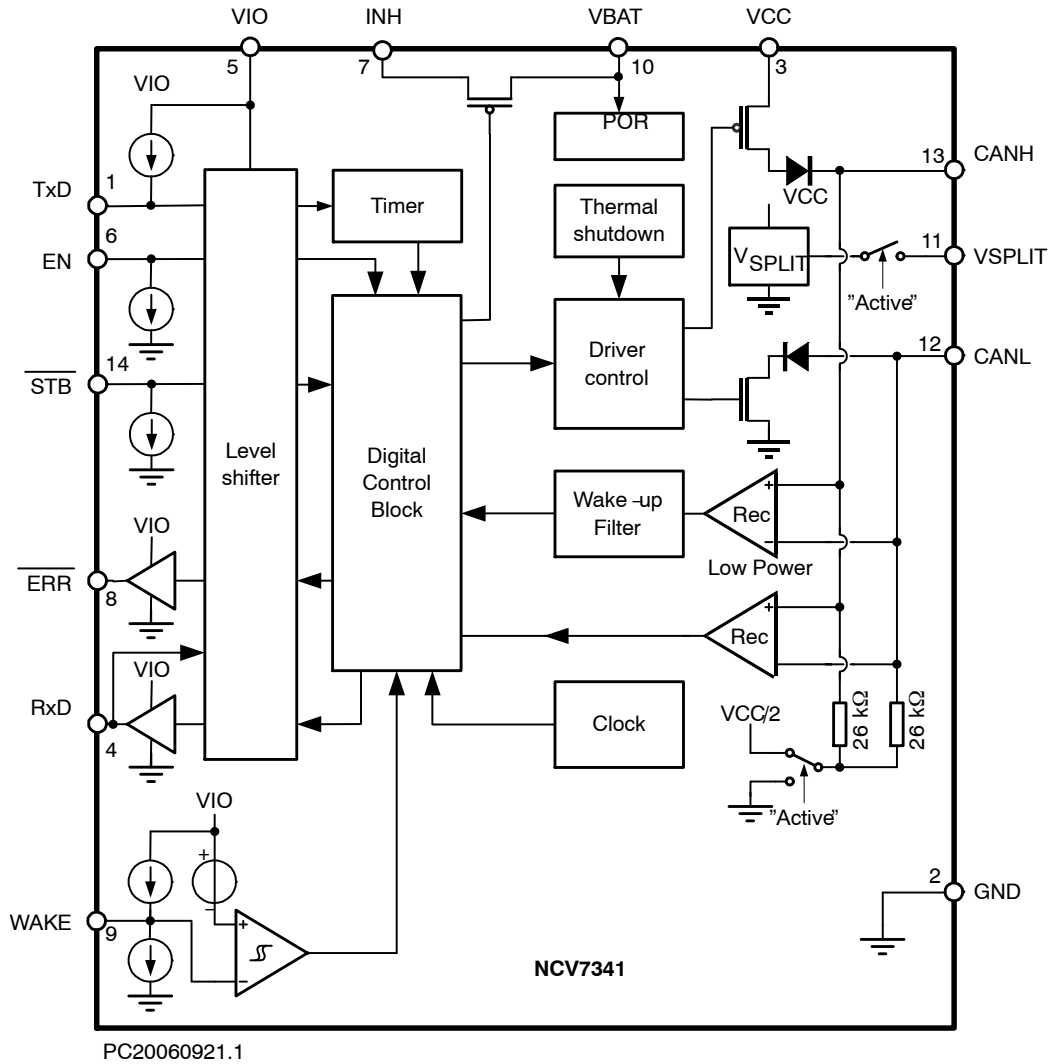
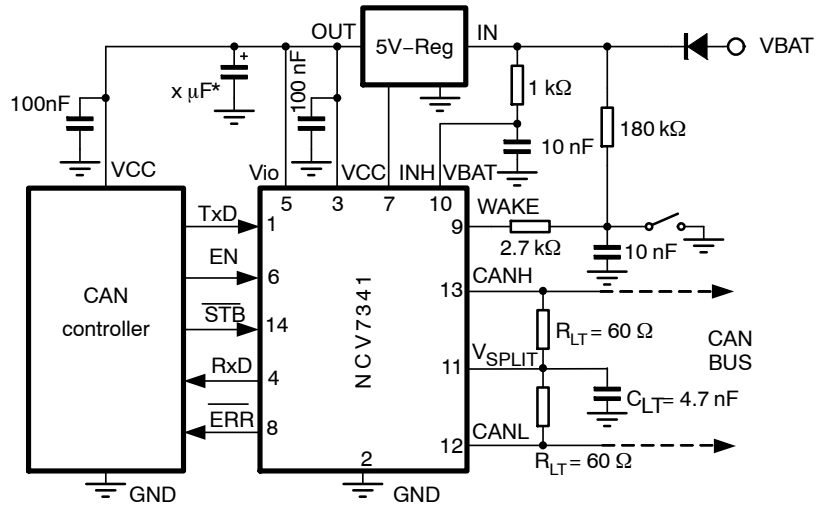


Figure 1. Block Diagram

NCV7341

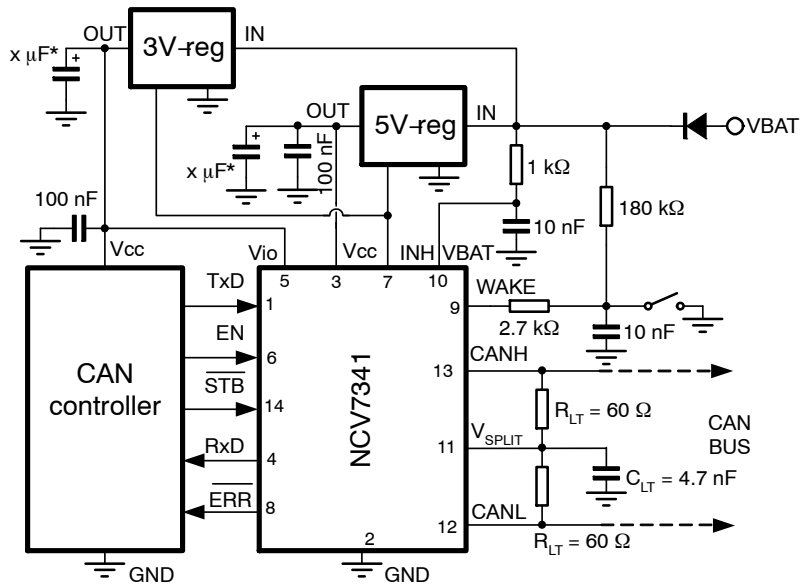
TYPICAL APPLICATION SCHEMATICS



Note (*): Value depending on regulator

PC20060921.4

Figure 2. Application Diagram with a 5V CAN Controller



Note (*): Value depending on regulator

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Figure 3. Application Diagram with a 3V CAN Controller

NCV7341

PIN DESCRIPTION

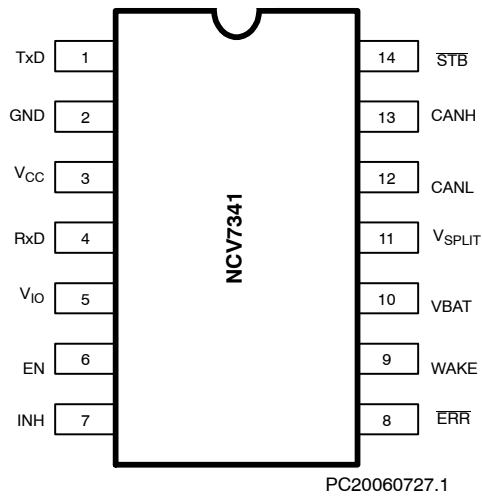


Figure 4. NCV7340 Pin Assignment

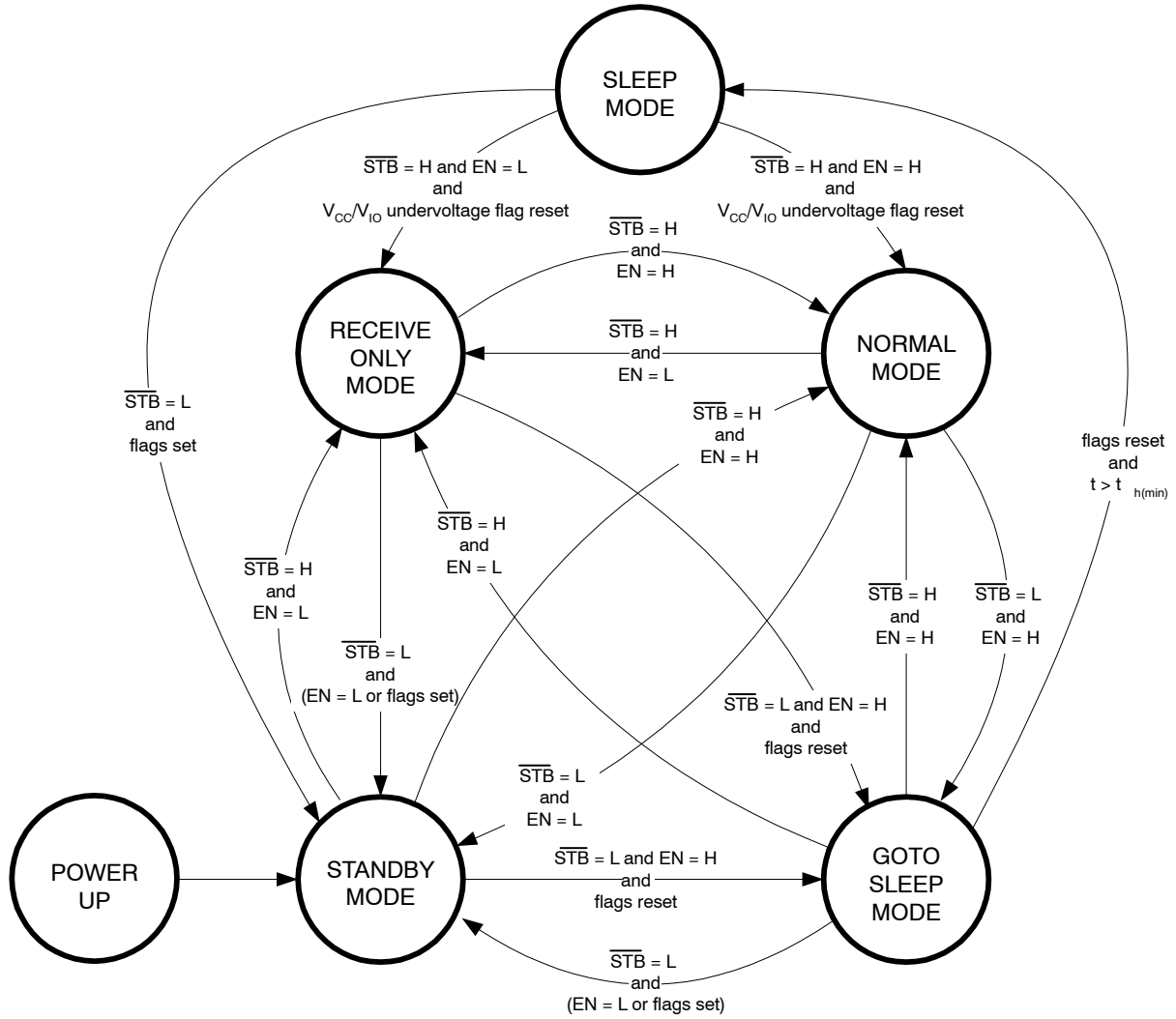
Table 2. PIN DESCRIPTION

| Pin | Name | Description |
|-----|--------------------|--|
| 1 | TxD | Transmit data input; low level = dominant on the bus; internal pull-up current |
| 2 | GND | Ground |
| 3 | V _{CC} | Supply voltage for the core circuitry and the transceiver |
| 4 | RxD | Receive data output; dominant bus => low output |
| 5 | V _{IO} | Supply voltage for the CAN controller interface |
| 6 | EN | Enable input; internal pull-down current |
| 7 | INH | High voltage output for controlling external voltage regulators |
| 8 | ERR | Digital output indicating errors and power-up; active low |
| 9 | WAKE | Local wake-up input |
| 10 | V _{BAT} | Battery supply connection |
| 11 | V _{SPLIT} | Common-mode stabilization output |
| 12 | CANL | Low-level CAN bus line (low in dominant) |
| 13 | CANH | High-level CAN bus line (high in dominant) |
| 14 | STB | Stand-by mode control input; internal pull-down current |

FUNCTIONAL DESCRIPTION

OPERATING MODES

Operation modes of NCV7341 are shown in Figures 5 and in Table 3.



LEGEND

"Flags set" : wake-up or power-up
 "Flags reset" : not (wake-up or power-up)

PC20060921.2

Figure 5. Operation Modes

Table 3. OPERATION MODES

| Conditions | | | | | Transceiver Behavior | |
|------------|--------|--|------------------------------------|-------------------------|-----------------------------|----------|
| Pin STB | Pin EN | V _{CC} /V _{IO} Undervoltage Flag | V _{BAT} Undervoltage Flag | Power-up or Wakeup Flag | Operating Mode | Pin INH |
| X | X | Set | X | X | Sleep | Floating |
| | | Reset | Set | Set | Standby | High |
| | | | | Reset | If in sleep, then no change | Floating |
| | | | | | otherwise stand-by | High |
| Low | Low | Reset | Reset | Set | Stand-by | High |
| | | | | Reset | If in sleep, then no change | Floating |
| | | | | | otherwise stand-by | High |
| Low | High | Reset | Reset | Set | Stand-by | High |
| | | | | Reset | If in sleep, then no change | Floating |
| | | | | | otherwise go-to-sleep | High |
| High | Low | Reset | Reset | X | Receive-only | High |
| High | High | Reset | Reset | X | Normal | High |

Normal Mode

In Normal mode, the transceiver is able to communicate via the bus lines. The CAN controller can transmit data to the bus via TxD pin and receive data from the bus via Pin RxD. The bus lines (CANH and CANL) are internally biased to V_{CC}/2 via the common-mode input resistance. Pin V_{SPLIT} is also providing voltage V_{CC}/2 which can be further used to externally stabilize the common mode voltage of the bus – see Figure 2 and Figure 3. Pin INH is active (pulled high) so that the external regulators controlled by INH Pin are switched on.

Receive-Only Mode

In Receive-only mode, the CAN transmitter is disabled. The CAN controller can still receive data from the bus via RxD Pin as the receiver part remains active. Equally to normal mode, the bus lines (CANH and CANL) are internally biased to V_{CC}/2 and Pin V_{SPLIT} is providing voltage V_{CC}/2. Pin INH is also active (pulled high).

Standby Mode

Standby mode is a low-power mode. Both the transmitter and the receiver are disabled and a very low-power differential receiver monitors the CAN bus activity. Bus lines are biased internally to ground via the common mode input resistance and Pin V_{SPLIT} is high-impedant (floating). A wake-up event can be detected either on the CAN bus or on the WAKE Pin. A valid wake-up is signaled on pins ERR and RxD. Pin INH remains active (pulled high) so that the external regulators controlled by INH Pin are switched on.

Go-To-Sleep Mode

Go-To-Sleep mode is an intermediate state used to put the transceiver into sleep mode in a controlled way. Go-To-Sleep mode is entered when the CAN controller

puts pin EN to High and $\overline{\text{STB}}$ Pin to Low. If the logical state of Pins EN and $\overline{\text{STB}}$ is kept unchanged for minimum period of t_{h(min)} and neither a wake-up nor a power-up event occur during this time, the transceiver enters sleep mode. While in go-to-sleep mode, the transceiver behaves identically to stand-by mode.

Sleep Mode

Sleep mode is a low-power mode in which the consumption is further reduced compared to stand-by mode. Sleep mode can be entered via go-to-sleep mode or in case an undervoltage on either V_{CC} or V_{IO} occurs for longer than the under-voltage detection time. The transceiver behaves identically to standby mode, but the INH Pin is deactivated (left floating) and the external regulators controlled by INH Pin are switched off. In this way, the V_{BAT} consumption is reduced to a minimum. The device will leave sleep mode either by a wake-up event (in case of a CAN bus wake-up or via Pin WAKE) or by putting Pin $\overline{\text{STB}}$ high (as long as an under-voltage on V_{CC} or V_{IO} is not detected).

Internal Flags

The transceiver keeps several internal flags reflecting conditions and events encountered during its operation. Some flags influence the operation mode of the transceiver (see Figure 5 and Table 3). Beside the undervoltage and the TxD dominant timeout flags, all others can be read by the CAN controller on Pin ERR. Pin ERR signals internal flags depending on the operation mode of the transceiver. An overview of the flags and their visibility on Pin ERR is given in Table 4. Because the ERR Pin uses negative logic, it will be pulled low if the signaled flag is set and will be pulled high if the signaled flag is reset.

Table 4. INTERNAL FLAGS AND THEIR VISIBILITY

| Internal Flag | Set Condition | Reset Condition | Visibility on Pin ERR |
|---|--|--|---|
| V _{CC} /V _{IO} Undervoltage | V _{CC} < V _{CC(SLEEP)} longer than t _{UV(VCC)} or V _{IO} < V _{IO(SLEEP)} longer than t _{UV(VIO)} | At wake-up or power-up | No |
| V _{BAT} Undervoltage | V _{BAT} < V _{BAT(STB)} | When V _{BAT} recovers | No |
| Powerup | V _{BAT} rises above V _{BAT(PWUP)} (V _{BAT} connection to the transceiver) | When normal mode is entered | In receive-only mode. Not going from normal mode |
| Wake-up | When remote or local wake-up is detected | At power-up or when normal mode is entered or when V _{CC} /V _{IO} undervoltage flag is set | Both on \overline{ERR} and RxD (both pulled to low). In go-to-sleep, standby and sleep mode. |
| Local Wake-up | When local wake-up is detected (i.e. via pin WAKE) | At power-up or when leaving normal mode | In normal mode before 4 consecutive dominant symbols are sent. Then \overline{ERR} pin becomes High again |
| Failure | Pin TxD clamped low or overtemperature | When entering normal mode or when RxD is Low while TxD is high (provided all failures disappeared) | Overtemperature condition observable in receive-only mode entered from normal mode |
| Bus Failure (NCV7341D20) | One of the bus lines shorted to ground or supply during four consecutive transmitted dominants | No bus line short (to ground or supply) detected during four consecutive dominant bit transmissions | In normal mode |

V_{CC}/V_{IO} Undervoltage Flag

The V_{CC}/V_{IO} undervoltage flag is set if V_{CC} supply drops below V_{CC(sleep)} level for longer than t_{UV(VCC)} or V_{IO} supply drops below V_{IO(sleep)} level for longer than t_{UV(VIO)}. If the flag is set, the transceiver enters sleep mode. After a waiting time identical to the undervoltage detection times t_{UV(VCC)} and t_{UV(VIO)}, respectively, the flag can be reset either by a valid wake-up request or when the powerup flag is set. During this waiting time, the wakeup detection is blocked.

V_{BAT} Under-voltage Flag

The flag is set when V_{BAT} supply drops below V_{BAT(STB)} level. The transceiver will enter the standby mode. The flag is reset when V_{BAT} supply recovers. The transceiver then enters the mode defined by inputs \overline{STB} and EN.

Power-up Flag

This flag is set when V_{BAT} supply recovers after being below V_{BAT(PWUP)} level, which corresponds to a connection of the transceiver to the battery. The V_{CC}/V_{IO} undervoltage flag is cleared so that the transceiver cannot enter the Go-to-sleep Mode, ensuring that INH Pin is high and the external voltage regulators are activated at the battery connection. In Receive-only mode, the powerup flag can be observed on the \overline{ERR} Pin. The flag is reset when Normal mode is entered.

Wake-up Flag

This flag is set when the transceiver detects a valid wake-up request via the bus or via the WAKE Pin. Setting the wake-up flag is blocked during the waiting time of the V_{CC}/V_{IO} undervoltage flag. The wake-up flag is immediately propagated to Pins \overline{ERR} and RxD – provided that supplies V_{CC} and V_{IO} are available. The wake-up flag

is reset at power-up or when V_{CC}/V_{IO} undervoltage occurs or when Normal mode is entered.

Local wake-up Flag

This flag is set when a valid wake-up request through WAKE Pin occurs. It can be observed on the \overline{ERR} Pin in normal mode. It can only be set when the powerup flag is reset. The local wake-up flag is reset at powerup or at leaving Normal mode.

Failure Flag

The failure flag is set in one of the following situations:

- TxD Pin is Low (i.e. dominant is requested by the CAN controller) for longer than t_{dom(TxD)} – Under this condition, the transmitter is disabled so that a bus lockup is avoided in case of an application failure which would drive permanent dominant on the bus. The transmitter remains disabled until the failure flag is reset.
- Overtemperature – If the junction temperature reaches T_{J(SD)}, the transmitter is disabled in order to protect it from overheating and the failure flag is set. The transmitter remains disabled until the failure flag is reset.

The failure flag is reset when Normal mode is entered or when TxD pin is High while RxD pin is Low. In case of overtemperature, the failure flag is observable on pin \overline{ERR} .

Bus Failure Flag (NCV7341D20)

The transmitter of the NCV7341D20 device version allows bus failure detection. During dominant bit transmission, a short of the CANH or CANL line to ground or supply (V_{CC}, V_{BAT} or other) is internally detected. If the short circuit condition lasts for four consecutive dominant

transmissions, an internal bus failure flag is set and made immediately visible through a Low level on the ERR pin. The transmission and reception circuitry continues to function.

When four consecutive dominant transmissions succeed without a bus line short being detected, the internal bus failure flag is reset and $\overline{\text{ERR}}$ pin is released to High level.

Split Circuit

The V_{SPLIT} Pin is operational only in normal and receive-only modes. It is floating in standby and sleep modes. The V_{SPLIT} can be connected as shown in Figure 2 and Figure 3 and its purpose is to provide a stabilized DC voltage of $V_{\text{CC}}/2$ to the bus avoiding possible steps in the common-mode signal, therefore reducing EME. These unwanted steps could be caused by an unpowered node on the network with excessive leakage current from the bus that shifts the recessive voltage from its nominal $V_{\text{CC}}/2$ level.

Wake-up

The transceiver can detect wake-up events in stand-by, go-to-sleep and sleep modes. Two types of wake-up events are handled – remote wake-up via the CAN bus or a local wake-up via the WAKE pin. A valid remote wake-up is recognized after two dominant states of the CAN bus of at least t_{dom} , each of them followed by a recessive state of at least t_{rec} .

A local wake-up is detected after a change of state (High to Low, or Low to High) on WAKE Pin which is stable for at least t_{WAKE} . To increase the EMS level of the WAKE Pin, an internal current source is connected to it. If the state of the WAKE Pin is stable at least for t_{WAKE} , the direction of the current source follows (pulldown current for Low state, pullup current for High state). It is recommended to connect Pin WAKE either to GND or VBAT if it's not used in the application.

Fail Safe Features

Fail safe behavior is ensured by the detection functions associated with the internal flags.

Furthermore, a current-limiting circuit protects the transmitter output stage from damage caused by accidental short circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

The Pins CANH and CANL are protected from automotive electrical transients (according to ISO 7637; see Figure 9). Pins TxD is pulled high and Pins $\overline{\text{STB}}$ and EN are pulled low internally should the input become disconnected. Pins TxD, $\overline{\text{STB}}$, EN and RxD will be floating, preventing reverse supply should the V_{IO} supply be removed.

ELECTRICAL CHARACTERISTICS

Definitions

All voltages are referenced to GND (Pin 2). Positive currents flow into the IC. Sinking current means the current is flowing into the pin; sourcing current means the current is flowing out of the pin.

Absolute Maximum Ratings

Stresses above those listed in the following table may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 5. ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Min. | Max. | Unit |
|---|---|---|------------|----------------|---------|
| V_{BAT} | Supply voltage | | -0.3 | 58 | V |
| V_{CC} | Supply voltage | | -0.3 | +7 | V |
| V_{IO} | Supply voltage | | -0.3 | +7 | V |
| V_{CANH} | DC voltage at pin CANH | $0 < V_{CC} < 5.25$ V; no time limit | -58 | +58 | V |
| V_{CANL} | DC voltage at pin CANL | $0 < V_{CC} < 5.25$ V; no time limit | -58 | +58 | V |
| $V_{CANL}-V_{CANH}$ | DC voltage between bus pins CANH and CANL | $0 < V_{CC} < 5.25$ V; no time limit | -58 | +58 | V |
| V_{SPLIT} | DC voltage at pin VSPLIT | $0 < V_{CC} < 5.25$ V; no time limit | -58 | +58 | V |
| V_{INH} | DC voltage at pin INH | | -0.3 | $V_{BAT}+0.3$ | V |
| V_{WAKE} | DC voltage at pin WAKE | | -0.3 | 58 | V |
| V_{TxD} | DC voltage at pin TxD | | -0.3 | 7 | V |
| V_{RxD} | DC voltage at pin RxD | | -0.3 | $V_{IO} + 0.3$ | V |
| $\overline{V_{STB}}$ | DC voltage at pin \overline{STB} | | -0.3 | 7 | V |
| V_{EN} | DC voltage at pin EN | | -0.3 | 7 | V |
| $\overline{V_{ERR}}$ | DC voltage at pin \overline{ERR} | | -0.3 | $V_{IO} + 0.3$ | V |
| $V_{tran}(CANH)$ | Transient voltage at pin CANH | (Note 1) | -300 | +300 | V |
| $V_{tran}(CANL)$ | Transient voltage at pin CANL | (Note 1) | -300 | +300 | V |
| $V_{tran}(VSPLIT)$ | Transient voltage at pin VSPLIT | (Note 1) | -300 | +300 | V |
| $V_{esd}(CANL/CANH/VSPLIT, VBAT, WAKE)$ | Electrostatic discharge voltage at pins intended to be wired outside of the module (CANH, CANL, V_{SPLIT} , VBAT, WAKE) | (Note 2) (Note 4) | -4 -500 | 4 500 | kV V |
| V_{esd} | Electrostatic discharge voltage at all other pins | (Note 2) (Note 4) | -3 -500 | 3 500 | kV V |
| Latch-up | Static latch-up at all pins | (Note 3) | | 120 | mA |
| T_{stg} | Storage temperature | | -50 | +150 | °C |
| T_{amb} | Ambient temperature | | -50 | +125 | °C |
| T_{junc} | Maximum junction temperature | | -50 | +180 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Applied transient waveforms in accordance with ISO 7637 part 3, test pulses 1, 2, 3a, and 3b (see Figure 9).
2. Standardized human body model electrostatic discharge (ESD) pulses in accordance to MIL883 method 3015.7.
3. Static latch-up immunity: Static latch-up protection level when tested according to EIA/JESD78.
4. Standardized charged device model ESD pulses when tested according to EOS/ESD DS5.3-1993.

Operating Conditions

Operating conditions define the limits for functional operation, parametric characteristics and reliability specification of the device. Functionality of the device is not guaranteed outside the operating conditions.

Table 6. OPERATING RANGES

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------------------------|---|---|------|------------------------|------|
| V _{BAT} | Supply Voltage | | 5.0 | 50 | V |
| V _{BAT_SLEEP} | Supply Voltage in the Sleep Mode | (Note 1) | 6.0 | 50 | V |
| V _{CC} | Supply Voltage | | 4.75 | 5.25 | V |
| V _{IO} | Supply Voltage | | 2.8 | 5.25 | V |
| V _{CANH} | DC Voltage at Pin CANH | Receiver Function Guaranteed | -35 | +35 | V |
| V _{CANL} | DC Voltage at Pin CANL | Receiver Function Guaranteed | -35 | +35 | V |
| V _{CANL-V_{CANH}} | DC Voltage Between Bus Pins CANH and CANL | Receiver Function Guaranteed | -35 | +35 | V |
| V _{SPLIT} | DC Voltage at Pin V _{SPLIT} | Leakage and Current Limitation are Guaranteed | -35 | +35 | V |
| V _{INH} | DC Voltage at Pin INH | | -0.3 | V _{BAT} + 0.3 | V |
| V _{WAKE} | DC Voltage at Pin WAKE | | -0.3 | V _{BAT} + 0.3 | V |
| V _{TxD} | DC Voltage at Pin TxD | | -0.3 | V _{IO} + 0.3 | V |
| V _{RxD} | DC Voltage at Pin RxD | | -0.3 | V _{IO} + 0.3 | V |
| V _{STB} | DC Voltage at Pin STB | | -0.3 | V _{IO} + 0.3 | V |
| V _{EN} | DC Voltage at Pin EN | | -0.3 | V _{IO} + 0.3 | V |
| V _{ERR} | DC Voltage at Pin ERR | | -0.3 | V _{IO} + 0.3 | V |
| C _{LOAD} | Capacitive Load on Digital Outputs (Pins RxD and ERR) | | | 15 | pF |
| T _A | Ambient Temperature | | -40 | +125 | °C |
| T _J | Maximum Junction Temperature | | -40 | +150 | °C |

1. In the sleep mode, all relevant parameters are guaranteed only for V_{BAT} > 6 V. For V_{BAT} between 5 V and 6 V, no power-on-reset will occur and the functionality is also guaranteed, but some parameters might get slightly out of the specification – e.g. the wakeup detection thresholds.

Table 7. THERMAL CHARACTERISTICS

| Symbol | Parameter | Conditions | Value | Unit |
|-----------------------|--|------------|-------|------|
| R _{th(vj-a)} | Thermal Resistance from Junction-to-Ambient in SOIC-14 Package | 1S0P PCB | 128 | K/W |
| R _{th(vj-a)} | Thermal Resistance from Junction-to-Ambient in SOIC-14 Package | 2S2P PCB | 70 | K/W |

Characteristics

The characteristics of the device are valid for operating conditions defined in Table 7 and the bus lines are considered to be loaded with $R_{LT} = 60 \Omega$, unless specified otherwise.

Table 8. DC CHARACTERISTICS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|--|---|--------------|-----|----------------|---------|
| SUPPLY (PIN VBAT) | | | | | | |
| $V_{BAT(STB)}$ | Level for Setting V_{BAT} Undervoltage Flag | $V_{CC} = 5 V$ | 2.75 | 3.3 | 4.5 | V |
| $V_{BAT(PWUP)}$ | Level for Setting Powerup Flag | $V_{CC} = 0 V$ | 2.75 | 3.3 | 4.5 | V |
| I_{VBAT} | V_{BAT} Current Consumption in Normal and Receive-Only Modes | INH and WAKE Not Loaded | 1.0 | 10 | 40 | μA |
| | V_{BAT} Current Consumption in Standby and Go-to-Sleep Modes. The total supply current is drawn partially from V_{BAT} and partially from V_{CC} . | $V_{VCC} > 4.75 V, V_{VIO} > 2.8 V$ $V_{INH} = V_{WAKE} = V_{VBAT} = 12 V$ $T_{amb} < 100^{\circ}C$ | | | 18 | μA |
| | | $V_{VCC} > 4.75 V, V_{VIO} > 2.8 V$ $V_{INH} = V_{WAKE} = V_{VBAT} = 12 V$ | 8.0 | 12 | 22.5 | μA |
| | V_{BAT} Current Consumption in Sleep Mode. The supply current is drawn from V_{BAT} only. | $V_{VCC} = V_{INH} = V_{VIO} = 0 V$ $V_{WAKE} = V_{VBAT} = 12 V$ $T_{amb} < 100^{\circ}C$ | | | 35 | μA |
| $V_{VCC} = V_{INH} = V_{VIO} = 0 V$ $V_{WAKE} = V_{VBAT} = 12 V$ | | 10 | 20 | 50 | μA | |
| SUPPLY (PIN VCC) | | | | | | |
| $V_{CC(SLEEP)}$ | V_{CC} Level for Setting V_{CC}/V_{IO} Undervoltage Flag | $V_{BAT} = 12 V$ | 2.75 | 3.3 | 4.5 | V |
| I_{VCC} | V_{CC} Current Consumption in Normal or Receive-Only Mode | Normal Mode: $V_{TXD} = 0 V$, i.e. Dominant | 25 | 55 | 80 | mA |
| | | Normal Mode: $V_{TXD} = V_{IO}$, i.e. Recessive (or Receive-Only Mode) | 2.0 | 6.0 | 10 | mA |
| | V_{CC} Current Consumption in Standby and Go-to-Sleep Mode. The total supply current is drawn partially from V_{BAT} and partially from V_{CC} . | $T_{amb} < 100^{\circ}C$ | | | 17.5 | μA |
| | | | 6.5 | 12 | 19.5 | μA |
| | V_{CC} Current Consumption in Sleep Mode | $T_{amb} < 100^{\circ}C$ | | | 1.0 | μA |
| | | 0.2 | 0.5 | 2.0 | μA | |
| SUPPLY (PIN VIO) | | | | | | |
| $V_{IO(SLEEP)}$ | V_{IO} Level for Setting V_{CC}/V_{IO} Undervoltage Flag | | 0.9 | 1.6 | 2.0 | V |
| I_{VIO} | V_{IO} Current Consumption in Normal or Receive-Only Mode | Normal Mode: $V_{TXD} = 0V$, i.e. Dominant | 100 | 350 | 1000 | μA |
| | | Normal Mode: $V_{TXD} = V_{IO}$, i.e. Recessive (or Receive-Only mode) | 0 | 0.2 | 1.0 | μA |
| | V_{IO} Current Consumption in Standby or Sleep Mode | $T_{amb} < 100^{\circ}C$ | | | 1.0 | μA |
| | | 0 | 0 | 5.0 | μA | |
| TRANSMITTER DATA INPUT (PIN TXD) | | | | | | |
| V_{IH} | High-Level Input Voltage | Output Recessive | $0.7V_{VIO}$ | - | $V_{IO} + 0.3$ | V |
| V_{IL} | Low-Level Input Voltage | Output Dominant | -0.3 | - | $0.3V_{VIO}$ | V |
| I_{IH} | High-Level Input Current | $V_{TXD} = V_{VIO}$ | -5.0 | 0 | +5.0 | μA |

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Table 8. DC CHARACTERISTICS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|---|---|------------------|--------------------|------------------|---------|
| TRANSMITTER DATA INPUT (PIN TxD) | | | | | | |
| I_{IL} | Low-Level Input Current | $V_{TxD} = 0.3 V_{VIO}$ | -70 | -250 | -500 | μA |
| C_i | Input Capacitance | Not Tested | 1.0 | 5.0 | 10 | μF |
| STANDBY AND ENABLE INPUTS (PINS STB AND EN) | | | | | | |
| V_{IH} | High-Level Input Voltage | | $0.7V_{VIO}$ | - | $V_{IO} + 0.3$ | V |
| V_{IL} | Low-Level Input Voltage | | -0.3 | - | $0.3V_{VIO}$ | V |
| I_{IH} | High-Level Input Current | $V_{STB} = V_{EN} = 0.7V_{VIO}$ | 1.0 | 5.0 | 10 | μA |
| I_{IL} | Low-Level Input Current | $V_{STB} = V_{EN} = 0 V$ | -0.5 | 0 | 5.0 | μA |
| C_i | Input Capacitance | | 1.0 | 5.0 | 10 | μF |
| RECEIVER DATA OUTPUT (PIN RxD) | | | | | | |
| I_{OH} | High-Level Output Current | $V_{RxD} = V_{VIO} - 0.4 V$ $V_{VIO} = V_{VCC}$ | -1.0 | -3.0 | -6.0 | mA |
| I_{OL} | Low-Level Output Current | $V_{RxD} = 0.4 V$ $V_{TxD} = 0 V$ Bus is Dominant | 2.0 | 5.0 | 12 | mA |
| FLAG INDICATION OUTPUT (PIN ERR) | | | | | | |
| I_{OH} | High-Level Output Current | $V_{ERR} = V_{VIO} - 0.4 V$ $V_{VIO} = V_{VCC}$ | -4.0 | -20 | -50 | μA |
| I_{OL} | Low-Level Output Current | $V_{ERR} = 0.4 V$ | 100 | 200 | 350 | μA |
| LOCAL WAKE-UP INPUT (PIN WAKE) | | | | | | |
| I_{IH} | High-Level Input Current | $V_{WAKE} = V_{VBAT} - 1.9 V$ | -1.0 | -5.0 | -10 | μA |
| I_{IL} | Low-Level Input Current | $V_{WAKE} = V_{VBAT} - 3.1 V$ | 1.0 | 5.0 | 10 | μA |
| $V_{threshold}$ | Threshold of the Local Wake-up Comparator | Sleep or Standby Mode | $V_{VBAT} - 3 V$ | $V_{VBAT} - 2.5 V$ | $V_{VBAT} - 2 V$ | V |
| INHIBIT OUTPUT (PIN INH) | | | | | | |
| V_{HDROP} | High Level Voltage Drop | $I_{INH} = -180 \mu A$ | 50 | 200 | 800 | mV |
| I_{LEAK} | Leakage Current in Sleep Mode | | 0 | - | 5.0 | μA |
| | | $T_{amb} < 100^\circ C$ | 0 | - | 1.0 | μA |
| BUS LINES (PINS CANH AND CANL) | | | | | | |
| $V_{o(reces)} (norm)$ | Recessive Bus Voltage | $V_{TxD} = V_{VCC}$; No Load, Normal Mode | 2.0 | 2.5 | 3.0 | V |
| $V_{o(reces)} (stby)$ | Recessive Bus Voltage | $V_{TxD} = V_{VCC}$; No Load, Standby Mode | -100 | 0 | 100 | mV |
| $I_{o(reces)} (CANH)$ | Recessive Output Current at Pin CANH | $-35 V < V_{CANH} < +35 V$; $0 V < V_{CC} < 5.25 V$ | -2.5 | - | +2.5 | mA |
| $I_{o(reces)} (CANL)$ | Recessive Output Current at Pin CANL | $-35 V < V_{CANL} < +35 V$; $0 V < V_{VCC} < 5.25 V$ | -2.5 | - | +2.5 | mA |
| $V_{o(dom)} (CANH)$ | Dominant output Voltage at Pin CANH | $V_{TxD} = 0 V$ | 3.0 | 3.6 | 4.25 | V |
| $V_{o(dom)} (CANL)$ | Dominant Output Voltage at Pin CANL | $V_{TxD} = 0 V$ | 0.5 | 1.4 | 1.75 | V |
| $V_{o(dif)} (bus_dom)$ | Differential Bus Output Voltage ($V_{CANH} - V_{CANL}$) | $V_{TxD} = 0 V$; Dominant; $42.5 \Omega < R_{LT} < 60 \Omega$ | 1.5 | 2.25 | 3.0 | V |
| $V_{o(dif)} (bus_rec)$ | Differential Bus Output Voltage ($V_{CANH} - V_{CANL}$) | $V_{TxD} = V_{CC}$; Recessive; No Load | -120 | 0 | +50 | mV |
| $I_{o(sc)} (CANH)$ | Short-Circuit Output Current at Pin CANH | $V_{CANH} = 0 V$; $V_{TxD} = 0 V$ | -45 | -70 | -120 | mA |

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Table 8. DC CHARACTERISTICS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|--|---|---------------------|---------------------|---------------------|------------------|
| BUS LINES (PINS CANH AND CANL) | | | | | | |
| $I_{o(sc)}$ (CANL) | Short-Circuit Output Current at Pin CANL | $V_{CANL} = 42\text{ V}; V_{TXD} = 0\text{ V}$ | 45 | 70 | 120 | mA |
| $V_{i(dif)}$ (th) | Differential Receiver Threshold Voltage (see Figure 7) | $-12\text{ V} < V_{CANL} < +12\text{ V}$ $-12\text{ V} < V_{CANH} < +12\text{ V}$ | 0.5 | 0.7 | 0.9 | V |
| $V_{ihcm(dif)}$ (th) | Differential Receiver Threshold Voltage for High Common-Mode (see Figure 7) | $-35\text{ V} < V_{CANL} < +35\text{ V}$ $-35\text{ V} < V_{CANH} < +35\text{ V}$ | 0.35 | 0.7 | 1.00 | V |
| $V_{i(dif)}$ (hys) | Differential Receiver Input Voltage Hysteresis (see Figure 7) | $-35\text{ V} < V_{CANL} < +35\text{ V}$ $-35\text{ V} < V_{CANH} < +35\text{ V}$ | 50 | 70 | 100 | mV |
| $V_{I(dif_WAKE)}$ | Differential Receiver Input Voltage for Bus Wake-up Detection (in Sleep or Standby Mode) | $-12\text{ V} < V_{CANH} < +12\text{ V}$ $-12\text{ V} < V_{CANL} < +12\text{ V}$ | 0.4 | 0.8 | 1.15 | V |
| $R_{i(cm)}$ (CANH) | Common-Mode Input Resistance at Pin CANH | | 15 | 26 | 39 | k Ω |
| $R_{i(cm)}$ (CANL) | Common-Mode Input Resistance at Pin CANL | | 15 | 26 | 39 | k Ω |
| $R_{i(cm)}$ (m) | Matching between Pin CANH and Pin CANL Common Mode Input Resistance | $V_{CANH} = V_{CANL}$ | -3.0 | 0 | +3.0 | % |
| $R_{i(dif)}$ | Differential Input Resistance | | 25 | 50 | 75 | k Ω |
| $C_{i(CANH)}$ | Input Capacitance at Pin CANH | $V_{TXD} = V_{CC}$ | | 7.5 | 20 | pF |
| $C_{i(CANL)}$ | Input Capacitance at Pin CANL | $V_{TXD} = V_{CC}$ | | 7.5 | 20 | pF |
| $C_{i(dif)}$ | Differential Input Capacitance | $V_{TXD} = V_{CC}$ | | 3.75 | 10 | pF |
| COMMON-MODE STABILIZATION (PIN V_{SPLIT}) | | | | | | |
| V_{SPLIT} | Reference Output Voltage at Pin V_{SPLIT} | Normal mode; $-500\text{ }\mu\text{A} < I_{SPLIT} < 500\text{ }\mu\text{A}$ | $0.3 \times V_{CC}$ | $0.5 \times V_{CC}$ | $0.7 \times V_{CC}$ | |
| $I_{SPLIT(i)}$ | V_{SPLIT} Leakage Current | Standby Mode $-27\text{ V} < V_{SPLIT} < 40\text{ V}$ | -50 | | +50 | μA |
| | | Standby Mode $-27\text{ V} < V_{SPLIT} < 40\text{ V}$ $T_{amb} < 100^\circ\text{C}$ | -5.0 | | +5.0 | |
| $I_{SPLIT(lim)}$ | V_{SPLIT} Limitation Current (Absolute Value) | Normal Mode | 1.3 | 3.0 | 5.0 | mA |
| THERMAL SHUTDOWN | | | | | | |
| $T_{J(SD)}$ | Shutdown Junction Temperature | | 150 | 160 | 180 | $^\circ\text{C}$ |

Table 9. AC CHARACTERISTICS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|---|-----------------------------|------|-----|------|---------|
| TIMING CHARACTERISTICS (Figure 6) | | | | | | |
| $t_{d(TxD-BUSon)}$ | Delay TxD to Bus Active | Setup According to Figure 8 | 40 | 85 | 105 | ns |
| $t_{d(TxD-BUSoff)}$ | Delay TxD to Bus Inactive | Setup According to Figure 8 | 30 | 60 | 105 | ns |
| $t_{d(BUSon-RxD)}$ | Delay Bus Active to RxD | Setup According to Figure 8 | 25 | 55 | 105 | ns |
| $t_{d(BUSoff-RxD)}$ | Delay Bus Inactive to RxD | Setup According to Figure 8 | 40 | 65 | 105 | ns |
| $t_{pd(rec-dom)}$ | Propagation Delay TxD to RxD from Recessive to Dominant | Setup According to Figure 8 | 90 | 130 | 230 | ns |
| $t_{d(dom-rec)}$ | Propagation Delay TxD to RxD from Dominant to Recessive | Setup According to Figure 8 | 90 | 140 | 245 | ns |
| $t_{UV(VCC)}$ | Undervoltage Detection Time on V_{CC} | | 5.0 | 10 | 12.5 | ms |
| $t_{UV(VIO)}$ | Undervoltage Detection Time on V_{IO} | | 5.0 | 10 | 12.5 | ms |
| $t_{dom(TxD)}$ | TxD Dominant Timeout | | 300 | 600 | 1000 | μ s |
| $t_{h(min)}$ | Minimum Hold-Time for the Go-to-Sleep Mode | | 15 | 35 | 50 | μ s |
| t_{dom} | Dominant Time for Wake-up via the Bus | $V_{dif}(CAN) > 1.4 V$ | 0.75 | 2.5 | 5.0 | μ s |
| | | $V_{dif}(CAN) > 1.2 V$ | 0.75 | 3.0 | 5.8 | μ s |
| t_{rec} | Recessive Time for Wake-up via the Bus | $V_{BAT} = 12 V$ | 0.75 | 2.5 | 5.0 | μ s |
| t_{WAKE} | Debounce Time for the Wake-up via WAKE Pin | $V_{BAT} = 12 V$ | 5.0 | 25 | 50 | μ s |
| t_{errdet} | Minimum dominant bit time for bus error detection | NCV7341D20 version | 1 | 2 | 4 | μ s |

MEASUREMENT DEFINITIONS AND SETUPS

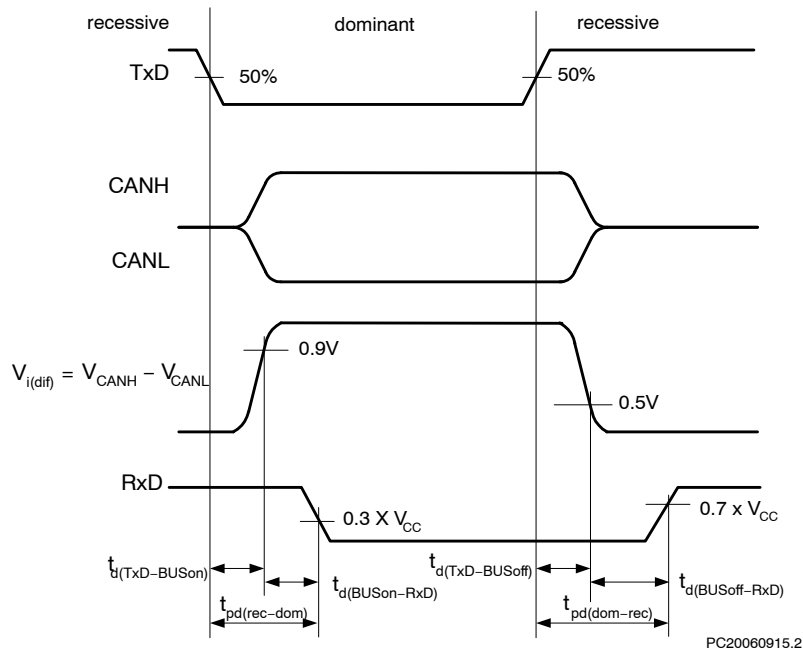


Figure 6. Timing Diagram for AC Characteristics

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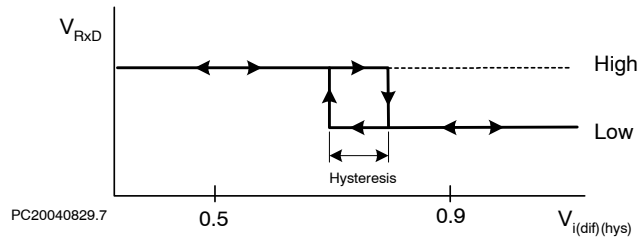


Figure 7. Hysteresis of the Receiver

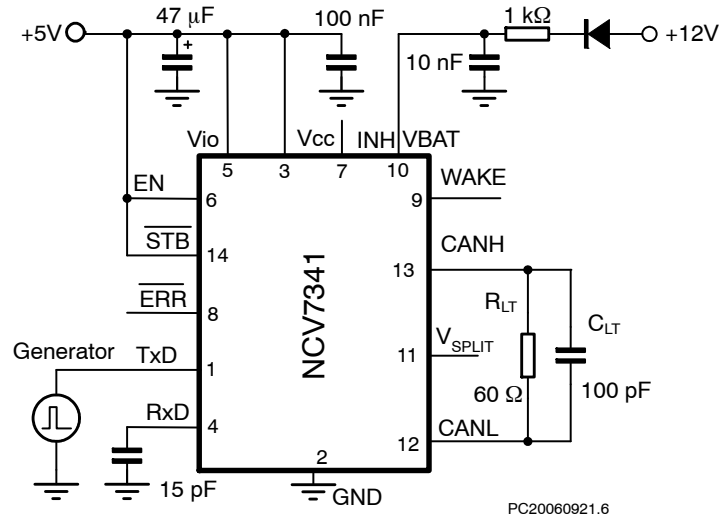


Figure 8. Test Circuit for Timing Characteristics

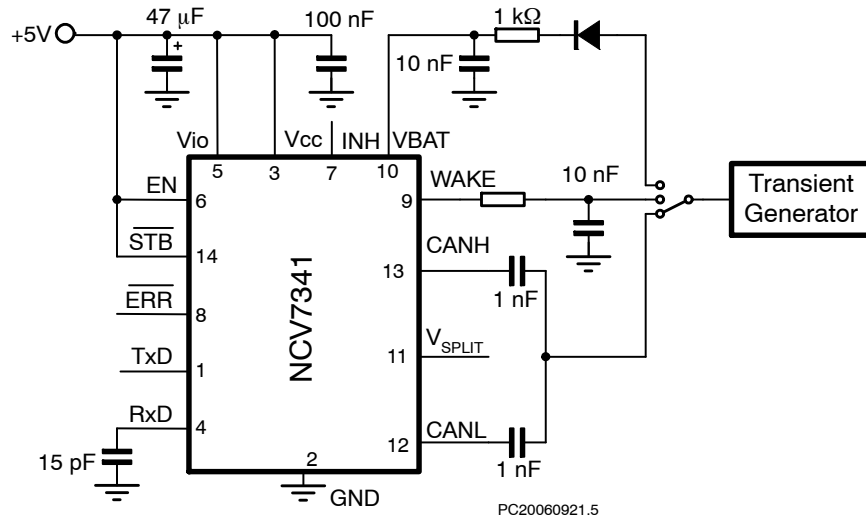


Figure 9. Test Circuit for Automotive Transients

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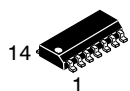
DEVICE ORDERING INFORMATION

| Part Number | Description | Temperature Range | Package Type | Shipping† |
|---------------|--|-------------------|----------------------|--------------------|
| NCV7341D20G | HS CAN Transceiver with bus error detection | -40°C – 125°C | SOIC-14 (Pb-Free) | 55 Tube / Tray |
| NCV7341D20R2G | | -40°C – 125°C | SOIC-14 (Pb-Free) | 3000 / Tape & Reel |
| NCV7341D21G | HS CAN Transceiver | -40°C – 125°C | SOIC-14 (Pb-Free) | 55 Tube / Tray |
| NCV7341D21R2G | | -40°C – 125°C | SOIC-14 (Pb-Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

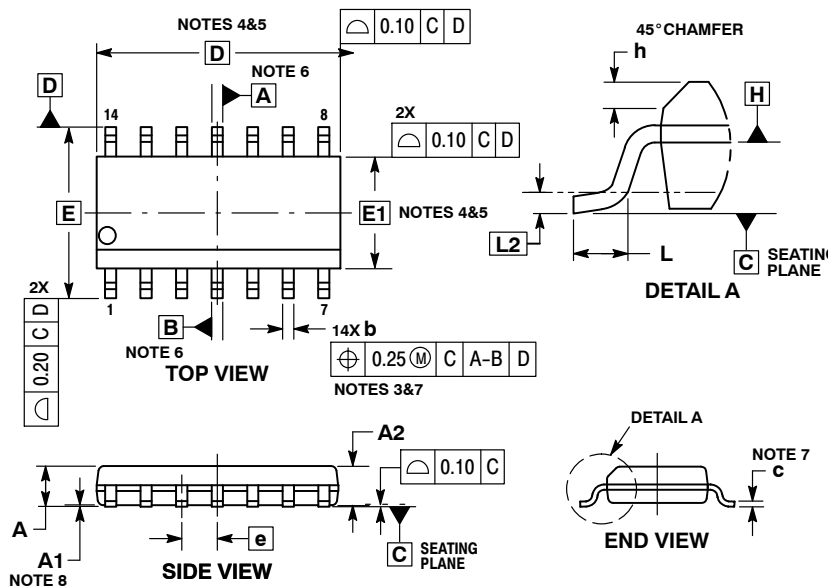
ON Semiconductor®



SCALE 1:1

SOIC-14 CASE 751AP ISSUE B

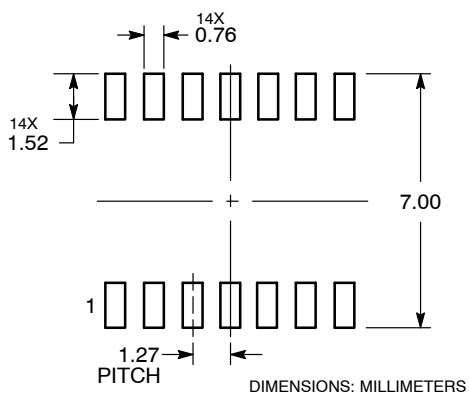
DATE 18 MAY 2015



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
 4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006 mm PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
 5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTER-MOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
 6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM H.
 7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
 8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

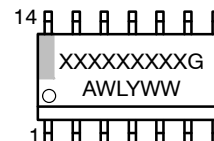
| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | --- | 1.75 |
| A1 | 0.10 | 0.25 |
| A2 | 1.25 | --- |
| b | 0.31 | 0.51 |
| c | 0.10 | 0.25 |
| D | 8.65 BSC | |
| E | 6.00 BSC | |
| E1 | 3.90 BSC | |
| e | 1.27 BSC | |
| h | 0.25 | 0.41 |
| L | 0.40 | 1.27 |
| L2 | 0.25 BSC | |

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

| | | |
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