Twelve Low-Side Relay Drivers

NCV7751

The NCV7751 is an automotive grade twelve channel low−side driver providing drive capability up to 600 mA per channel. Output control is via a SPI communication and offers convenient reporting of faults for open load (or short to ground), over load, and over temperature conditions. Additionally, all the drivers have integrated output clamps for inductive loads.

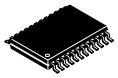
The NCV7751 is available in a SSOP−24 exposed pad package for optimal thermal performance.

Features

- 12 Channels
- 600 mA Low−Side Drivers
  - $R_{DS(on)}$ 1.3 Ω (typ), 2.5 Ω (max)
- Configurable SPI Control (16/24/32 Bit)
  - Compatible with NCV7240
  - Frame Error Detection
  - Daisy Chain Capable
- Power Up Without Open Circuit Detection Active (for LED applications)
- Low Quiescent Current in Sleep and Standby Modes
- 3.3 V and 5 V compatible Digital Input Supply Range
- Fault Reporting
  - Open Load Detection (Selectable)
  - Over Load
  - Over Temperature
- Power−on Reset (VDD, VDDA)
- SSOP−24 with an Exposed Pad
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Automotive Body Control Unit
- Automotive Engine Control Unit
- Relay Drive
- LED Drive
- Stepper Motor



SSOP24 NB EP
CASE 940AK

MARKING DIAGRAM

−X	= Optional Wafer Fab Indicator
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCV7751DQR2G	SSOP24−EP (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

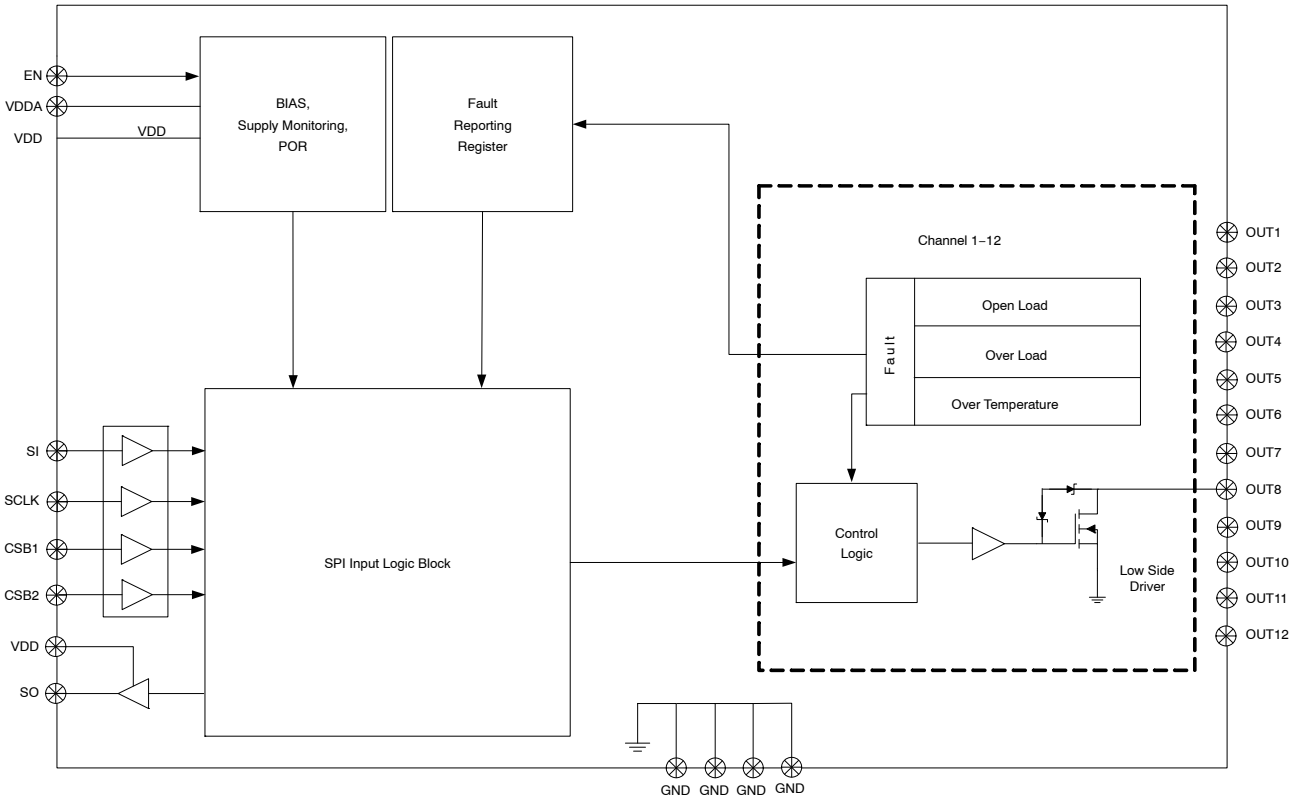


Figure 1. Block Diagram

PACKAGE PIN DESCRIPTION

SSOP−24 EPAD	Symbol	Description
1	GND	Ground.
2	GND	Ground.
3	OUT1	Channel 1 low−side drive output. Requires an external pull−up device for operation.
4	OUT2	Channel 2 low−side drive output. Requires an external pull−up device for operation.
5	OUT3	Channel 3 low−side drive output. Requires an external pull−up device for operation.
6	OUT4	Channel 4 low−side drive output. Requires an external pull−up device for operation.
7	OUT5	Channel 5 low−side drive output. Requires an external pull−up device for operation.
8	OUT6	Channel 6 low−side drive output. Requires an external pull−up device for operation.
9	OUT7	Channel 7 low−side drive output. Requires an external pull−up device for operation.
10	OUT8	Channel 8 low−side drive output. Requires an external pull−up device for operation.
11	GND	Ground.
12	GND	Ground.
13	VDD	Digital Power Supply for SO output (3.3 V or 5 V).
14	CSB2	Chip Select “Bar” Two (120 kΩ pull up resistor to VDD).
15	OUT9	Channel 9 low−side drive output. Requires an external pull−up device for operation.
16	OUT10	Channel 10 low−side drive output. Requires an external pull−up device for operation.
17	OUT11	Channel 11 low−side drive output. Requires an external pull−up device for operation.
18	OUT12	Channel 12 low−side drive output. Requires an external pull−up device for operation.
19	SO	SPI serial data output. Output high voltage level referenced to pin VDD.
20	SCLK	SPI clock (120 kΩ pull down resistor).
21	EN	Global Enable (active high). (120 kΩ pull down resistor).
22	SI	SPI serial data input (120 kΩ pull down resistor).
23	CSB1	SPI Chip Select “Bar” One (120 kΩ pull up resistor to VDD).
24	VDDA	Analog Power Supply Input voltage (5 V).
EPAD	Exposed Pad	Connect to Ground or Leave Unconnected.

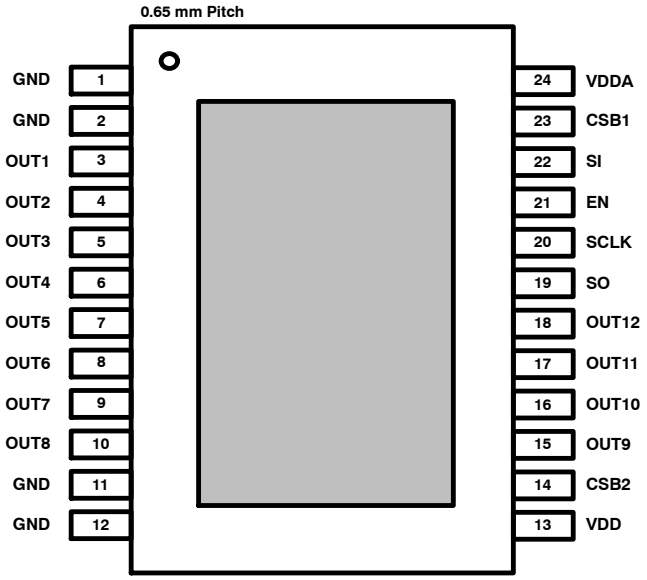


Figure 2. NCV7751 Pinout

MAXIMUM RATINGS

	Symbol	Min	Max	Unit
Supply Input Voltage (VDDA, VDD) DC	V_{dcMax}	−0.3	5.5	V
Digital I/O pin voltage (EN, CSB1, CSB2 SCLK, SI) (SO)	V_{ioMax}	−0.3 −0.3	5.5 VDD + 0.3	V
High Voltage Pins (OUTx) DC Peak Transient	$V_{outxDcMax}$ $V_{outxAcMax}$	−0.3	36 44**	V
Output Current (OUTx)		−1	1.3	A
Clamping Energy Maximum (single pulse) Repetitive (multiple pulse)***	$V_{clpDcMax}$ $V_{clpAcMax}$	– –	75 –	mJ
Operating Junction Temperature Range	T_J	−40	150	°C
Storage Temperature Range	T_{str}	−55	150	°C
ESD Capability, AEC−Q100−02 Human body model (100 pF, 1.5 kΩ) (OUTx pins) Human body model (100 pF, 1.5 kΩ) (all other pins)	V_{esd4k} V_{esd2k}	−4000 −2000	4000 2000	V
AECQ10x−12 Short Circuit Reliability Characterization	AECQ10x	Grade A	–	

PACKAGE

Moisture Sensitivity Level	MSL2	2		–
Lead Temperature Soldering: SMD style only, Reflow (Note 1) Pb−Free Part 60 − 150 sec above 217°C, 40 sec max at peak	Treflow		265 peak	°C
Package Thermal Resistance (Note 2) SSOP−24 EPAD Junction−to−Ambient	$R_{\theta JA}$		57.9	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Internally limited. Specification applies to unpowered and powered modes. (0 V to VDDA, 0 V to VDD)

***2M pulses (triangular), VS = 15 V, 63 Ω, 390 mH, T_A = 25°C. (See Figure 3)

1. For additional information, see or download **onsemi's** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D and Application Note AND8083/D.
2. Values represent typical still air steady−state thermal performance on 2 oz. copper FR4 PCB with 645 mm^2 copper area.

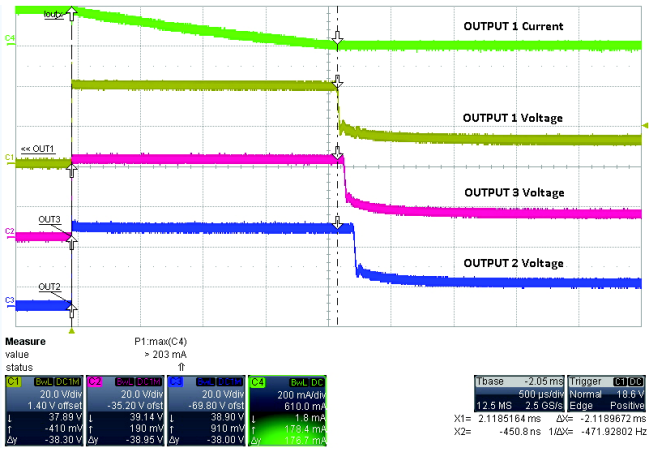


Figure 3. Repetitive Clamping Energy Test

ELECTRICAL CHARACTERISTICS (3.0 V < VDD < VDDA, 4.5 V < VDDA (Note 3) < 5.5 V, −40°C ≤ T_J ≤ 150°C, EN = VDD unless otherwise specified).

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
GENERAL						
Operating Current (VDDA) ON Mode (All Channels On)		IopVDDA	–	3	5	mA
Quiescent Current (VDDA) Global Standby Mode (All Channels Off)	SI = SCLK = 0 V, CSB1 = CSB2 = VDD −40°C ≤ T_J ≤ 125°C T_J = 150°C	$IstbyV_{DDA}125$ $IstbyV_{DDA}150$	– –	– –	32 40	μA
Quiescent Current (VDDA) Low Iq Mode	SI = SCLK = EN = 0 V, CSB1 = CSB2 = VDD −40°C ≤ T_J ≤ 125°C T_J = 150°C	$IqV_{DDA}125$ $IqV_{DDA}150$	– –	– –	10 20	μA
Operating Current (VDD) ON Mode (All Channels On)	EN = high, SCLK = 0 V, CSB1 = CSB2 = VDD = VDDA	IopVDD	–	0.3	0.5	mA
Quiescent Current (VDD) Global Standby Mode (All Channels Off)	CSB1 = CSB2 = VDD = VDDA, f_{SCLK} = 0 Hz −40°C ≤ T_J ≤ 125°C T_J = 150°C	$IstbyV_{DD}125$ $IstbyV_{DD}150$	– –	– –	20 40	μA
Quiescent Current (VDD) Low Iq Mode	EN = 0 V −40°C ≤ T_J ≤ 125°C T_J = 150°C	$IqV_{DD}125$ $IqV_{DD}150$	– –	– –	5 20	μA
Total Quiescent Current VDD + VDDA + OUT_x	T_J = 125°C OUT_x = 18 V EN = SCLK = SI = 0 VDDA = VDD = CSB1 = CSB2 = 5 V	$Iq_{tot}125$	–	–	10	μA
Power−on Reset threshold (VDDA)	VDDA rising VDD = 3 V	V_{DDApor}	–	3.8	4.5	V
Power−on Reset Hysteresis (VDDA)		V_{DDAhys}	–	250	–	mV
Power−on Reset threshold (VDD)	VDD rising	V_{DDpor}	–	2.4	2.7	V
Power−on Reset Hysteresis (VDD)		V_{DDhys}	–	165	–	mV
Thermal Shutdown (Note 4)	Not ATE tested.	T_{sd}	150	175	200	°C
Thermal Hysteresis	Not ATE tested.	T_{sHy}	10	25	–	°C
OUTPUT DRIVER						
Output Transistor $R_{DS(on)}$	IOUTx = 180 mA	$R_{DS(on)LS}$	–	1.3	2.5	Ω
Overload Detection Current		I_{sd}	0.6	0.95	1.3	A
Output Leakage	OUTx = 13.5 V, 25°C OUTx = 13.5 V	$I_{snkLkg25}$ I_{snkLkg}	– –	– –	1 5	μA
Output Clamp Voltage	VDD = 0 V to 5.5 V VDDA = 0 V to 5.5 V IOUTx = 180 mA	V_{clmp}	36	40	44	V
Output Body Diode Voltage	IOUTx = −180 mA	V_{bdFwd}	–	–	1.5	V
Open Load Detection Threshold Voltage		V_{ol}	1.0	1.75	2.5	V
Open Load Diagnostic Sink Current	1 V < OUTx < 13.5 V, Output Disabled	I_{ol}	20	60	100	μA

3. Reduced performance down to 4 V provided VDDA is not in Power−On Reset.
4. Each output driver is protected by its' own individual thermal sensor.
5. Input signals H→L→H greater than 50usec are guaranteed to be detected.

ELECTRICAL CHARACTERISTICS (3.0 V < VDD < VDDA, 4.5 V < VDDA (Note 3) < 5.5 V, −40°C ≤ T_J ≤ 150°C, EN = VDD unless otherwise specified).

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
OUTPUT TIMING SPECIFICATIONS						
Enable (EN) wake−up time	CSB1 = CSB2 = 0 V, VDDA = VDD = 5 V EN going high 80% to SO active	T_{enWk}	–	–	200	μs
Enable (EN) Valid Signal Duration (Note 5)	VDDA = VDD = 5 V	T_{enVld}	50	–	–	μs
Serial Control Output turn−on time All Channels	V_{DS} = 20% V_{bat} ,V_{bat} = 13.5 V, I_{DS} = 180 mA resistive load	T_{outOn}	–	15	50	μs
Serial Control Output turn−off time All Channels	V_{DS} = 80% V_{bat},V_{bat} = 13.5 V, I_{DS} = 180 mA resistive load	T_{outOff}	–	12	50	μs
Over Load Shut−Down Delay Time		T_{isd}	3	15	50	μs
Open Load Detection Time		T_{ol}	30	115	200	μs
DIGITAL INTERFACE CHARACTERISTICS						
Input Characteristics						
Digital Input Threshold (CSB1, CSB2, SI, SCLK, EN)		V_{thIn}	0.8	1.4	2.0	V
Digital Input Hysteresis (CSB1, CSB2, SI, SCLK)		V_{hysIn}	50	175	300	mV
Digital Input Hysteresis (EN)		V_{thENHy}	–	400	800	mV
Input Pulldown Resistance (SI, SCLK, EN)	SI = SCLK = EN = V_{DD}	R_{pdx}	50	120	190	kΩ
Input Pullup Resistance (CSB1, CSB2)	CSB1, CSB2 = 0 V	RpdCSBx	50	120	190	kΩ
CSB1 and CSB2 Leakage to VDD	CSB1 = CSB2 = 5 V, V_{DD} = 0 V	$IlkgCSBV_{DD}$	–	–	100	μA
CSB1 and CSB2 Leakage to VDDA	CSB1 = CSB2 = 5 V, V_{DDA} = 0 V	$IlkgCSBV_{DDA}$	–	–	100	μA
Output Characteristics						
SO − Output High	$I_{(out)}$ = −1.5 mA	V_{soH}	V_{DD} − 0.4	–	–	V
SO − Output Low	$I_{(out)}$ = 2.0 mA	V_{soL}	–	–	0.6	V
SO Tristate Leakage	CSB1 = CSB2 = V_{DD} = 5.5 V	$I_{triStLkg}$	−3	0	3	μA

3. Reduced performance down to 4 V provided VDDA is not in Power−On Reset.
4. Each output driver is protected by its' own individual thermal sensor.
5. Input signals H→L→H greater than 50usec are guaranteed to be detected.

ELECTRICAL CHARACTERISTICS (3.0 V < VDD < VDDA, 4.5 V < VDDA (Note 3) < 5.5 V, −40°C ≤ T_J ≤ 150°C, EN = VDD unless otherwise specified).

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
DIGITAL INTERFACE CHARACTERISTICS						
Timing (all timing specifications measured at 20% and 80% voltage levels)						
SCLK Frequency		F_{clk}	–	–	5	MHz
SCLK Clock Period		Tp_{Clk}	200	–	–	ns
SCLK High Time	Figure 4	TclkH	85	–	–	ns
SCLK Low Time	Figure 4	TclkL	85	–	–	ns
SI Setup Time	Figure 4	TsiSup	50	–	–	ns
SI Hold Time	Figure 4	TsiHld	50	–	–	ns
CSB1, CSB2 Setup Time	Figure 4	TcsbxSup	100	–	–	ns
CSB1, CSB2 High Time (Note 6)	Figure 4	TcsbH	1.5	–	–	μs
SCLK Setup Time	Figure 4	TclkSup	85	–	–	ns
SO Output Enable Time (CSB1, CSB2 falling to SO valid)	Figure 4, C_{load} = 50 pF VDDA = VDD = 5 V	TenSO	–	–	200	ns
SO Output Disable Time (CSB1, CSB2 rising to SO tri−state)	Figure 4 VDDA = VDD = 5 V	T_{disSO}	–	–	200	ns
SO Output Data Valid Time with capacitive load	Figure 4, C_{load} = 50 pF VDDA = VDD = 5 V	T_{soV}	–	–	100	ns

6. Time between the trailing CSB_x signal going high to complete a SPI cycle to the leading CSB_x signal going low to start a new SPI cycle.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

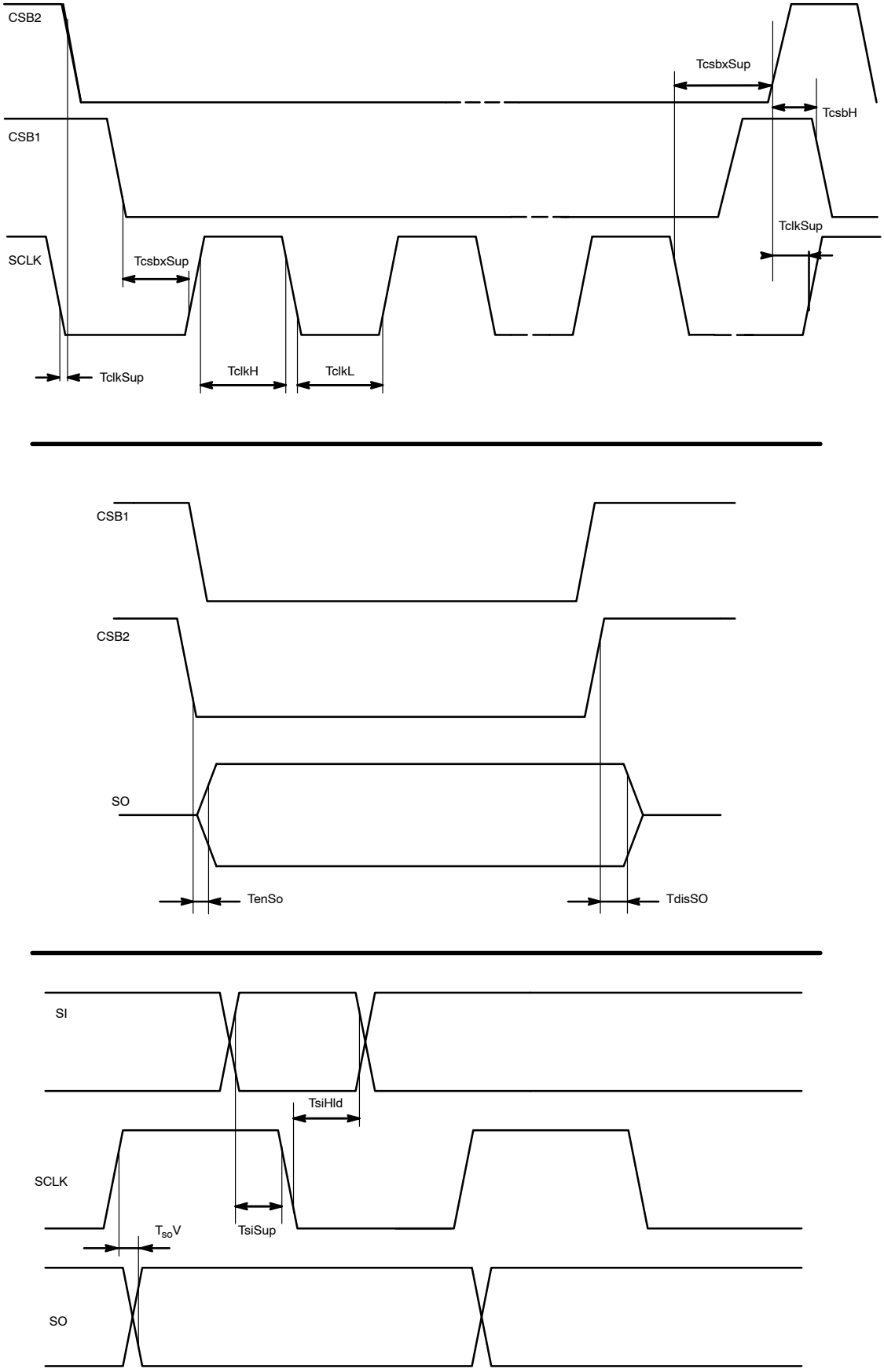


Figure 4. Detailed SPI Timing (measured at 20% and 80% voltage levels)

TYPICAL PERFORMANCE GRAPHS

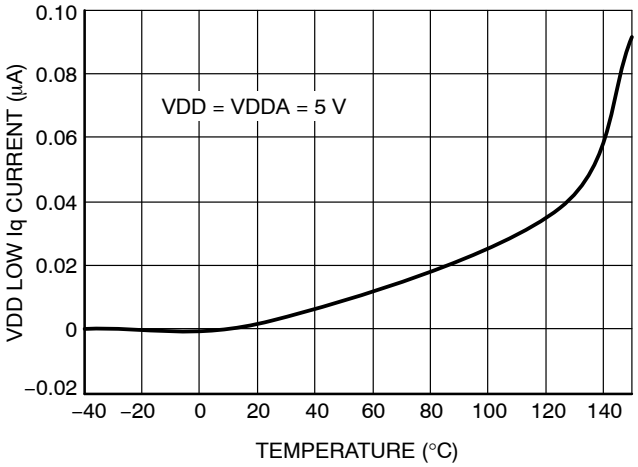


Figure 5. VDD Low Iq Current vs. Temperature

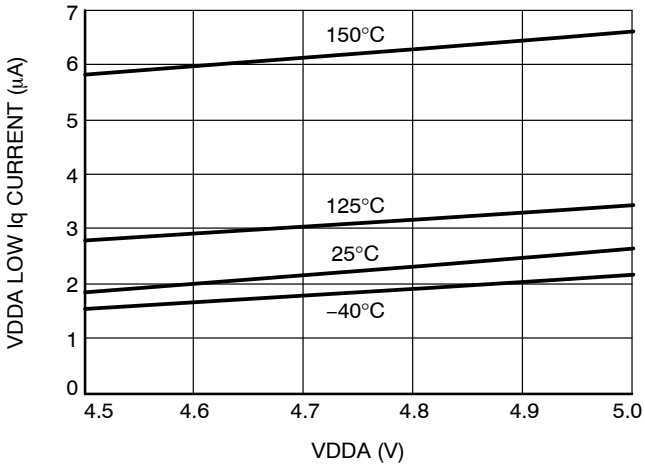


Figure 6. VDDA Low Iq Current vs. VDDA

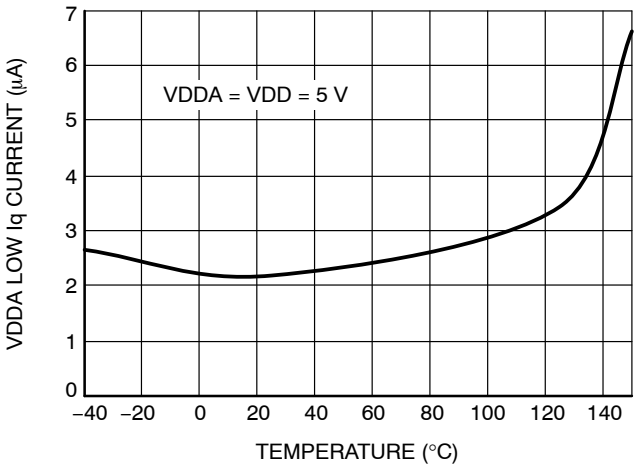


Figure 7. VDDA Low Iq Current vs. Temperature

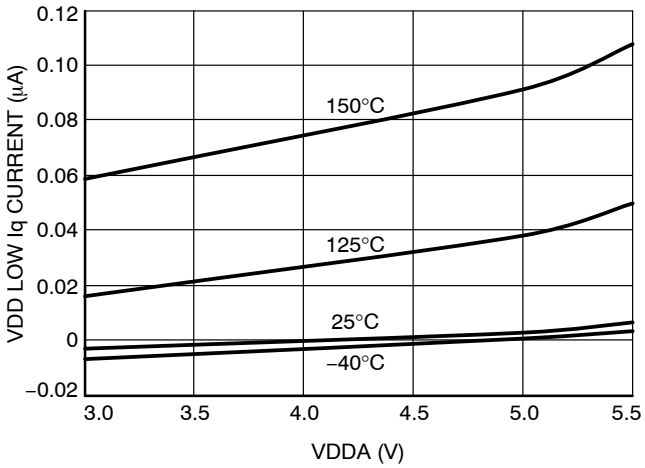


Figure 8. VDD Low Iq Quiescent Current vs.VDD

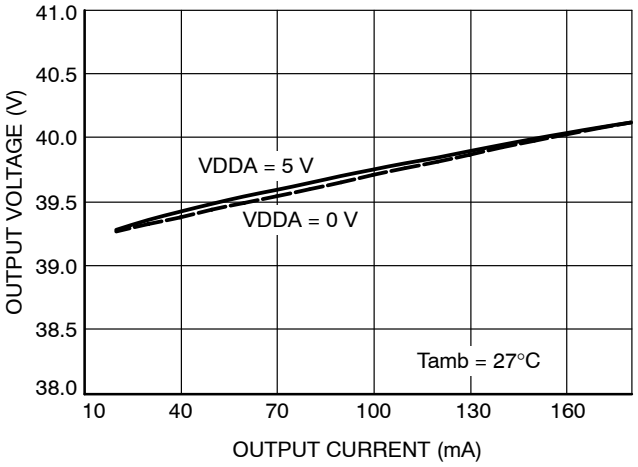


Figure 9. Output Clamping Voltage vs. Current

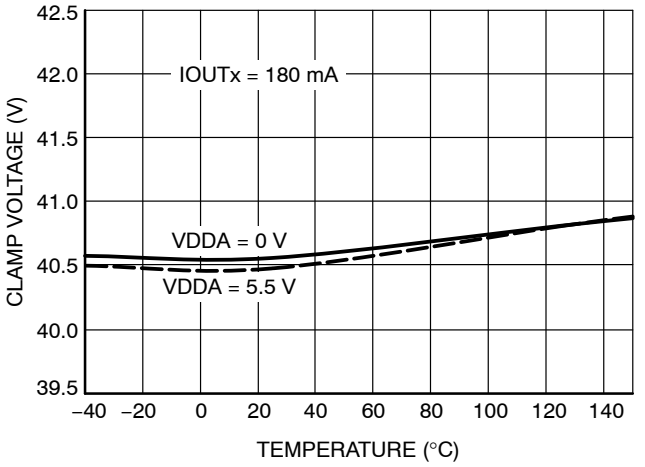


Figure 10. Output Clamping Voltage vs. Temperature

TYPICAL PERFORMANCE GRAPHS

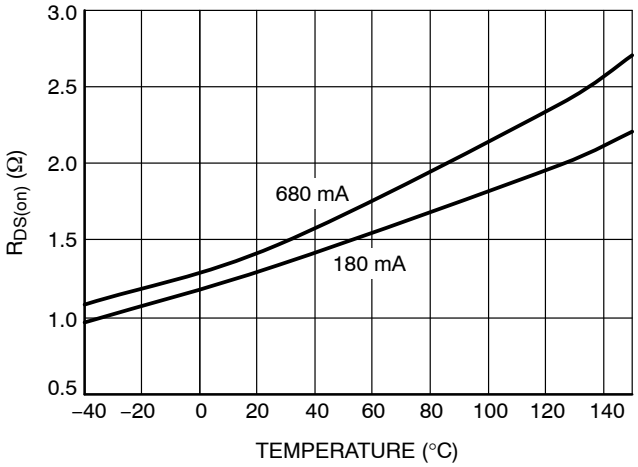


Figure 11. $R_{DS(on)}$ vs. Temperature

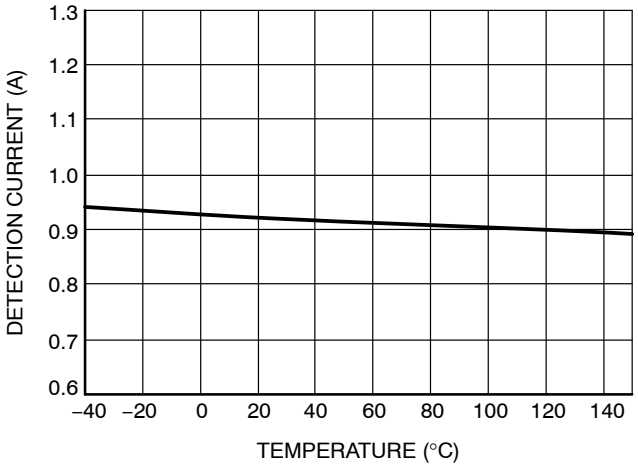


Figure 12. Over Load Current vs. Temperature

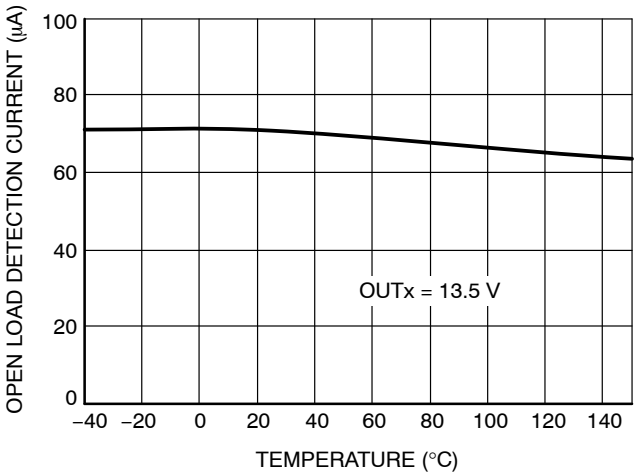


Figure 13. Open Load Detect Current vs. Temperature

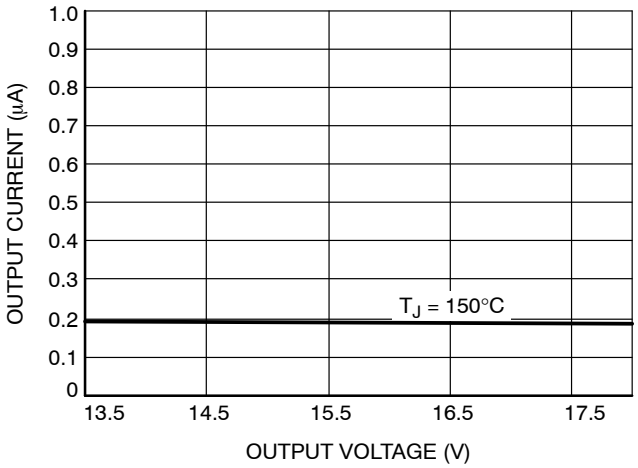


Figure 14. Output Leakage vs. Voltage

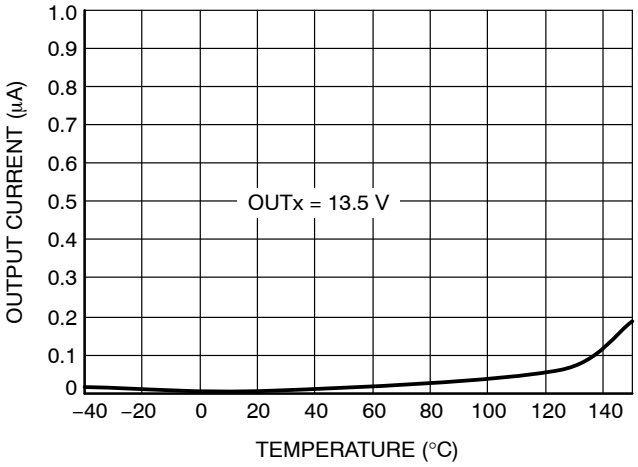


Figure 15. Output Leakage Current vs. Temperature

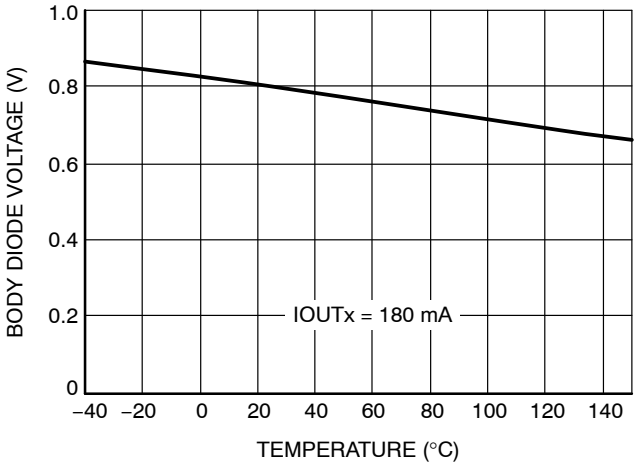


Figure 16. Output Body Diode Voltage vs. Temperature

TYPICAL PERFORMANCE GRAPHS

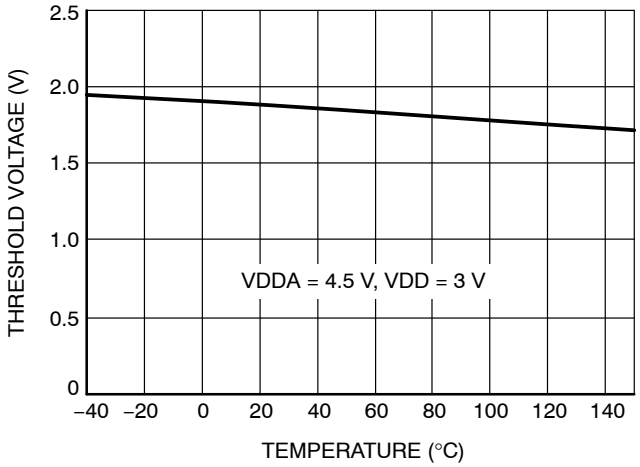


Figure 17. Open Load Detection Voltage vs. Temperature

GENERAL OVERVIEW

The NCV7751 provides 12 independent 600 mA power transistors with their source connection referenced to the ground pin and with their drain connection brought out to individual pins resulting in 12 independent low−side drivers.

Internal clamping structures are provided to limit transient voltages when switching inductive loads. Each output has an over load detection current of 0.6 A (min) where the driver will turn−off and stay latched off.

The NCV7751 has a dedicated Enable pin for low quiescent mode operation. The different modes of operation are summarized in Table 1, where the behavior of each mode is a result of a programmed state via SPI, of an externally triggered event (EN) or of the power supply requirements.

Table 1. MODES OF OPERATION

Modes of Operation	Conditions	Description
UVLO Mode	VDD or VDDA below their respective POR thresholds	All outputs off in this mode. Coming out of this mode with EN = 1 sets all channels in the OFF mode without open circuit diagnostic current enabled.
Low Iq Mode	EN = low	Provides a state with the lowest quiescent current for VDD and VDDA.
OFF Mode	SPI Control (Command 11)	Output off. Open circuit diagnosis current is disabled (powerup mode). Open circuit diagnosis current is enabled (normal mode).
Global OFF Mode	SPI Control All Channels (Command 11)	Output off. Open circuit diagnosis current is disabled (powerup mode). Open circuit diagnosis current is enabled (normal mode).
ON Mode	SPI Control (Command 10)	Output on.
Standby Mode	SPI Control (Command 00)	Provides an OFF state with Open circuit diagnosis current disabled. All latched faults are cleared when Command 00 is sent.
Global Standby Mode	SPI Control All Channels (Command 00)	Provides a reduced quiescent current mode. Provides an OFF state with Open Load diagnostic current disabled.

The NCV7751 is available in a SSOP−24 EPAD package.

Power up, Power−On Reset (UVLO mode)

Both VDD and VDDA supply an independent power−on−reset function to the IC. Coming out of power−on−reset, all input bits are set to a 1 (OFF Mode) and all output bits are set to a 0 except for the TER bit which is set to a 1. The device cannot operate unless both supplies are above their respective power−on reset thresholds. A breach of VDD or VDDA Power−On Reset thresholds will cause the outputs to turn off and enter the UVLO mode.

The NCV7751 powers up into the Global OFF Mode without the open circuit diagnostic current enabled and all the faults registers cleared. In some application the diagnostic current may be sufficient enough to produce a noticeable illumination of the LED loads. The NCV7751 power−up behavior avoids unintentional illumination of the LED loads when entering into Global Off Mode after recovering from a POR condition. All other paths to Global OFF Mode enable open circuit diagnostic current.

Enable Input (EN)

An Enable function (EN) provides a low quiescent sleep current mode when the device is not being utilized. No data is stored when the device is in sleep mode. An internal pull down resistor is provided on the EN input to ensure the device is off if the input signal is lost. Programming the EN signal to a low state clears all the registers and resets the driver. The EN input pin is a logic controlled input with a voltage threshold defined by the VthIn parameter. When the EN signal is asserted the IC will proceed with the VDDA POR cycle and brings the drivers will enter into normal operation (Global OFF Mode).

Serial Peripheral Interface (SPI) Communication

Serial Peripheral Interface (SPI) is used to establish a communication medium between the master device and the NCV7751. The SPI input data is stored in the input registers and the diagnostic data that the slave device transmits to the master is stored in the output registers. The input register translates the SPI input to driver control logic consequently controlling the gate of the LS drivers and the output register transmits the output fault bits and the frame detection integrity. The input data registers are 32 bits wide and the output data registers are 33 bits wide and are defined here forth:

1. Input Register: Input for IC mode state and output driver state control.
2. Output Register: Provides diagnostic information on the output driver condition and transmission error condition of the previous SPI cycle.

Given the size of the data registers, a decoded SPI interface is utilized to access the two data registers in the NCV7751. The decoded SPI interface offers the flexibility of accessing either the entire data registers (input and output registers) at once or just partially programming the data registers with a 16−bit or 24−bit frame. The input and output registers are divided into ports and sub−ports for the ease of explaining the decoded SPI structure and the implementation of the diagnostic data shifted out to the SO pin. Partitioning of the data registers are shown in Figure 18.

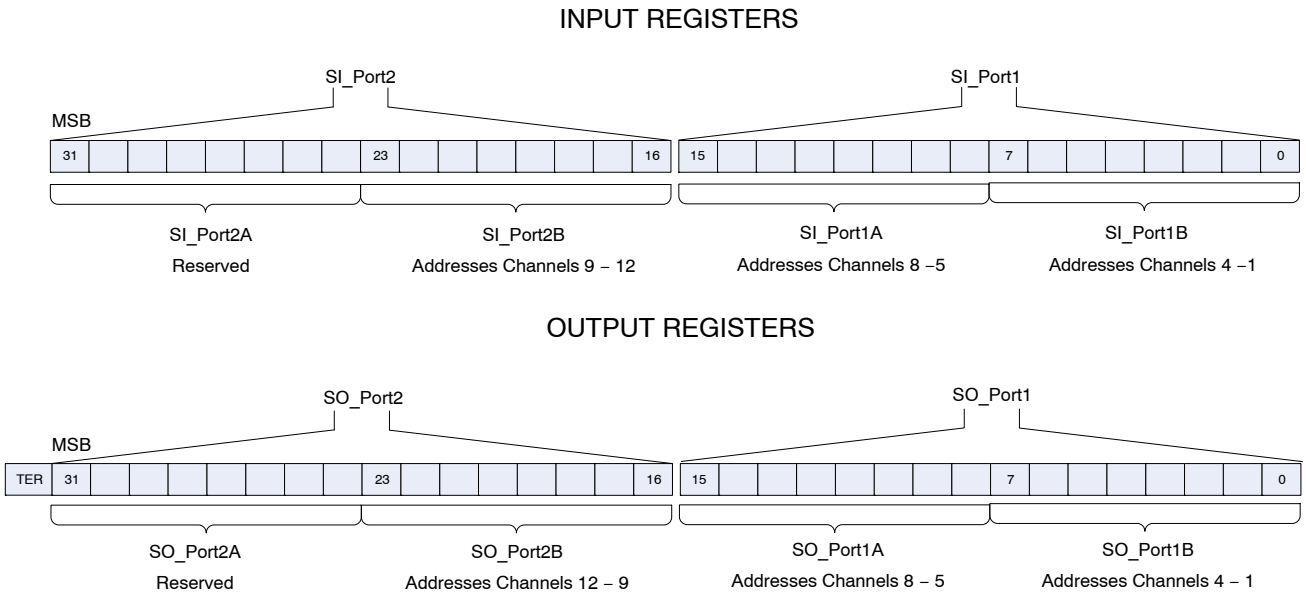


Figure 18. Input and Output Register Port Assignment

The partitioned register data can be programmed or accessed through five different decoded scheme and they are defined in Table 2. The decoding scheme is comprised of two chip select signals generated from the input pins, CSB1 and CSB2 and an internally generated bit “FLEN”. Using two CSB pins allow the conventional 16−bit SPI frame to be expanded to a 24−bit or 32−bit frame and still maintain uniformity with the 16−bit legacy devices such as the NCV7240.

Table 2. SPI DECODING

SPI Mode Name	Decoding Selection Signals			Input Bit Requirement	Input Register Functionality	Output Register Functionality
	FLEN (Note 7)	CSB2	CSB1			
CSB_00	x	0	0	32 Bits	Programs SI_Port2 and SI_Port1	Reads SO_Port2 and SO_Port1
CSB_01_T	0	0	1	16 Bits	Programs SI_Port2	Reads SO_Port2B and SO_Port1A
CSB_01_E	1	0	1	24 Bits	Programs SI_Port2B and SI_Port1	Reads SO_Port2B and SO_Port1
CSB_10	x	1	0	16 Bits	Programs SI_Port1	SO_Port1
CSB_11	x	1	1	SPI Inactive		

7. FLEN: Auto Frame Detection Scheme on CSB2
16−bit frame on CSB2: Truncated SPI Frame → FLEN = ‘0’
24−bit frame on CSB2: Extended SPI Frame → FLEN = ‘1’

A visual representation of the decoded SPI scheme is demonstrated in Figure 19.

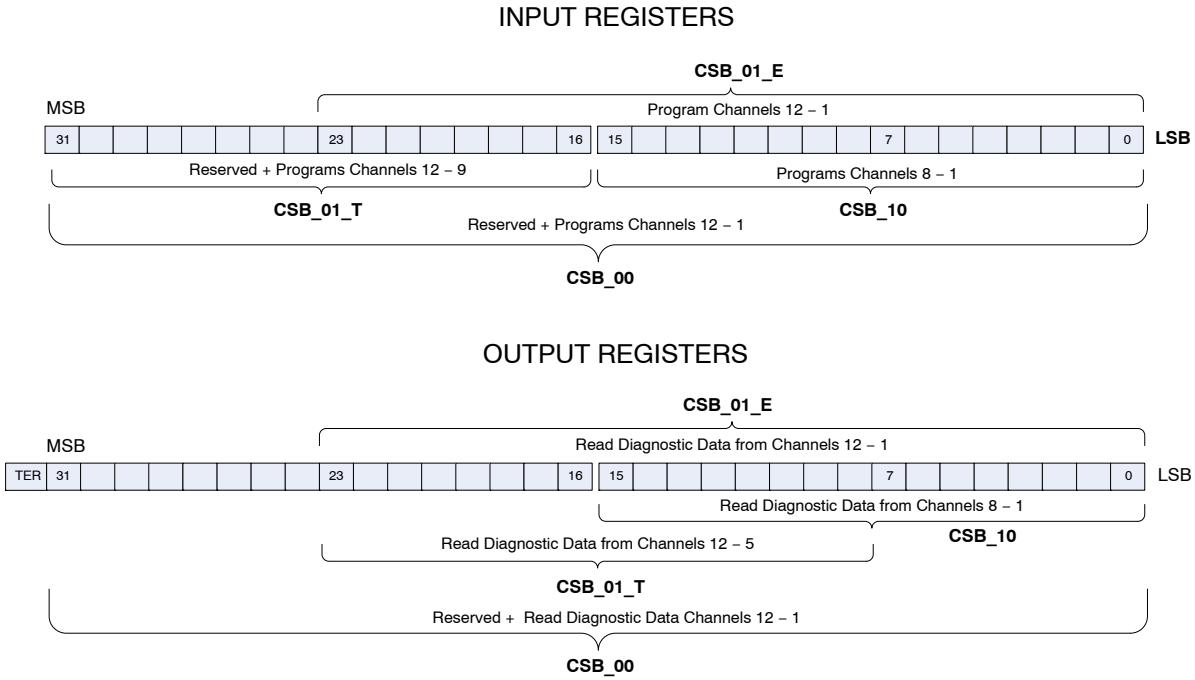


Figure 19. SPI Decoding Structure and Register Configuration Scheme

16−Bit SPI Control: CSB_10 and CSB_01_T

SI_Port1 and SO_Port1 governed by CSB_10 mode are identical to the NCV7240 devices, which supports channels 1−8 operation modes and diagnostics. Thus when CSB1 is pulled low, the SPI data is multiplexed to SI_Port1 and the data shifted out are of SO_Port1. CSB2 appends the SPI operation for channels 9 − 12 by storing the driver control and diagnostic data to data registers 23 down to 8. Bringing CSB2 low while keeping CSB1 high allows data transfer to SI_Port2 and the data retrieved on the SO pin is of SO_Port2B and SO_Port1A when a 16−bit frame is generated from the master (CSB_01_T).

24−Bit SPI Control: CSB_01_E

The auto−frame configuration of CSB2 offers control and diagnostic of all the output drivers through a single CSB2 cycle when a 24−bit frame is transmitted from the master (CSB_01_E). The auto−frame configuration on CSB2 is realized by an internal storage bit “FLEN”, where the bit is set when a modulo 16 bit counter extends to a modulo 24−bit count. The SPI modes represented by the status of the “FLEN” bit are displayed in Table 2.

32−Bit SPI Control: CSB_00

If both CSB1 and CSB2 signals (CSB_00) are pulled low, Port1’s input and output registers are serially connected to Port2’s input and output registers respectively; effectively making a single 32−bit SPI interface.

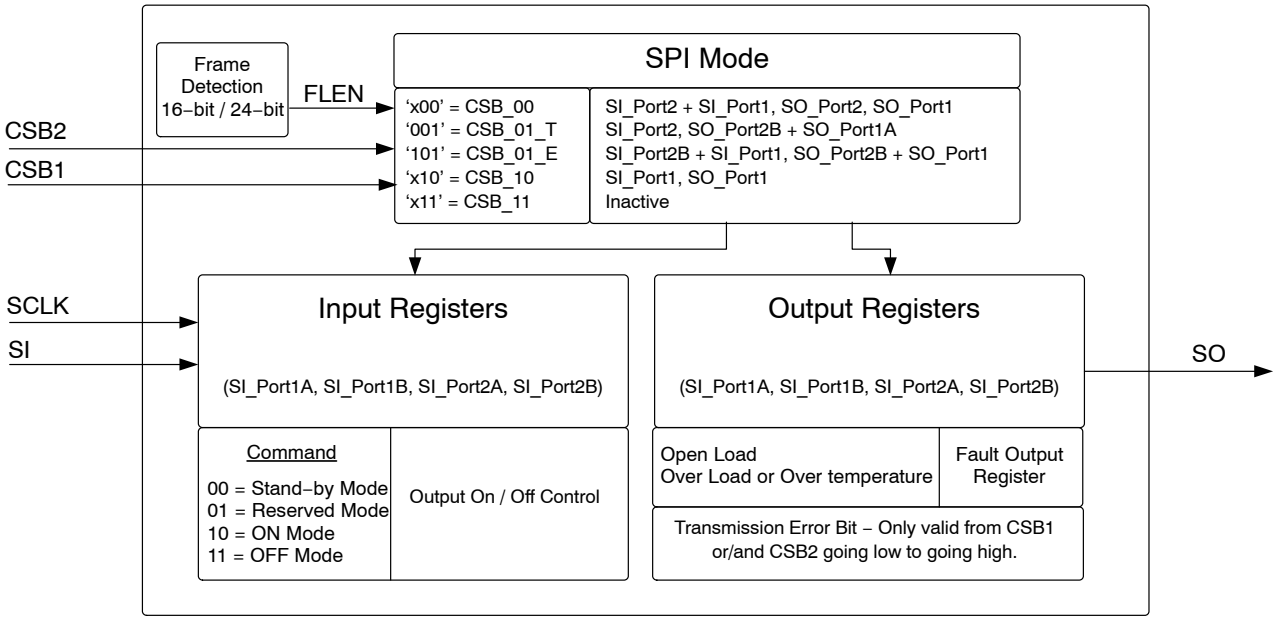


Figure 20. Detailed SPI Register Overview

SPI Frame Overview

Depending on the SPI port configuration, words generated from the masters should be composed of 16, 24 or 32 bits MSB (most significant bit) transmitted first. Figure 21 shows the two 16−bit frames for the SPI interface configured as dual ports with the global TER bit and Figure 22 illustrates a single frame consists of two words and the TER bit.

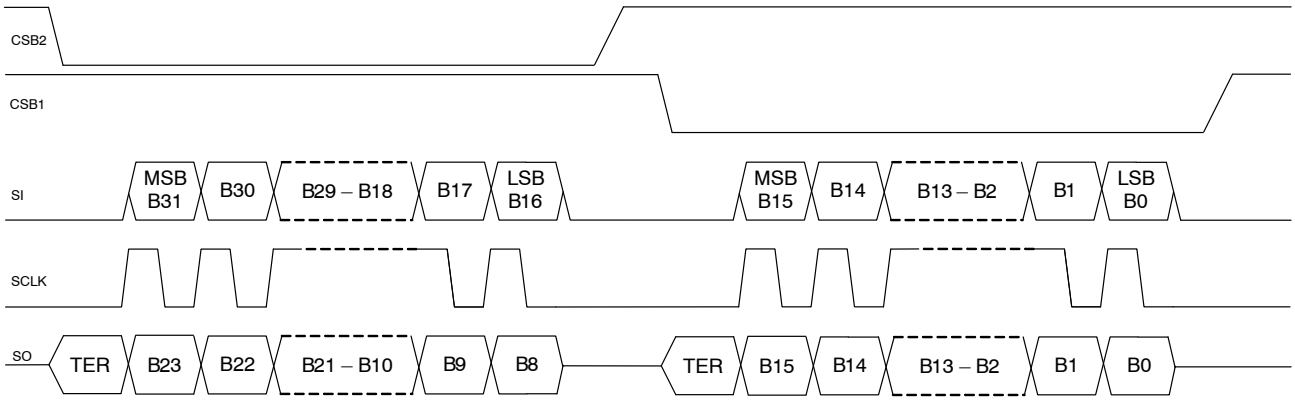


Figure 21. SPI Interface Configured for SPI Mode: CSB_01_T then CSB_10

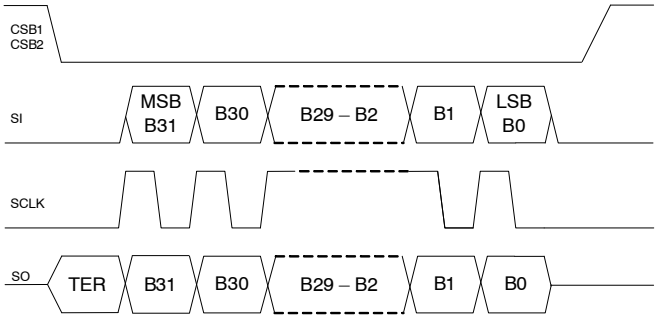


Figure 22. SPI Interface Configured as SPI Mode: CSB_00

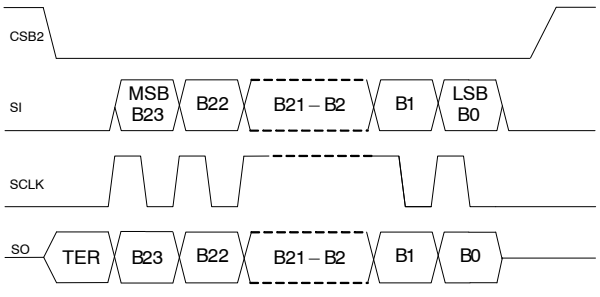


Figure 23. SPI Interface Configured SPI Mode: CSB_01_E

Figure 23 shows the 24−bit format for maximum transmission efficiency when controlling 12 channels.

The following constraints must be met to assure proper SPI communication:

1. CSB1 and/or CSB2 transition to the desired decoded state to initiate SPI communication.
2. SCLK should be in a low state before CSB1 and/or CSB2 transition from high to low.
3. CSB setup time (TcsbxSup) must be met from the trailing CSBx signal to the first rising edge of SCLK to allow decoding of the CSB signals.
4. Once the NCV7751 is decoded to the programmed SPI mode, either zero SCLK pulse or the minimum bit requirement must be met before any transition of CSB1 and/or CSB2 signals to avoid a transmission error (TER).
5. The MSB (most significant bit) is the first transmitted bit.
6. Data is sampled from SI on the falling edge of SCLK
7. Data is shifted out from SO on the rising edge of SCLK
8. Once the required number of bits is shifted in, the SCLK should idle low for a minimum of TcsbxSup period before bring the CSB1 and/or CSB2 signals high to complete the SPI cycle.

SI SPI Input Data (Serial structure of input word)

The data shifted into the input data registers are decoded into instructions for each channel per the table below. Standby Mode, ON Mode, and OFF Mode are all selectable via the SPI for each channel independently.

The CSB mode required to access the different registers are also provided in Table 3.

After a power−on reset, all register bits are set to a 1.

Table 3. SPI INPUT DATA

Reserved	Channel 12		Channel 11		Channel 10		Channel 9		Channel 8		Channel 7		Channel 6		Channel 5		Channel 4		Channel 3		Channel 2		Channel 1	
31–24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB – B31									SI_Port2 + SI_Port1 – CSB_00															LSB – B0
	MSB – B23								SI_Port2B + SI_Port1 – CSB_01_E															LSB – B0
MSB–B31 SI_Port2–CSB_01_T LSB–B16																								
									MSB – B15		SI_Port1 – CSB_10													LSB – B0

		Input Data Register	
Field	**Bits**	**Description**	
Reserved	31–24	Reserved	
channel x (x=1–12)	23,22 21,20 19,18 17,16 15,14 13,12 11,10 9, 8 7,6 5,4 3,2 1,0	Command	
		00	Channel Stand–by Mode Fast channel turn off Fault Registers reset
			Diagnostic Current: Disabled
		01	Reserved Mode Channel turned off.
			Diagnostic Current: Enabled (Disabled after POR) (Note 8)
		10	ON Mode Channel turned on.
			Diagnostic Current: Disabled
		11	OFF Mode Channel turned off.
			Diagnostic Current: Enabled (Disabled after POR) (Note 8)

8. For Proper LED Operation

SO Fault Diagnostic Retrieval (16 bit serial structure of output word)

The decoded CSB mode and the frame length dictate the output fault diagnostics appeared on the SO pin. Only output fault diagnostics and frame detection errors are available through the serial output (SO). The response frame (SO) provides channel−specific (2 bits / channel) status information fault reporting.

Table 4. SO DIAGNOSTIC DATA

CSB Mode	Bit Requirement	SO Reporting
CSB_00	32	Diagnostic data from output registers 31 − 0
CSB_01_E	24	Diagnostic data from output registers 23 − 0
CSB_01_T	16	Diagnostic data from output registers 23 − 8
CSB_10	16	Diagnostic data from output registers 15 − 0
CSB_11	−	Tristate

TER*	Reserved	TER*	Channel 12		Channel 11		Channel 10		Channel 9		TER*	Channel 8		Channel 7		Channel 6		Channel 5		Channel 4		Channel 3		Channel 2		Channel 1	
			23	22	21	20	19	18	17	16		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

P31	31−24	P23	23	22	21	20	19	18	17	16	P15	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB − B31																											LSB − B0
		MSB − B23																									LSB − B0
		MSB − B23																		LSB − B8							
											MSB − B15																LSB − B0

Fault Diagnostic Register

Field	Bits	Description
TER	CSB1 or CSB2 high−to−low	Transmission Error.
		0 Successful transmission in previous communication.
		1 Frame detection error in previous transmission or exiting UVLO Mode.
OIn (n = 1−12)	1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23	Open Load
		0 Normal Operation
		1 Fault detected
Dn (n = 1−12)	0, 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22	Over Load or Over Temperature
		0 Normal Operation
		1 Fault detected

*TER Bit is available only when either or both CSB signals goes low and before the first SCLK rising edge

Frame Detection

The NCV7751 detects the number of bits transmitted after either CSB1 or CSB2 goes low. The device have minimum bit requirement for the internal counter to insure that proper number of bits are clocked in during the SPI cycle. After the minimum bit count has been met, any multiple of 8−bits are allowed (*minimum bit count* + *8 * n*). When the SPI ports are configured separately, a minimum of 16 bits are needed to avoid a frame error. Similarly, a minimum of 32 bits are required when the SPI is configured as a single port by using both CSB1 and CSB2 pins (CSB_00).

For data transferred via CSB2, 16−bits are acceptable, but a total of 24−bits of data are required to fill the input registers. Thus, it is crucial that if daisy chaining via CSB2 only, 24−bits of data must be allocated for NCV7751.

The frame counter is enabled when either of the CSB signals goes low and at the rising edge of the SCLK. By default the frame detection counter is set to expire when it exceeds 16 for the initial 16 clock cycles for CSB1 and CSB2 and then a modulo eight counter is utilized. If both CSB1 and CSB2 are low the counter immediately extends the count to 32. Once the counter is extended to 32, it can only be disabled once both CSB pulses are set high again.

Given that the bits clocked in didn't violate the internal frame detection counter, the data is latched into the input register.

Transmission Error Reporting (TER)

Reporting of the TER bit in SO is treated as a global fault, so any transmission error on either port or frame count is reflected on the next CSB1 or CSB2 cycle. The TER is cleared by sending a valid SPI command.

The transmission error information is available on SO after either of the CSB signals goes low until the first rising SCLK edge.

In addition to unqualified bit counts setting TER = 1, the bit will also be set by

1. Coming out of UVLO.
2. Transitioning from Low Iq Mode to Global Off Mode.

The TER bit is multiplexed with the SPI SO data and OR'd with the SI input (Figure 24) to allow for reporting in a serial daisy chain configuration. A TER error bit as a "1" automatically propagates through the serial daisy chain circuitry from the SO output of one device to the SI input of the next. This is shown in Figures 25 and 26 first as the daisy chained devices connected with no Transmission Error (Figure 25) and subsequently with a Transmission Error in device 1 propagating through to device 2 (Figure 26).

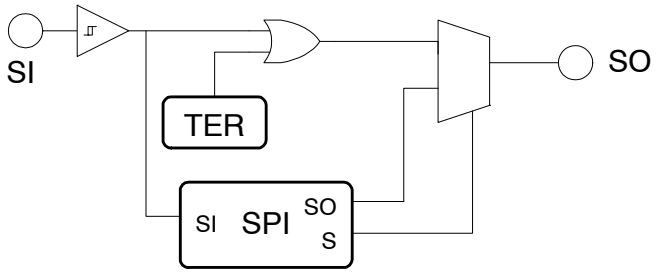


Figure 24. TER SPI Link

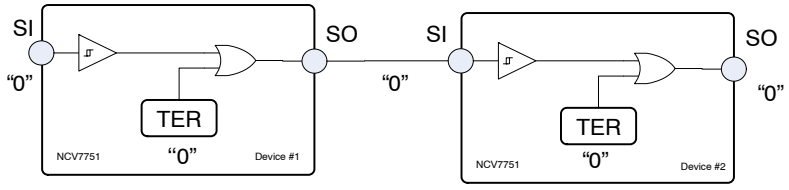


Figure 25. TER (no error)

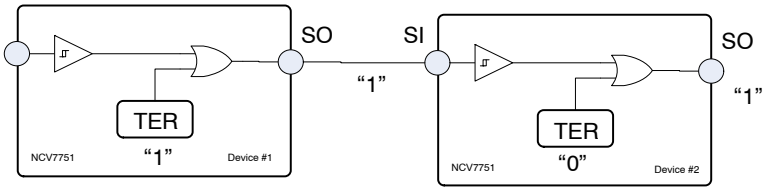


Figure 26. TER Error Propagation

Note − TER is valid from CSB1 and/or CSB2 going low until the 1st low−to−high transition of SCLK to allow for propagation of the SI signal (Reference Figures 21, 22 and 23).

TER Information Retrieval

TER information retrieval is as simple as bringing either CSB1 or CSB2 high−to−low. No clock signals are required.

Daisy Chain Setup

Daisy chain setups are possible with the NCV7751. The serial setup shown in Figure 27 highlight two daisy chaining configuration with the NCV7751:

1. Either tying (switch closed in Figure 27) or stimulating the CSB1 and CSB2 signals together
2. With only CSB2 pin (switch open in Figure 27)

With these two different configurations, the number of bits dedicated for NCV7751 is 24−bits and 32−bits for option 1 and 2 respectively. Any other 16 bit device on the chain is required to be using a similar SPI protocol. Particular attention should be focused on the fact that the initial data that are shifted out of the device are the diagnostic information. The master must generate enough input bits to propagate all the diagnostic bits from the slave devices in the serial chain to the master's MISO registers. The timing diagram shows a typical transfer of data from the microprocessor to the SPI connected IC's.

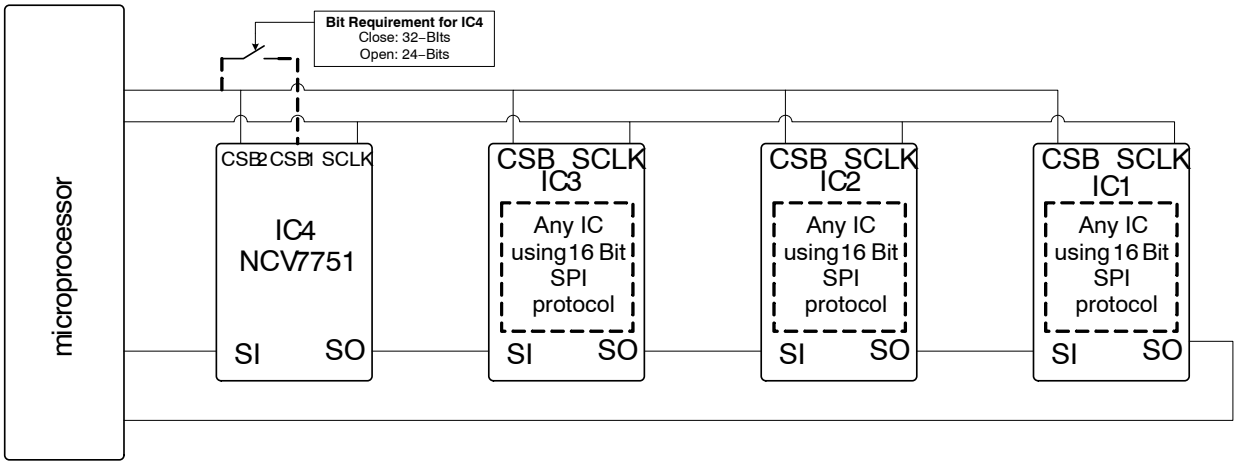


Figure 27. Serial Daisy Chain

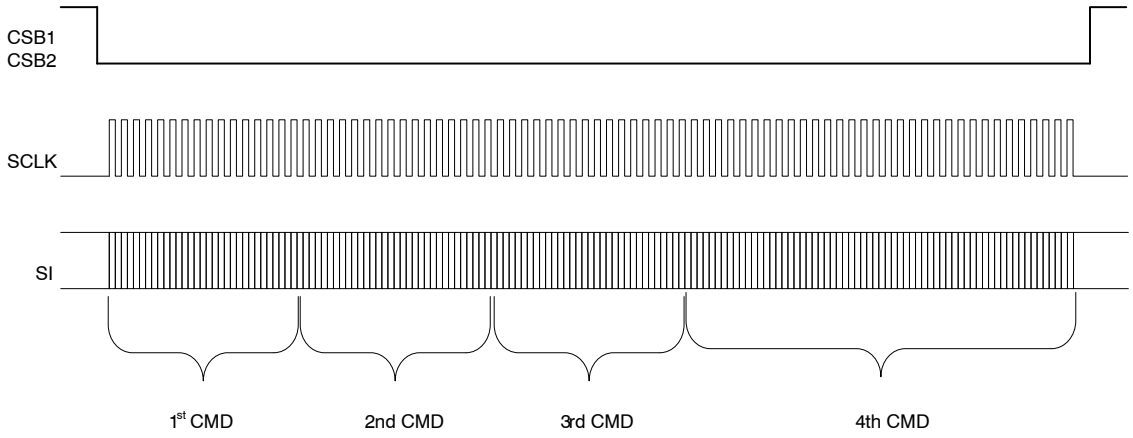


Figure 28. Serial Daisy Chain Timing Diagram with CSB1 tied to CSB2 (Switch Closed)

Table 5. SERIAL DAISY CHAIN DATA PATTERN FOR CSB1 TIED TO CSB2 CONFIGURATION (SWITCH CLOSED)

	CLK = 16 bits	CLK = 32 bits	CLK = 48 bits	CLK = 64 bits	CLK = 80 bits
IC4	1st CMD	2nd CMD	3rd CMD	First Half of 4th CMD	Second Half of 4th CMD
IC3	IC4 DIAG SO_Port2	IC4 DIAG SO_Port1	1st CMD	2nd CMD	3rd CMD
IC2	IC3 DIAG	IC4 DIAG SO_Port2	IC4 DIAG SO_Port1	1st CMD	2nd CMD
IC1	IC2 DIAG	IC3 DIAG	IC4 DIAG SO_Port2	IC4 DIAG SO_Port1	1st CMD
micro	IC1 DIAG	IC2 DIAG	IC3 DIAG	IC4 DIAG SO_Port2	IC4 DIAG SO_Port1

Table 5 refers to the progression of data over time of the Serial Daisy Chain setup of Figure 27 with the switch closed as word bits are shifted through the system. 80 bits are needed for complete transport of data in the example system. Each column of the table displays the status after transmittal of each word (in 16 bit increments) and the location of each word packet along the way.

The NCV7751 is also compatible with 8 bits devices due to the features of the frame detection circuitry. The internal bit counter of the NCV7751 starts counting clock pulses when either or both CSB signals go low. After the minimum bit requirement is met for the NCV7751, the subsequent words can be comprised of just 8−bits.

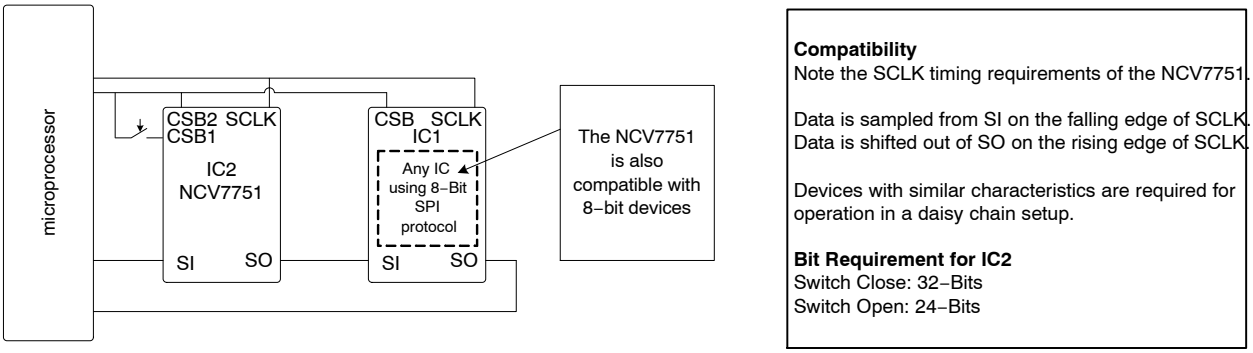


Figure 29. Daisy Chaining with 8−bit Devices

Output Drive Clamping

Internal zener diodes (Z1 and Z2, Figure 30) help to protect the output drive transistors from the expected fly back energy generated from an inductive load turning off. Z1 provides the voltage setting of the clamp (along with Vgs of the output transistor and Z2) while Z2 isolates Z1 from normal turn−on activity.

The output clamp voltage is specified between 36 V and 44 V. This includes clamping operation during un−powered input supplies (VDD and VDDA). Device protection will be provided when the load is driven from an alternative driver source. This is an important feature when considering protecting for load dump with an un−powered IC.

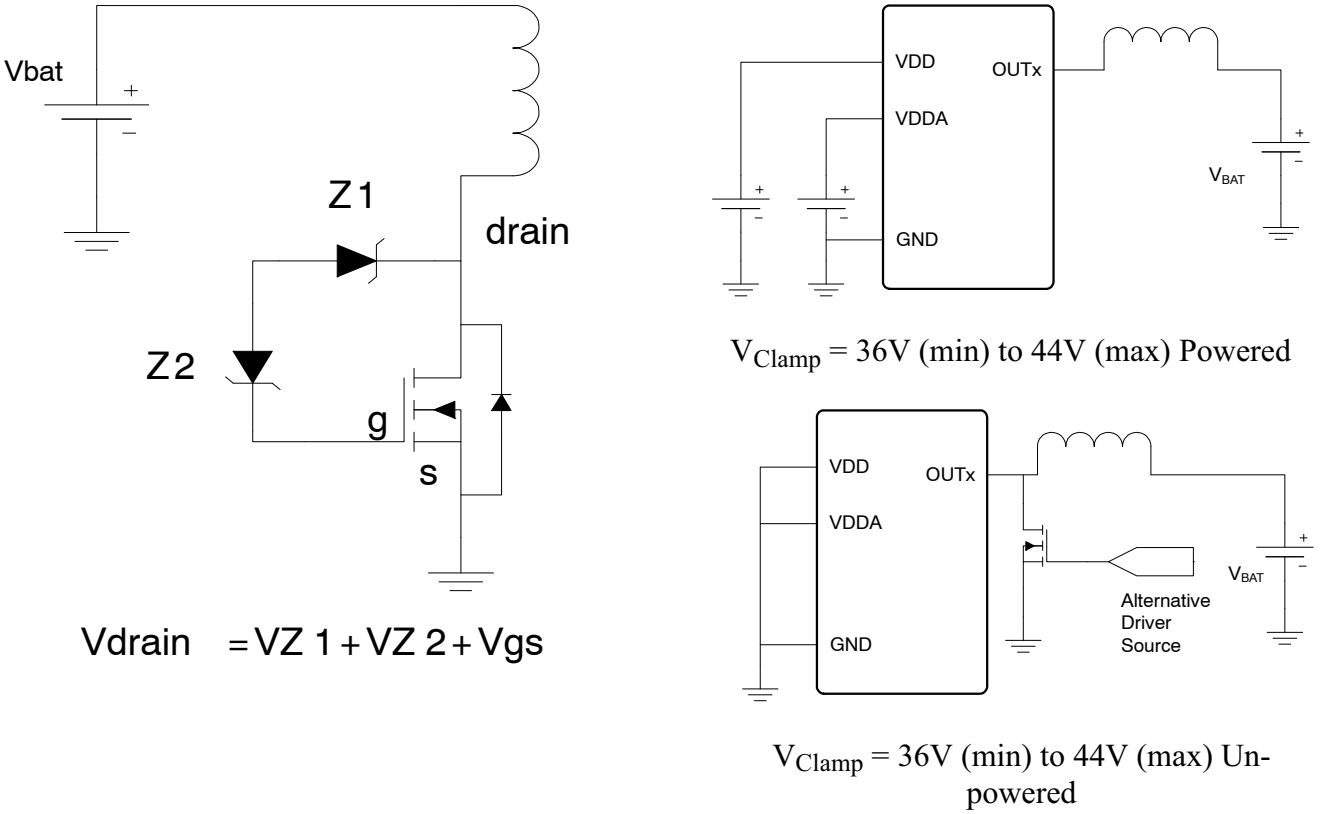


Figure 30. Output Clamp

Over Temperature / Thermal Shutdown

The NCV7751 incorporates 12 individual thermal sensors located in proximity to each output driver. A channel is latched off upon the detection of an Over Temperature event. This allows operation of unaffected channels before, during, and after a channel detection of over temperature. The thermal shutdown detection threshold is typically 175°C with 25° of hysteresis.

Open Load Detection

Open Load Detection is achieved for each output with the Open Load Detection Threshold Voltage reference voltage (Vol) and its' corresponding Open Load Diagnostic Sink Current (when the output driver (OUTx) is off). The output driver maintains its' functionality with and without the open bit set (i.e. it can turn on and off).

During normal operation, the open circuit impedance (Roc) is zero ohms. This sets the voltage on OUTx to VS volts. As long as VS is above Vol no open circuit fault will be recognized. The voltage appearing on OUTx is a result of VS and the voltage drop across Roc realized by the current flow created by Iol.

The NCV7751 voltage level trip points are referenced to ground. The threshold range is between 1.0 V and 2.5 V.

With a nominal battery voltage (VS) of 14 V, the resultant worst case thresholds of detection are as follows.

$$\frac{(VS - OpenLOadDetectionThresholdvoltage)}{OpenLoadDiagnosticSinkCurrent} = OpenLoadImpedance$$

$$\frac{(14 - 2.5\ V)}{100\ \mu A} = 115\ k\Omega \qquad \frac{(14\ V - 1.0\ V)}{20\ \mu A} = 650\ k\Omega$$

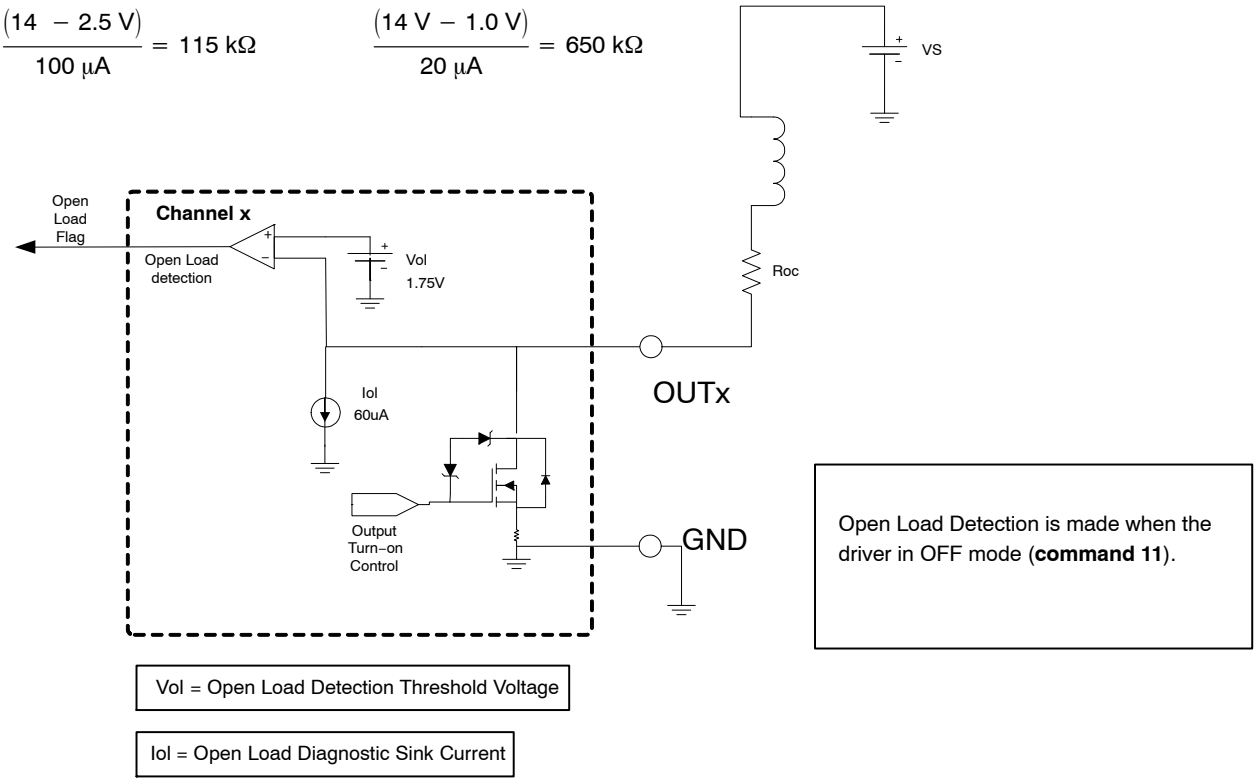


Figure 31. Open Load Detection

LED Loads

The NCV7751 features a power up feature for the Global OFF Mode enabling the part to power up in a mode without the open load diagnostic current enabled. This averts any unintended illumination of LED loads during power up.

Over Current Protection

An Over Load Current Shut−Down Delay Time of 3 μs (min) is designed into the IC as a filter allowing for spikes in current which may occur during normal operation and allowing for protection from overload conditions.

Fault Handling

Registers are reset with the following conditions.

1. Channel in Standby Mode.
2. Power−on reset of VDD.
3. Power−on reset of VDDA.
4. EN low.

Table 6. FAULT SUMMARY

Output Fault Condition	Fault Memory	Miscellaneous
Open Load	Latched	Detected in Driver Off State (1.75 V (typ) threshold) when detection is enabled. Reported in Output Fault Diagnostics Register until cleared via the SPI port. Output will maintain turn−on capability. Over Load or Over Temperature Faults will be prioritized.
Short to Ground	Latched	Detection as part of the Open Load circuitry described above.
Short to Vbat	N/A	Protected via Over Load and Over Temperature functions.
Over Load	Latched	Detected in Driver On State 0.6 A (min), 1.3 (max) A latched off condition must be cleared via the SPI port before it can be turned on.
Over Temperature	Latched	Detection in IC On State (T_J = 175°C (typ)) A latched off condition must be cleared via the SPI port before it can be turned on.

SCALE 1:1

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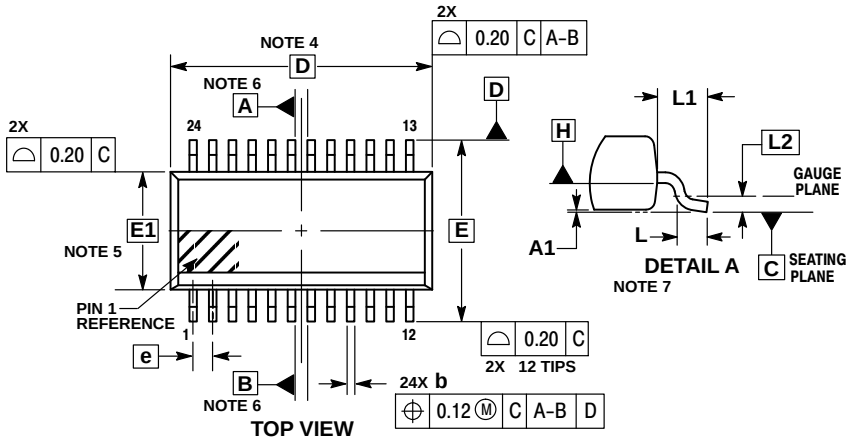
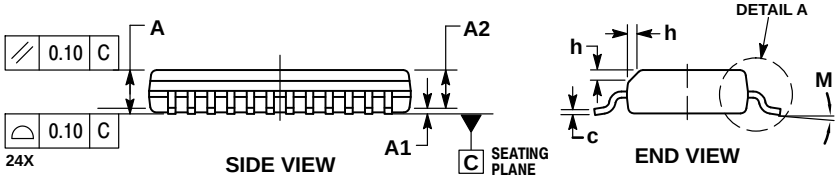
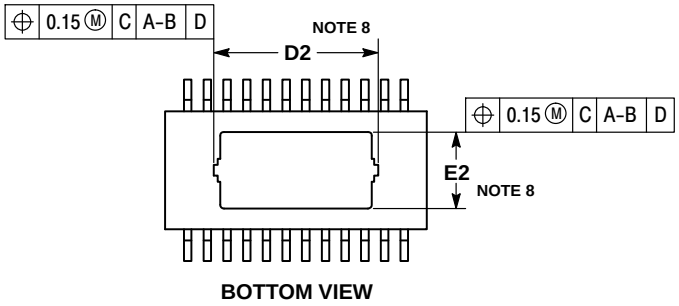
CASE 940AK
ISSUE O

DATE 24 APR 2012



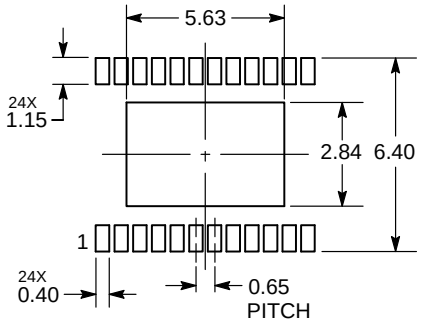




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.10 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. DIMENSION b APPLIES TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D IS DETERMINED AT DATUM PLANE H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM PLANE H.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. CONTOURS OF THE THERMAL PAD ARE UNCONTROLLED WITHIN THE REGION DEFINED BY DIMENSIONS D2 AND E2.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.70
A1	0.00	0.10
A2	1.10	1.65
b	0.19	0.30
c	0.09	0.20
D	8.64 BSC	
D2	5.28	5.58
E	6.00 BSC	
E1	3.90 BSC	
E2	2.44	2.64
e	0.65 BSC	
h	0.25	0.50
L	0.40	0.85
L1	1.00 REF	
L2	0.25 BSC	
M	0°	8°

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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