NLSX4401DFT2G

1-Bit 20 Mb/s Dual-Supply Level Translator

The NLSX4401DFT2G is a 1−bit configurable dual−supply bidirectional auto sensing translator that does not require a directional control pin. The I/O V_{CC} and I/O V_L ports are designed to track two different power supply rails, V_{CC} and V_L respectively. Both the V_{CC} and V_L supply rails are configurable from 1.65 V to 5.5 V. This allows voltage logic signals on the V_L side to be translated into lower, higher or equal value voltage logic signals on the V_{CC} side, and vice−versa.

The NLSX4401DFT2G translator has integrated 10 kΩ pull−up resistors on the I/O lines. The integrated pull−up resistors are used to pull up the I/O lines to either V_L or V_{CC}. The NLSX4401 is an excellent match for open−drain applications such as the I^2C communication bus.

Features

- V_L can be Less than, Greater than or Equal to V_{CC}
- Wide V_{CC} Operating Range: 1.65 V to 5.5 V
  Wide V_L Operating Range: 1.65 V to 5.5 V
- High Speed with 24 Mb/s Guaranteed Date Rate
- Low Bit−to−Bit Skew
- Enable Input and I/O Pins are Overvoltage Tolerant (OVT) to 5.5 V
- Non−preferential Powerup Sequencing
- Partial Power−Off Protection − I/Os at High Impedance with Either Supply at 0 V
- Integrated 10 kΩ Pull−up Resistors
- Small Space Saving Packages:
  SC−88/SC70−6/SOT−363 Package
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- I^2C, SMBus, PMBus
- Low Voltage ASIC Level Translation
- Mobile Phones, PDAs, Cameras

Important Information

- ESD Protection for All Pins
  − Human Body Model (HBM) > 5000 V

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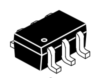
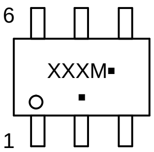
MARKING DIAGRAM



SC−88
2.10 x 2.0
CASE 419B

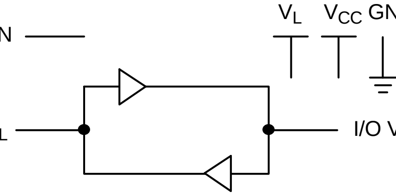


XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

LOGIC DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping†
NLSX4401DFT2G	SC−88 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

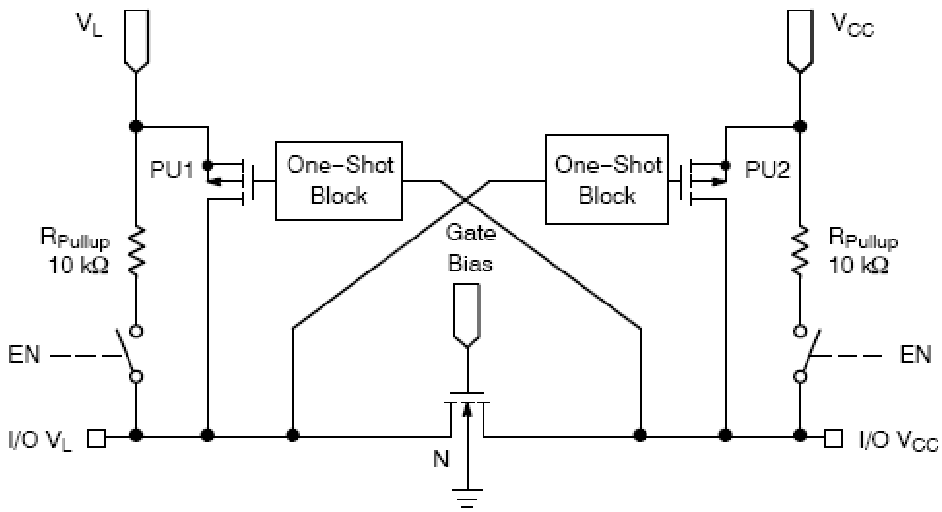
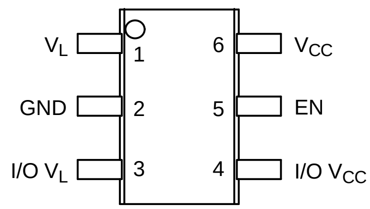


Figure 1. Block Diagram (1 I/O Line)



SC−88 / SC70−6 / SOT−363
(Top Through View)

Figure 2. Pinout Diagram

PIN ASSIGNMENT

Pins	Description
V_{CC}	V_{CC} Supply Voltage
V_L	V_L Supply Voltage
GND	Ground
EN	Output Enable, Referenced to V_L
I/O V_{CC}	I/O Port, Referenced to V_{CC}
I/O V_L	I/O Port, Referenced to V_L

FUNCTION TABLE

EN	Operating Mode
L	Hi−Z
H	I/O Buses Connected

MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	−0.5 to +7.0		V
V_L	DC Supply Voltage	−0.5 to +7.0		V
I/O V_{CC}	V_{CC}−Referenced DC Input/Output Voltage	−0.5 to +7.0		V
I/O V_L	V_L−Referenced DC Input/Output Voltage	−0.5 to +7.0		V
V_{EN}	Enable Control Pin DC Input Voltage	−0.5 to +7.0		V
I_{I/O_SC}	Short−Circuit Duration (I/O V_L and I/O V_{CC} to GND)	±50	Continuous	mA
$I_{I/OK}$	Input/Output Clamping Current (I/O V_L and I/O V_{CC})	−50	$V_{I/O} < 0$	mA
T_{STG}	Storage Temperature	−65 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage		1.5	5.5	V
V_L	Positive DC Supply Voltage		1.5	5.5	V
V_{EN}	Enable Control Pin Voltage		GND	5.5	V
V_{IO_VCC}	I/O Pin Voltage (Side referred to V_{CC})		GND	5.5	V
V_{IO_VL}	I/O Pin Voltage (Side referred to V_L)		GND	5.5	V
Δt/ΔV	Input Transition Rise and Fall Rate	A− or B−Ports, Push−Pull Driving Control Input		10 10	ns/V
T_A	Operating Temperature Range		−55	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (V_L = 1.65 V to 5.5 V and V_{CC} = 1.65 V to 5.5 V, unless otherwise specified) (Note 1)

Symbol	Parameter	Test Conditions (Note 2)	−55°C to +125°C			Unit
			Min	Typ	Max	
V_{IHC}	I/O V_{CC} Input HIGH Voltage		V_{CC} – 0.4	–	–	V
V_{ILC}	I/O V_{CC} Input LOW Voltage		–	–	0.15	V
V_{IHL}	I/O VL Input HIGH Voltage		V_L – 0.4	–	–	V
V_{ILL}	I/O VL Input LOW Voltage		–	–	0.15	V
V_{IH}	Control Pin Input HIGH Voltage		0.65 * V_L	–	–	V
V_{IL}	Control Pin Input LOW Voltage	V_L = 1.65 V to 1.95 V V_L = 2.3 V to 5.5 V	– –	– –	0.25 * V_L 0.35 * V_L	V
V_{OHC}	I/O V_{CC} Output HIGH Voltage	I/O V_{CC} source current = 20 μA	2/3 * V_{CC}	–	–	V
V_{OLC}	I/O V_{CC} Output LOW Voltage	I/O V_{CC} sink current = 1 mA	–	–	0.4	V
V_{OHL}	I/O V_L Output HIGH Voltage	I/O V_L source current = 20 μA	2/3 * V_L	–	–	V
V_{OLL}	I/O V_L Output LOW Voltage	I/O V_L sink current = 1 mA	–	–	0.4	V
I_{QVCC}	V_{CC} Supply Current	I/O V_{CC} and I/O V_L unconnected, V_{EN} = V_L V_L = 5.5 V, V_{CC} = 0 V V_L = 0 V, V_{CC} = 5.5 V	– – –	0.5 – –	3.0 −1.0 1.0	μA
I_{QVL}	V_L Supply Current	I/O V_{CC} and I/O V_L unconnected, V_{EN} = V_L V_L = 5.5 V, V_{CC} = 0 V V_L = 0 V, V_{CC} = 5.5 V	– – –	0.3 – –	3.0 1.0 −1.0	μA
I_{TS-VCC}	V_{CC} Tristate Output Mode	I/O V_{CC} and I/O V_L unconnected, V_{EN} = GND	–	0.1	1.5	μA
I_{TS-VL}	V_L Tristate Output Mode Supply Current	I/O V_{CC} and I/O V_L unconnected, V_{EN} = GND	–	0.1	1.5	μA
I_I	Enable Pin Input Leakage Current		–	–	1.0	μA
I_{OFF}	I/O Power-Off Leakage Current	I/O V_{CC} Port, V_{CC} = 0 V, V_L = 0 to 5.5 V	–	–	1.0	μA
		I/O VL Port, VCC = 0 to 5.5 V, V_L = 0 V	–	–	1.0	
I_{OZ}	I/O Tristate Output Mode Leakage Current		–	0.1	1.0	μA
R_{PU}	Pull−Up Resistors I/O V_L and V_C		–	10	–	kΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Typical values are for V_L = +1.8 V, V_{CC} = +3.3 V and T_A = +25°C.
2. All units are production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

TIMING CHARACTERISTICS − RAIL−TO−RAIL DRIVING CONFIGURATIONS

(I/O test circuit of Figures 3 and 4, C_{LOAD} = 15 pF, driver output impedance ≤ 50 Ω, R_{LOAD} = 1 MΩ)

Symbol	Parameter	Test Conditions	−40°C to +85°C (Notes 3 & 4) Min	Typ	Max	Unit
V_L = 1.65 V, V_{CC} = 1.65 V						
t_{RVCC}	I/O V_{CC} Rise Time			9	32	ns
t_{FVCC}	I/O V_{CC} Fall Time			11	20	ns
t_{RVL}	I/O V_L Rise Time			20	30	ns
t_{FVL}	I/O V_L Fall Time			10	13	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L, V_L to V_{CC})			7	16	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC}, V_{CC} to V_L)			12	15	ns
t_{PZL}, t_{PZH}	Enable Time				269	ns
t_{PLZ}, t_{PHZ}	Disable Time				300	ns
t_{PPSKEW}	Part−to−Part Skew				2	ns
MDR	Maximum Data Rate		15			Mbps
V_L = 1.65 V, V_{CC} = 5.5 V						
t_{RVCC}	I/O V_{CC} Rise Time			9	12	ns
t_{FVCC}	I/O V_{CC} Fall Time			17	30	ns
t_{RVL}	I/O V_L Rise Time			8	10	ns
t_{FVL}	I/O V_L Fall Time			5	9	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L, V_L to V_{CC})			14	24	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC}, V_{CC} to V_L)			4	6	ns
t_{PZL}, t_{PZH}	Enable Time				66	ns
t_{PLZ}, t_{PHZ}	Disable Time				250	ns
t_{PPSKEW}	Part−to−Part Skew				2	ns
MDR	Maximum Data Rate		20			Mbps
V_L = 1.8 V, V_{CC} = 2.8 V						
t_{RVCC}	I/O V_{CC} Rise Time			11	18	ns
t_{FVCC}	I/O V_{CC} Fall Time			10	15	ns
t_{RVL}	I/O V_L Rise Time			12	15	ns
t_{FVL}	I/O V_L Fall Time			5	8	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L, V_L to V_{CC})			7	10	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC}, V_{CC} to V_L)			1	12	ns
t_{PZL}, t_{PZH}	Enable Time				100	ns
t_{PLZ}, t_{PHZ}	Disable Time				300	ns
t_{PPSKEW}	Part−to−Part Skew				2	ns
MDR	Maximum Data Rate		20			Mbps
V_L = 2.5 V, V_{CC} = 3.6 V						
t_{RVCC}	I/O V_{CC} Rise Time			8	12	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Typical values are for the specified V_L and V_{CC} at T_A = +25°C. All units are production tested at T_A = +25°C.
4. Limits over the operating temperature range are guaranteed by design.
5. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port (I/O_VLn or I/O_VCCn) and switching with the same polarity (LOW−to−HIGH or HIGH−to−LOW). Skew is defined by applying a single input to the two input channels and measuring the difference in propagation delays between the output channels.

TIMING CHARACTERISTICS − RAIL−TO−RAIL DRIVING CONFIGURATIONS (continued)
(I/O test circuit of Figures 3 and 4, C_{LOAD} = 15 pF, driver output impedance ≤ 50 Ω, R_{LOAD} = 1 MΩ)

Symbol	Parameter	Test Conditions	−40°C to +85°C (Notes 3 & 4) Min	Typ	Max	Unit
V_L = 2.5 V, V_{CC} = 3.6 V						
t_{FVCC}	I/O V_{CC} Fall Time			8	12	ns
t_{RVL}	I/O V_L Rise Time			7	10	ns
t_{FVL}	I/O V_L Fall Time			5	7	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L, V_L to V_{CC})			7	10	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC}, V_{CC} to V_L)			5	8	ns
t_{PZL}, t_{PZH}	Enable Time				74	ns
t_{PLZ}, t_{PHZ}	Disable Time				225	ns
t_{PPSKEW}	Part−to−Part Skew				2	ns
MDR	Maximum Data Rate		24			Mbps
V_L = 2.8 V, V_{CC} = 1.8 V						
t_{RVCC}	I/O V_{CC} Rise Time			13	20	ns
t_{FVCC}	I/O V_{CC} Fall Time			7	10	ns
t_{RVL}	I/O V_L Rise Time			8	13	ns
t_{FVL}	I/O V_L Fall Time			9	15	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L, V_L to V_{CC})			6	9	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC}, V_{CC} to V_L)			7	12	ns
t_{PZL}, t_{PZH}	Enable Time				103	ns
t_{PLZ}, t_{PHZ}	Disable Time				250	ns
t_{PPSKEW}	Part−to−Part Skew				2	ns
MDR	Maximum Data Rate		24			Mbps
V_L = 3.6 V, V_{CC} = 2.5 V						
t_{RVCC}	I/O V_{CC} Rise Time			9	12	ns
t_{FVCC}	I/O V_{CC} Fall Time			6	9	ns
t_{RVL}	I/O V_L Rise Time			6	12	ns
t_{FVL}	I/O V_L Fall Time			7	12	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L, V_L to V_{CC})			5	7	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC}, V_{CC} to V_L)			6	9	ns
t_{PZL}, t_{PZH}	Enable Time				77	ns
t_{PLZ}, t_{PHZ}	Disable Time				250	ns
t_{PPSKEW}	Part−to−Part Skew				2	ns
MDR	Maximum Data Rate		24			Mbps
V_L = 5.5 V, V_{CC} = 1.65 V						
t_{RVCC}	I/O V_{CC} Rise Time			13	20	ns
t_{FVCC}	I/O V_{CC} Fall Time			6	9	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Typical values are for the specified V_L and V_{CC} at T_A = +25°C. All units are production tested at T_A = +25°C.
4. Limits over the operating temperature range are guaranteed by design.
5. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port (I/O_VLn or I/O_VCCn) and switching with the same polarity (LOW−to−HIGH or HIGH−to−LOW). Skew is defined by applying a single input to the two input channels and measuring the difference in propagation delays between the output channels.

TIMING CHARACTERISTICS − RAIL−TO−RAIL DRIVING CONFIGURATIONS (continued)
(I/O test circuit of Figures 3 and 4, C_{LOAD} = 15 pF, driver output impedance ≤ 50 Ω, R_{LOAD} = 1 MΩ)

Symbol	Parameter	Test Conditions	−40°C to +85°C (Notes 3 & 4) Min	Typ	Max	Unit
V_L = 5.5 V, V_{CC} = 1.65 V						
t_{RVL}	I/O V_L Rise Time			8	10	ns
t_{FVL}	I/O V_L Fall Time			22	37	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L, V_L to V_{CC})			9	13	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC}, V_{CC} to V_L)			13	25	ns
t_{PZL}, t_{PZH}	Enable Time					ns
t_{PLZ}, t_{PHZ}	Disable Time					ns
t_{PPSKEW}	Part−to−Part Skew				2	ns
MDR	Maximum Data Rate		20			Mbps
V_L = 5.5 V, V_{CC} = 5.5 V						
t_{RVCC}	I/O V_{CC} Rise Time			5	7	ns
t_{FVCC}	I/O V_{CC} Fall Time			6	8	ns
t_{RVL}	I/O V_L Rise Time			5	7	ns
t_{FVL}	I/O V_L Fall Time			5	8	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L, V_L to V_{CC})			4	6	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC}, V_{CC} to V_L)			4	6	ns
t_{PZL}, t_{PZH}	Enable Time				30	ns
t_{PLZ}, t_{PHZ}	Disable Time				225	ns
t_{PPSKEW}	Part−to−Part Skew				2	ns
MDR	Maximum Data Rate		24			Mbps

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
3. Typical values are for the specified V_L and V_{CC} at T_A = +25°C. All units are production tested at T_A = +25°C.
4. Limits over the operating temperature range are guaranteed by design.
5. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port (I/O_VLn or I/O_VCCn) and switching with the same polarity (LOW−to−HIGH or HIGH−to−LOW). Skew is defined by applying a single input to the two input channels and measuring the difference in propagation delays between the output channels.

TIMING CHARACTERISTICS − OPEN DRAIN DRIVING CONFIGURATIONS
(I/O test circuit of Figures 5 and 6, C_{LOAD} = 15 pF, driver output impedance ≤ 50 Ω, R_{LOAD} = 1 MΩ)

Symbol	Parameter	Test Conditions	−40°C to +85°C (Notes 6 & 7) Min	Typ	Max	Unit
V_L = 1.65 V, V_{CC} = 1.65 V						
t_{RVCC}	I/O V_{CC} Rise Time			55	70	ns
t_{FVCC}	I/O V_{CC} Fall Time			7	14	ns
t_{RVL}	I/O V_L Rise Time			50	65	ns
t_{FVL}	I/O V_L Fall Time			7	12	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
6. Typical values are for the specified V_L and V_{CC} at T_A = +25°C. All units are production tested at T_A = +25°C.
7. Limits over the operating temperature range are guaranteed by design.
8. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port (I/O_VLn or I/O_VCCn) and switching with the same polarity (LOW−to−HIGH or HIGH−to−LOW). Skew is defined by applying a single input to the two input channels and measuring the difference in propagation delays between the output channels.

TIMING CHARACTERISTICS − OPEN DRAIN DRIVING CONFIGURATIONS (continued)
(I/O test circuit of Figures 5 and 6, C_{LOAD} = 15 pF, driver output impedance ≤ 50 Ω, R_{LOAD} = 1 MΩ)

Symbol	Parameter	Test Conditions	−40°C to +85°C (Notes 6 & 7) Min	Typ	Max	Unit
V_L = 1.65 V, V_{CC} = 1.65 V						
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L, V_L to V_{CC})			20	34	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC}, V_{CC} to V_L)			19	34	ns
t_{PZL}, t_{PZH}	Enable Time				100	ns
t_{PLZ}, t_{PHZ}	Disable Time				300	ns
t_{PPSKEW}	Part−to−Part Skew				2	ns
MDR	Maximum Data Rate		3			Mbps
V_L = 1.65 V, V_{CC} = 5.5 V						
t_{RVCC}	I/O V_{CC} Rise Time			22	34	ns
t_{FVCC}	I/O V_{CC} Fall Time			20	27	ns
t_{RVL}	I/O V_L Rise Time			43	55	ns
t_{FVL}	I/O V_L Fall Time			6	12	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L, V_L to V_{CC})			13	26	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC}, V_{CC} to V_L)			19	24	ns
t_{PZL}, t_{PZH}	Enable Time				80	ns
t_{PLZ}, t_{PHZ}	Disable Time				250	ns
t_{PPSKEW}	Part−to−Part Skew				2	ns
MDR	Maximum Data Rate		3			Mbps
V_L = 1.8 V, V_{CC} = 3.3 V						
t_{RVCC}	I/O V_{CC} Rise Time			34	40	ns
t_{FVCC}	I/O V_{CC} Fall Time			1	15	ns
t_{RVL}	I/O V_L Rise Time			40	48	ns
t_{FVL}	I/O V_L Fall Time			1	2	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L, V_L to V_{CC})			9	15	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC}, V_{CC} to V_L)			6	11	ns
t_{PZL}, t_{PZH}	Enable Time				70	ns
t_{PLZ}, t_{PHZ}	Disable Time				300	ns
t_{PPSKEW}	Part−to−Part Skew				2	ns
MDR	Maximum Data Rate		7			Mbps
V_L = 5.5 V, V_{CC} = 1.65 V						
t_{RVCC}	I/O V_{CC} Rise Time			44	52	ns
t_{FVCC}	I/O V_{CC} Fall Time			1	2	ns
t_{RVL}	I/O V_L Rise Time			7	30	ns
t_{FVL}	I/O V_L Fall Time			17	23	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L, V_L to V_{CC})			10	17	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
6. Typical values are for the specified V_L and V_{CC} at T_A = +25°C. All units are production tested at T_A = +25°C.
7. Limits over the operating temperature range are guaranteed by design.
8. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port (I/O_VLn or I/O_VCCn) and switching with the same polarity (LOW−to−HIGH or HIGH−to−LOW). Skew is defined by applying a single input to the two input channels and measuring the difference in propagation delays between the output channels.

TIMING CHARACTERISTICS − OPEN DRAIN DRIVING CONFIGURATIONS (continued)
(I/O test circuit of Figures 5 and 6, C_{LOAD} = 15 pF, driver output impedance ≤ 50 Ω, R_{LOAD} = 1 MΩ)

Symbol	Parameter	Test Conditions	−40°C to +85°C (Notes 6 & 7) Min	Typ	Max	Unit
V_L = 5.5 V, V_{CC} = 1.65 V						
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC}, V_{CC} to V_L)			12	24	ns
t_{PZL}, t_{PZH}	Enable Time				100	ns
t_{PLZ}, t_{PHZ}	Disable Time				300	ns
t_{PPSKEW}	Part−to−Part Skew				2	ns
MDR	Maximum Data Rate		3			Mbps
V_L = 5.5 V, V_{CC} = 5.5 V						
t_{RVCC}	I/O V_{CC} Rise Time			42	50	ns
t_{FVCC}	I/O V_{CC} Fall Time			2	3	ns
t_{RVL}	I/O V_L Rise Time			44	48	ns
t_{FVL}	I/O V_L Fall Time			2	3	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L, V_L to V_{CC})			4	6	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC}, V_{CC} to V_L)			6	9	ns
t_{PZL}, t_{PZH}	Enable Time				60	ns
t_{PLZ}, t_{PHZ}	Disable Time				225	ns
t_{PPSKEW}	Part−to−Part Skew				2	ns
MDR	Maximum Data Rate		7			Mbps

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Typical values are for the specified V_L and V_{CC} at T_A = +25°C. All units are production tested at T_A = +25°C.
7. Limits over the operating temperature range are guaranteed by design.
8. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port (I/O_VLn or I/O_VCCn) and switching with the same polarity (LOW−to−HIGH or HIGH−to−LOW). Skew is defined by applying a single input to the two input channels and measuring the difference in propagation delays between the output channels.

TEST SETUP

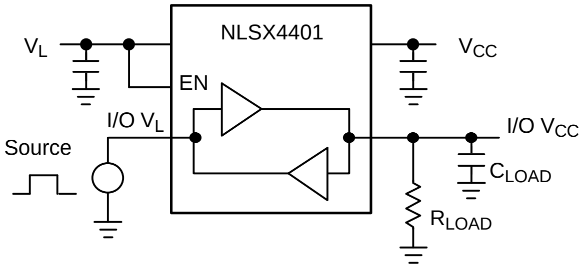


Figure 3. Rail−to−Rail Driving I/O V_L

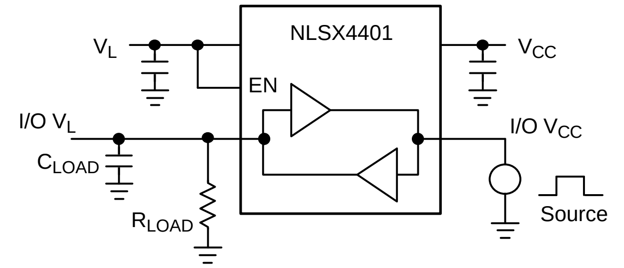


Figure 4. Rail−to−Rail Driving I/O V_{CC}

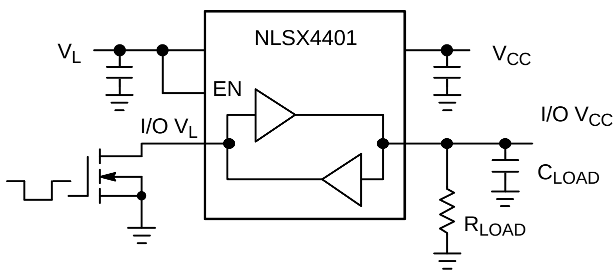


Figure 5. Open−Drain Driving I/O V_L

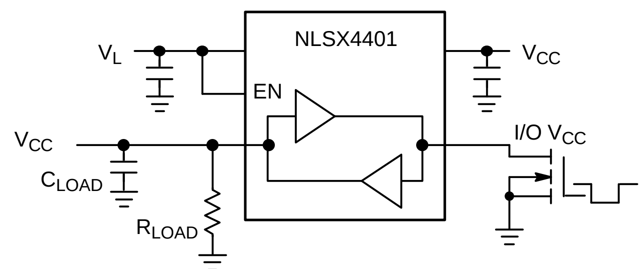


Figure 6. Open−Drain Driving I/O V_{CC}

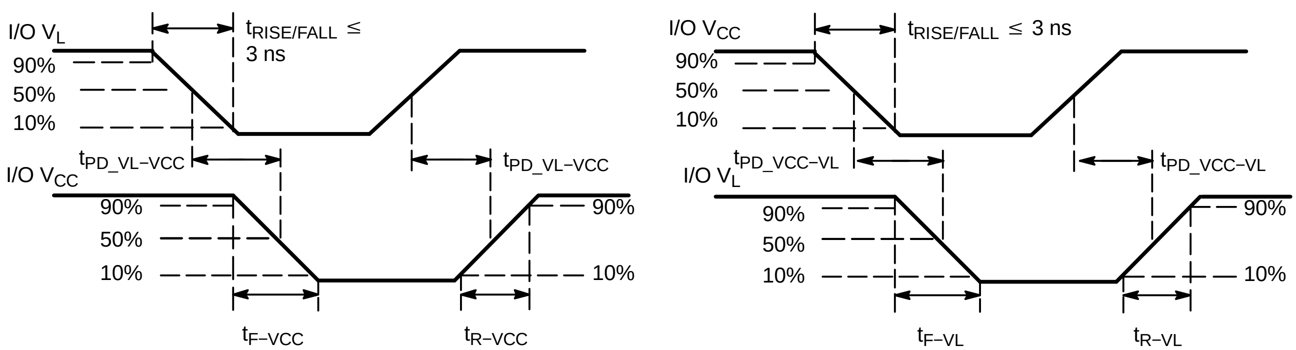
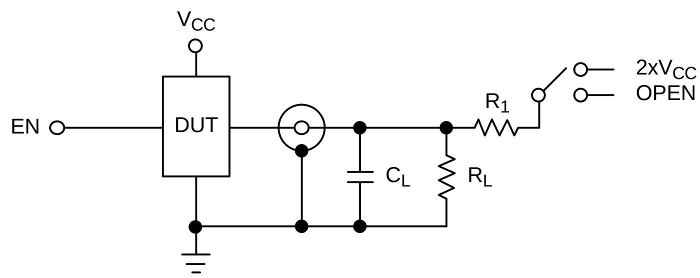


Figure 7. Definition of Timing Specification Parameters



Test	Switch
t_{PZH}, t_{PHZ}	Open
t_{PZL}, t_{PLZ}	2 x V_{CC}

C_L = 15 pF or equivalent (Includes jig and probe capacitance)
R_L = R_1 = 50 kΩ or equivalent

Figure 8. Test Circuit for Enable/Disable Time Measurement

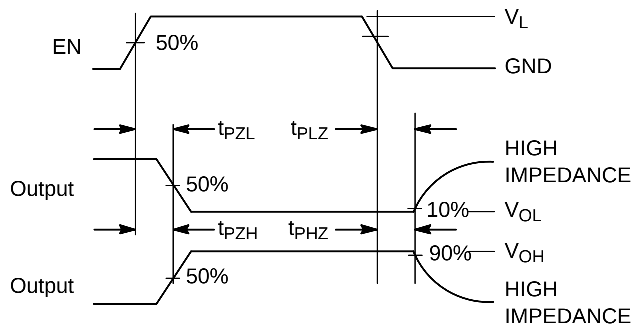


Figure 9. Timing Definitions for Propagation Delays and Enable/Disable Measurement

APPLICATIONS INFORMATION

Level Translator Architecture

The NLSX4401 auto sense translator provides bi−directional voltage level shifting to transfer data in multiple supply voltage systems. This device has two supply voltages, V_L and V_{CC}, which set the logic levels on the input and output sides of the translator. When used to transfer data from the I/O V_L to the I/O V_{CC} ports, input signals referenced to the V_L supply are translated to output signals with a logic level matched to V_{CC}. In a similar manner, the I/O V_{CC} to I/O V_L translation shifts input signals with a logic level compatible to V_{CC} to an output signal matched to V_L.

The NLSX4401 consists of a bi−directional channels that independently determines the direction of the data flow without requiring a directional pin. The one−shot circuits are used to detect the rising input signals. In addition, the one shots decrease the rise time of the output signal for low−to−high transitions.

Each input/output channel has an internal 10 kΩ pull−up. The magnitude of the pull−up resistors can be reduced by connecting external resistors in parallel to the internal 10 kΩ resistors.

Input Driver Requirements

The rise (t_R) and fall (t_F) timing parameters of the open drain outputs depend on the magnitude of the pull−up resistors. In addition, the propagation times (t_{PHL} / t_{PLH}), skew (t_{PSKEW}) and maximum data rate depend on the impedance of the device that is connected to the translator. The timing parameters listed in the data sheet assume that the output impedance of the drivers connected to the translator is less than 50 kΩ.

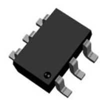
Enable Input (EN)

The NLSX4401 has an Enable pin (EN) that provides tri−state operation at the I/O pins. Driving the Enable pin to a low logic level minimizes the power consumption of the device and drives the I/O V_{CC} and I/O V_L pins to a high impedance state. Normal translation operation occurs when the EN pin is equal to a logic high signal. The EN pin is referenced to the V_L supply and has Overvoltage Tolerant (OVT) protection.

Power Supply Guidelines

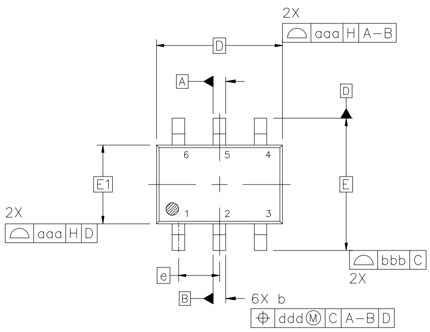
During normal operation, supply voltage V_L can be greater than, less than or equal to V_{CC}. The sequencing of the power supplies will not damage the device during the power up operation.

For optimal performance, 0.01 μF to 0.1 μF decoupling capacitors should be used on the V_{CCA} and V_{CCB} power supply pins. Ceramic capacitors are a good design choice to filter and bypass any noise signals on the voltage lines to the ground plane of the PCB. The noise immunity will be maximized by placing the capacitors as close as possible to the supply and ground pins, along with minimizing the PCB connection traces.



SC−88 2.00x1.25x0.90, 0.65P
CASE 419B−02
ISSUE Z

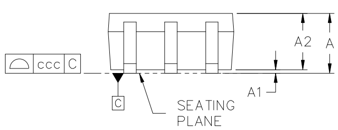
DATE 18 APR 2024



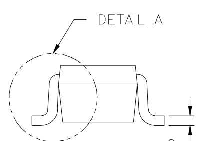
TOP VIEW

NOTES:

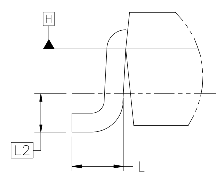
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.



SIDE VIEW

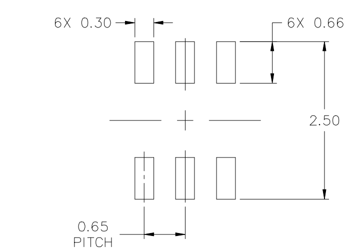


END VIEW



DETAIL A
SCALE 2:1

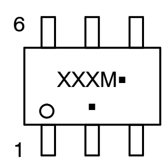
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	−−−	−−−	1.10
A1	0.00	−−−	0.10
A2	0.70	0.90	1.00
b	0.15	0.20	0.25
c	0.08	0.15	0.22
D	2.00 BSC		
E	2.10 BSC		
E1	1.25 BSC		
e	0.65 BSC		
L	0.26	0.36	0.46
L2	0.15 BSC		
aaa	0.15		
bbb	0.30		
ccc	0.10		
ddd	0.10		



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42985B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SC−88 2.00x1.25x0.90, 0.65P**	**PAGE 1 OF 2**

SC−88 2.00x1.25x0.90, 0.65P
CASE 419B−02
ISSUE Z

DATE 18 APR 2024

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

STYLE 30:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
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