

# **Dual Bias Resistor Transistor**

# NPN Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

# NSB1706DMW5T1G, NSVB1706DMW5T1G

The Bias Resistor Transistor (BRT) cntains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the NSB1706DMW5T1G, two BRT devices are housed in the SC-88A package which is ideal for low power surface mount applications where board space is at a premium.

#### **Features**

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

## **MAXIMUM RATINGS**

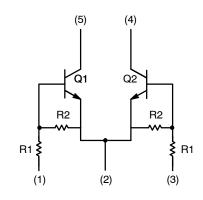
(T<sub>A</sub> = 25 °C unless otherwise noted, common for Q<sub>1</sub> and Q<sub>2</sub>)

Symbol	Rating	Value	Unit
V <sub>CBO</sub>	Collector-Base Voltage	50	Vdc
V <sub>CEO</sub>	Collector-Emitter Voltage	50	Vdc
I <sub>C</sub>	Collector Current	100	mAdc

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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#### MARKING DIAGRAM



U6 = Device Marking M = Date Code

■ = Pb-Free Package

(Note: Microdot may be in either location)

### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NSB1706DMW5T1G	SC-88A (Pb-Free)	3000 / Tape & Reel
NSVB1706DMW5T1G	SC-88A (Pb-Free)	3000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NSB1706DMW5T1G, NSVB1706DMW5T1G

## THERMAL CHARACTERISTICS

Symbol	Characteristic (One Junction Heated)	Max	Unit
P <sub>D</sub>	Total Device Dissipation $T_A = 25 ^{\circ}\text{C}$ Derate above 25 $^{\circ}\text{C}$	187 (Note 1) 256 (Note 2) 1.5 (Note 1) 2.0 (Note 2)	mW mW/°C
$R_{ hetaJA}$	Thermal Resistance, Junction-to-Ambient	670 (Note 1) 490 (Note 2)	°C/W
Symbol	Characteristic (Both Junctions Heated)	Max	Unit
P <sub>D</sub>	Total Device Dissipation $T_A = 25^{\circ}\text{C}$ Derate above 25 $^{\circ}\text{C}$	250 (Note 1) 385 (Note 2) 2.0 (Note 1) 3.0 (Note 2)	mW mW/°C
$R_{ heta JA}$	Thermal Resistance, Junction-to-Ambient	493 (Note 1) 325 (Note 2)	°C/W
$R_{ heta JL}$	Thermal Resistance, Junction-to-Lead	188 (Note 1) 208 (Note 2)	°C/W
T <sub>J</sub> , T <sub>stg</sub>	Junction and Storage Temperature	-55 to +150	°C

<sup>1.</sup> FR-4 @ Minimum Pad.

## **ELECTRICAL CHARACTERISTICS** ( $T_A = 25$ °C unless otherwise noted, common for $Q_1$ and $Q_2$ )

Symbol	Characteristic	Min	Тур	Max	Unit
OFF CHARAC	CTERISTICS		•		
I <sub>CBO</sub>	Collector-Base Cutoff Current (V <sub>CB</sub> = 50 V, I <sub>E</sub> = 0)	-	-	100	nAdc
I <sub>CEO</sub>	Collector-Emitter Cutoff Current (V <sub>CE</sub> = 50 V, I <sub>B</sub> = 0)	-	-	500	nAdc
I <sub>EBO</sub>	Emitter-Base Cutoff Current $(V_{EB} = 6.0 \text{ V}, I_{C} = 0)$	-	-	0.18	mAdc
V <sub>(BR)CBO</sub>	Collector-Base Breakdown Voltage ( $I_C = 10 \mu A, I_E = 0$ )	50	-	-	Vdc
V <sub>(BR)CEO</sub>	Collector-Emitter Breakdown Voltage (Note 3) (I <sub>C</sub> = 2.0 mA, I <sub>B</sub> = 0)	50	-	-	Vdc
ON CHARAC	TERISTICS (Note 3)	-			
h <sub>FE</sub>	DC Current Gain (V <sub>CE</sub> = 10 V, I <sub>C</sub> = 5.0 mA)	80	200	-	
V <sub>CE(sat)</sub>	Collector-Emitter Saturation Voltage ( $I_C = 10 \text{ mA}, I_B = 1 \text{ mA}$ )	-	-	0.25	Vdc
$V_{i(off)}$	Input Voltage (off) $(V_{CE} = 5.0 \text{ V}, I_{C} = 100 \mu\text{A})$	-	0.6	0.5	Vdc
V <sub>i(on)</sub>	Input Voltage (on) (V <sub>CE</sub> = 0.3 V, I <sub>C</sub> = 5 mA)	1.3	0.9	-	Vdc
V <sub>OL</sub>	Output Voltage (on) ( $V_{CC}$ = 5.0 V, $V_{B}$ = 2.5 V, $R_{L}$ = 1.0 k $\Omega$ )	-	-	0.2	Vdc
V <sub>OH</sub>	Output Voltage (off) $ (V_{CC} = 5.0 \text{ V}, V_B = 0.25 \text{ V}, R_L = 1.0 \text{ k}\Omega) $	4.9	-	-	Vdc
R1	Input Resistor	3.3	4.7	6.1	kΩ
R1/R2	Resistor Ratio	0.055	0.1	0.185	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. NOTE: New resistor combinations. Updated curves to follow in subsequent data sheets.

<sup>2.</sup> FR-4 @ 1.0 x 1.0 inch Pad.

<sup>3.</sup> Pulse Test: Pulse Width < 300  $\mu$ s, Duty Cycle < 2.0%.

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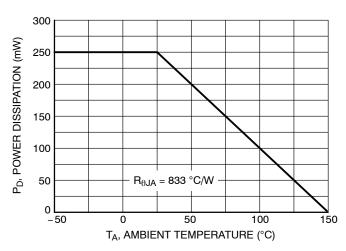


Figure 1. Derating Curve

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## **REVISION HISTORY**

Revision	Description of Changes	Date
7	Rebranded the Data Sheet to <b>onsemi</b> format.	7/11/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.





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5X b

◆ 0.2 M B M



## SC-88A (SC-70-5/SOT-353) CASE 419A-02 ISSUE M

**DATE 11 APR 2023** 

#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETERS
- 419A-01 DBSDLETE. NEW STANDARD 419A-02
- DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS,

DIM	MILLIMETERS			
الملتط	MIN.	N□M.	MAX.	
А	0.80	0.95	1.10	
A1			0.10	
A3		-		
b	0.10	0.20	0.30	
С	0.10		0.25	
D	1.80	2.00	2,20	
Е	2.00	2.10	2.20	
E1	1.15	1.25	1.35	
е	0.65 BSC			
L	0.10	0.15	0.30	

- OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

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Ţ <sup>0,40</sup>	0.50	——————————————————————————————————————	0.65
	1.90	o—	

#### RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SDLDERRM/D.

## **GENERIC MARKING DIAGRAM\***



\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code

= Date Code

= Pb-Free Package

(Note: Microdot may be in either location)

STYLE 1: PIN 1. BASE 2. EMITTER 3. BASE 4. COLLECTOR 5. COLLECTOR	STYLE 2: PIN 1. ANODE 2. EMITTER 3. BASE 4. COLLECTOR 5. CATHODE	STYLE 3: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. CATHODE 1	STYLE 4: PIN 1. SOURCE 1 2. DRAIN 1/2 3. SOURCE 1 4. GATE 1 5. GATE 2	STYLE 5: PIN 1. CATHODE 2. COMMON ANODE 3. CATHODE 2 4. CATHODE 3 5. CATHODE 4
STYLE 6: PIN 1. EMITTER 2 2. BASE 2 3. EMITTER 1 4. COLLECTOR 5. COLLECTOR 2/BASE 1	STYLE 7: PIN 1. BASE 2. EMITTER 3. BASE 4. COLLECTOR 5. COLLECTOR	STYLE 8: PIN 1. CATHODE 2. COLLECTOR 3. N/C 4. BASE 5. EMITTER	STYLE 9: PIN 1. ANODE 2. CATHODE 3. ANODE 4. ANODE 5. ANODE	Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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DESCRIPTION:	SC-88A (SC-70-5/SOT-353)		PAGE 1 OF 1	

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