ESD Protection Diode
Single Line CAN/LIN Bus Protector

NSQA6V8AW5T2 Series

This integrated surge protection device (surge protection) is designed for applications requiring transient overvoltage protection. It is intended for use in sensitive equipment such as computers, printers, business machines, communication systems, medical equipment, and other applications. Its integrated design provides very effective and reliable protection for four separate lines using only one package. These devices are ideal for situations where board space is at a premium.

Features

- Low Clamping Voltage
- Small SC−88A SMT Package
- Stand Off Voltage: 5 V
- Low Leakage Current < 1 μA
- Four Separate Unidirectional Configurations for Protection
- ESD Protection: IEC61000−4−2: Level 4
  MILSTD 883C − Method 3015−6: Class 3
- These Devices are Pb−Free and are RoHS Compliant

Benefits

- Provides Protection for ESD Industry Standards: IEC 61000, HBM
- Minimize Power Consumption of the System
- Minimize PCB Board Space

Typical Applications

- Instrumentation Equipment
- Serial and Parallel Ports
- Microprocessor Based Equipment
- Notebooks, Desktops, Servers
- Cellular and Portable Equipment

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Power Dissipation 8 × 20 μsec Double Exponential Waveform (Note 1)	P_{PK}	20	W
Steady State Power − 1 Diode (Note 2)	P_D	380	mW
Thermal Resistance − Junction−to−Ambient Above 25°C, Derate	$R_{\theta JA}$	 327 3.05	 °C/W mW/°C
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum 10 Seconds Duration	T_L	260	°C
IEC ^1000−4−2 (ESD) Contact		±8.0	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Non−repetitive current pulse per Figure 6.
2. Only 1 diode under power. For all 4 diodes under power, P_D will be 25%. Mounted on FR4 board with min pad.

See Application Note AND8308/D for further description of survivability specs.

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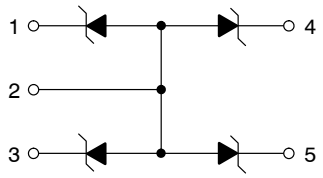
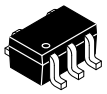
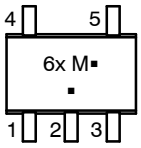




SC−88A/SOT−353
CASE 419A−02

MARKING DIAGRAM



x = H for NSQA6V8AW5T2
= X for NSQA12VAW5T2
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NSQA6V8AW5T2G	SC−88A (Pb−Free)	3000/Tape & Reel
NSQA12VAW5T2G	SC−88A (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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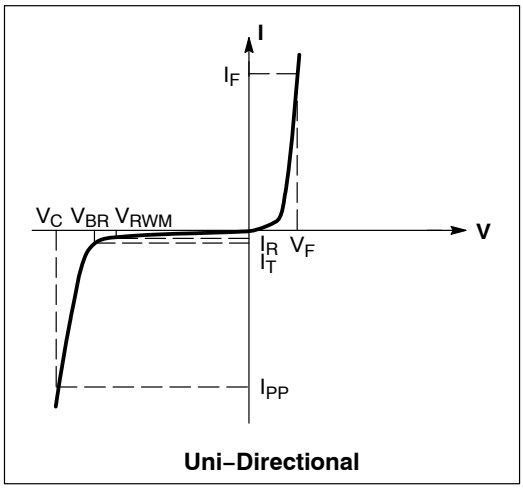
ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F
P_{pk}	Peak Power Dissipation
C	Capacitance @ V_R = 0 and f = 1.0 MHz

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
NSQA6V8AW5T2					
Breakdown Voltage (I_T = 1 mA) (Note 3)	V_{BR}	6.4	6.8	7.1	V
Leakage Current (V_{RWM} = 5.0 V)	I_R	–	–	1.0	μA
Clamping Voltage 1 (I_{PP} = 1.6 A) (Note 4)	V_C	–	–	13	V
Maximum Peak Pulse Current (Note 4)	I_{PP}	–	–	1.6	A
Junction Capacitance – (V_R = 0 V, f = 1 MHz) – (V_R = 3.0 V, f = 1 MHz)	C_J	– –	12 6.7	15 9.5	pF
Clamping Voltage – Per IEC61000−4−2	V_C	Figures 1 and 2			V
NSQA12VAW5T2					
Breakdown Voltage (I_T = 5 mA) (Note 3)	V_{BR}	11.4	12.0	12.7	V
Leakage Current (V_{RWM} = 9.0 V)	I_R	–	–	0.05	μA
Zener Impedence (I_T = 5 mA)	Z_Z	–	–	30	Ω
Clamping Voltage 1 (I_{PP} = 0.9 A) (Note 4)	V_C	–	–	23	V
Maximum Peak Pulse Current (Note 4)	I_{PP}	–	–	0.9	A
Junction Capacitance – (V_R = 0 V, f = 1 MHz)	C_J	–	–	15	pF
Clamping Voltage – Per IEC61000−4−2 (Note 5)	V_C	Figures 1 and 2			V

3. V_{BR} is measured at pulse test current I_T.
4. Surge current waveform per Figure 5.
5. For test procedure see Figures 3 and 4 and Application Note AND8307/D.

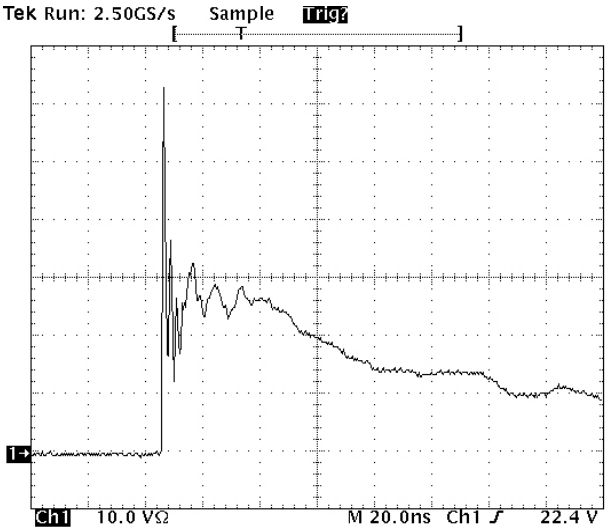


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2

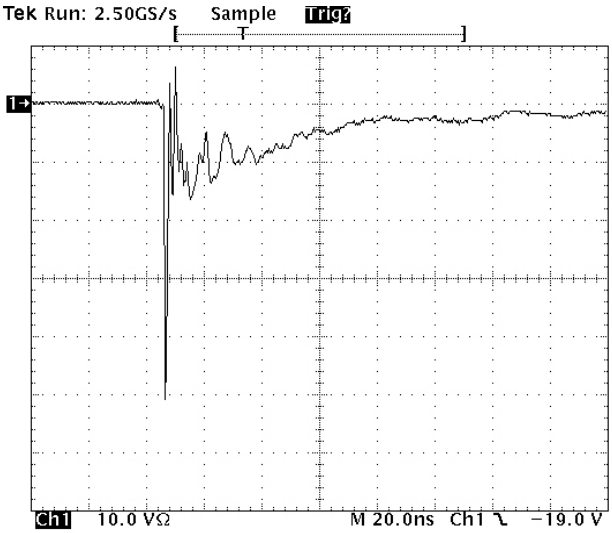


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

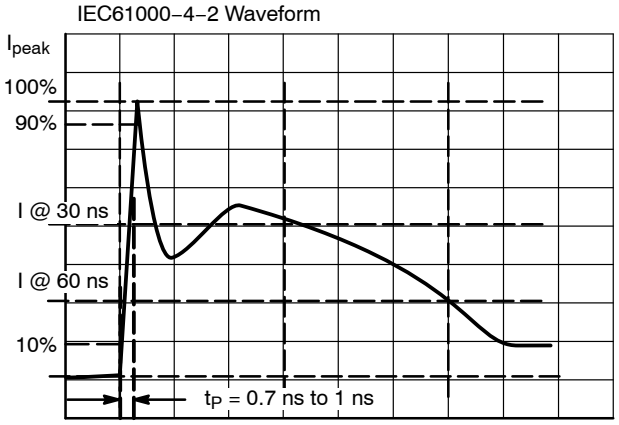


Figure 3. IEC61000−4−2 Spec

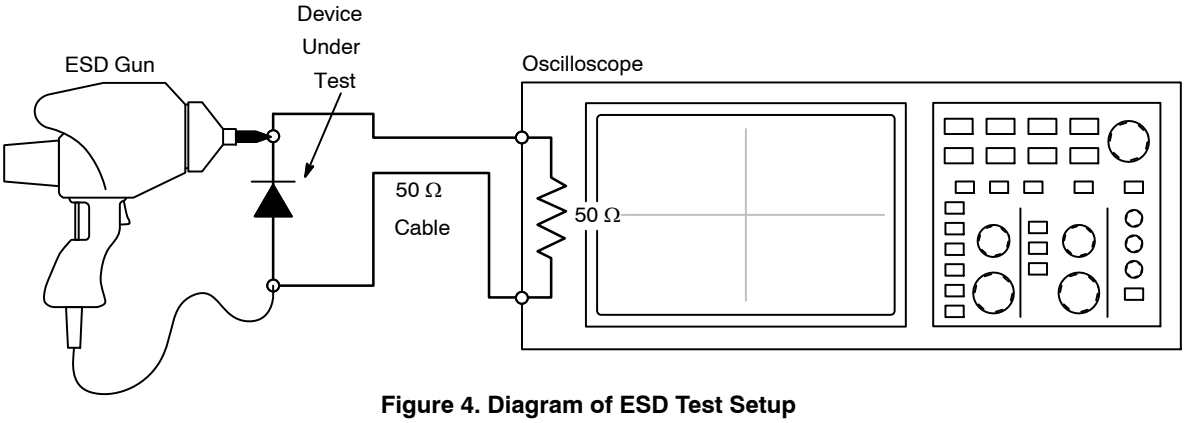


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

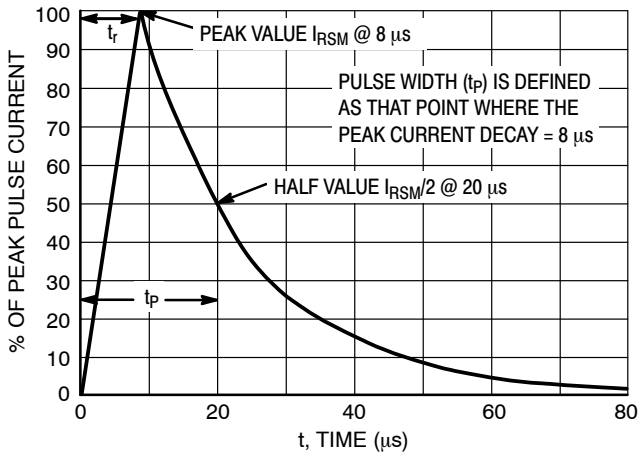


Figure 5. 8 x 20 μs Pulse Waveform

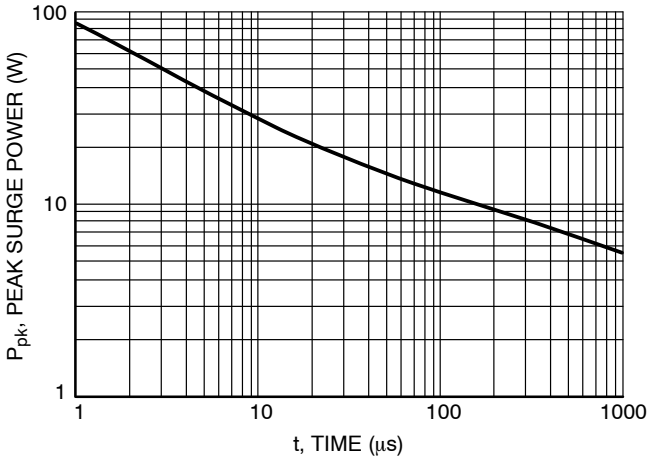


Figure 6. Pulse Width

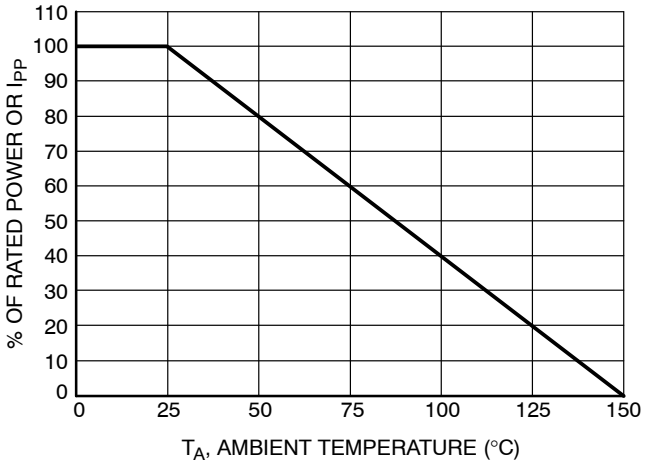


Figure 7. Power Derating Curve

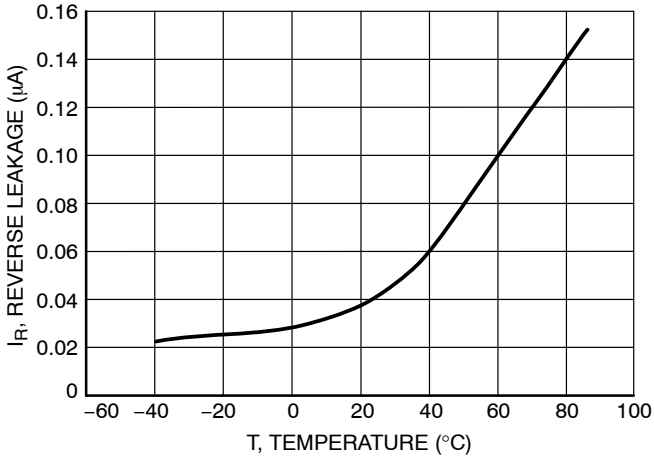


Figure 8. Reverse Leakage versus Temperature

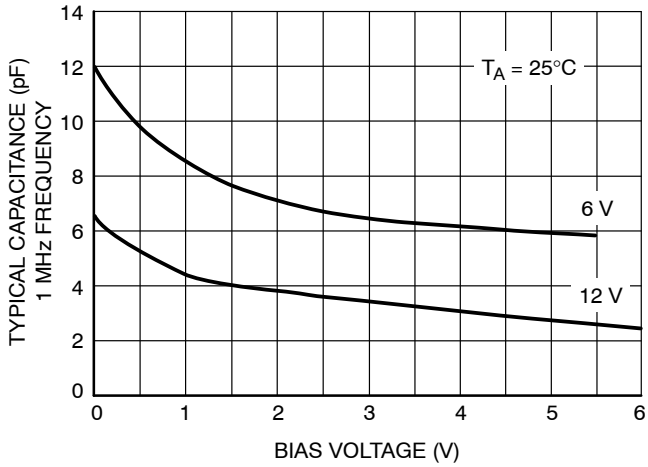


Figure 9. Capacitance

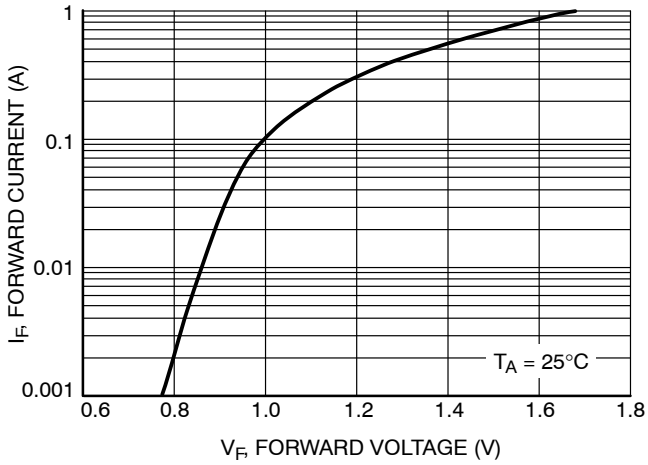
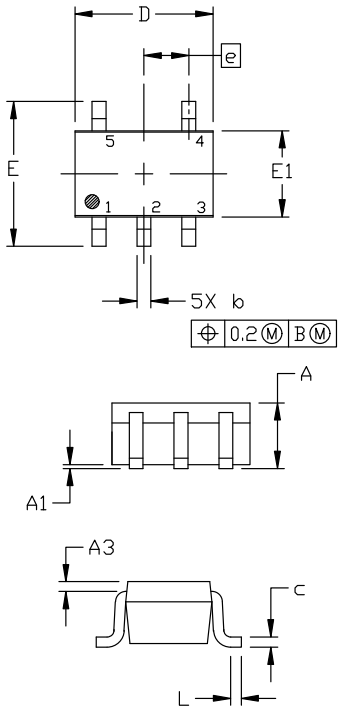


Figure 10. Forward Voltage

SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE M

SCALE 2:1

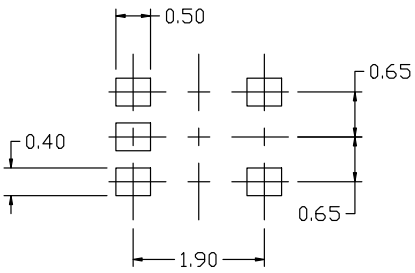
DATE 11 APR 2023



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

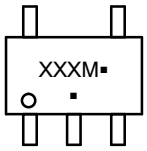
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3	0.20 REF		
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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DESCRIPTION:	SC−88A (SC−70−5/SOT−353)	PAGE 1 OF 1

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