NTB5405N, NVB5405N

MOSFET – Power, Single, N-Channel, D²PAK
40 V, 116 A

Features
- Low $R_{DS(on)}$
- High Current Capability
- Low Gate Charge
- AEC–Q101 Qualified and PPAP Capable – NVB5405N
- These Devices are Pb–Free and are RoHS Compliant

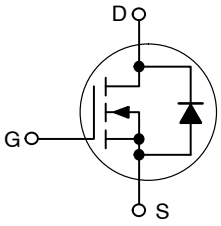
Applications
- Electronic Brake Systems
- Electronic Power Steering
- Bridge Circuits

ON Semiconductor®

http://onsemi.com

$V_{(BR)DSS}$	$R_{DS(ON)}$ TYP	I_D MAX (Note 1)
40 V	4.9 mΩ @ 10 V	116 A

N–Channel



MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

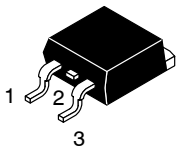
Parameter			Symbol	Value	Unit
Drain–to–Source Voltage			V_{DSS}	40	V
Gate–to–Source Voltage			V_{GS}	±20	V
Continuous Drain Current – $R_{\theta JC}$	Steady State	T_C = 25°C	I_D	116	A
		T_C = 100°C		82	
Power Dissipation – $R_{\theta JC}$	Steady State	T_C = 25°C	P_D	150	W
Continuous Drain Current – $R_{\theta JA}$ (Note 1)	Steady State	T_A = 25°C	I_D	16.5	A
		T_A = 100°C	I_D	11.6	
Power Dissipation – $R_{\theta JA}$ (Note 1)	Steady State	T_A = 25°C	P_D	3.0	W
Pulsed Drain Current	t_p = 10 μs		I_{DM}	280	A
Operating Junction and Storage Temperature			T_J, T_{STG}	–55 to 175	°C
Source Current (Body Diode) Pulsed			I_S	75	A
Single Pulse Drain–to Source Avalanche Energy – (V_{DD} = 50 V, V_{GS} = 10 V, I_{PK} = 40 A, L = 1 mH, R_G = 25 Ω)			EAS	800	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL RESISTANCE RATINGS

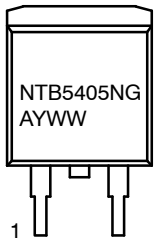
Parameter	Symbol	Max	Unit
Junction–to–Case (Drain)	$R_{\theta JC}$	1.0	°C/W
Junction–to–Ambient (Note 1)	$R_{\theta JA}$	50	°C/W

1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [2 oz] including traces).



D²PAK
CASE 418B
STYLE 2

MARKING DIAGRAM



NTB5405N	= Specific Device Code
G	= Pb–Free Device
A	= Assembly Location
Y	= Year
WW	= Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NTB5405NG	D²PAK (Pb–Free)	50 Units / Rail
NTB5405NT4G	D²PAK (Pb–Free)	800 / Tape & Reel
NVB5405NT4G	D²PAK (Pb–Free)	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise stated)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		40			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				39		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 40 V	T_J = 25°C			1.0	μA
			T_J = 100°C			10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±30 V				±100	nA
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.5		3.5	V
Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				−7.0		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 40 A			4.9	5.8	mΩ
		V_{GS} = 5.0 V, I_D = 15 A			7.0	8.0	
Forward Transconductance	g_{FS}	V_{GS} = 10 V, I_D = 15 A			32		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 32 V			2700	4000	pF
Output Capacitance	C_{OSS}				700	1400	
Reverse Transfer Capacitance	C_{RSS}				300	600	
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 32 V, I_D = 40 A			88		nC
Threshold Gate Charge	$Q_{G(TH)}$				3.25		
Gate−to−Source Charge	Q_{GS}				9.5		
Gate−to−Drain Charge	Q_{GD}				37		
SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 3)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DD} = 32 V, I_D = 40 A, R_G = 2.5 Ω			8.5		ns
Rise Time	t_r				52		
Turn−Off Delay Time	$t_{d(OFF)}$				55		
Fall Time	t_f				70		
SWITCHING CHARACTERISTICS, V_{GS} = 5 V (Note 3)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 5 V, V_{DD} = 20 V, I_D = 20 A, R_G = 2.5 Ω			19		ns
Rise Time	t_r				153		
Turn−Off Delay Time	$t_{d(OFF)}$				32		
Fall Time	t_f				42		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 20 A	T_J = 25°C		0.82	1.1	V
			T_J = 100°C		TBD		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_{SD}/dt = 100 A/μs, I_S = 20 A			66		ns
Charge Time	t_a				35		
Discharge Time	t_b				31		
Reverse Recovery Charge	Q_{RR}				113		nC

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

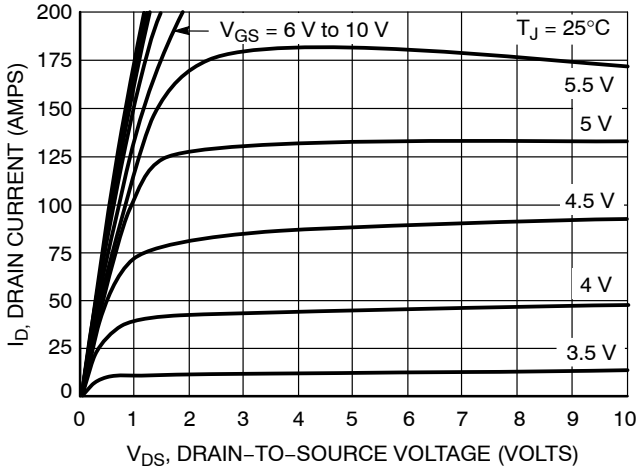


Figure 1. On−Region Characteristics

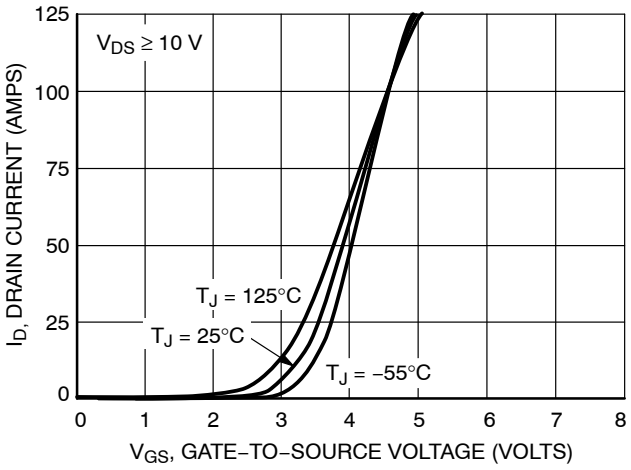


Figure 2. Transfer Characteristics

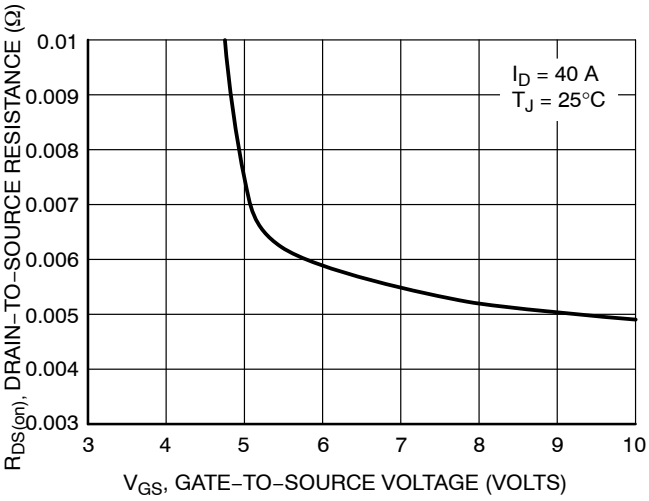


Figure 3. On−Resistance vs. Gate−to−Source Voltage

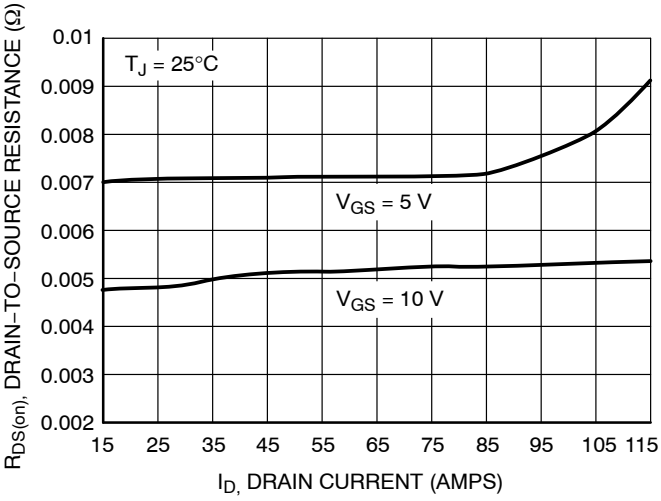


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

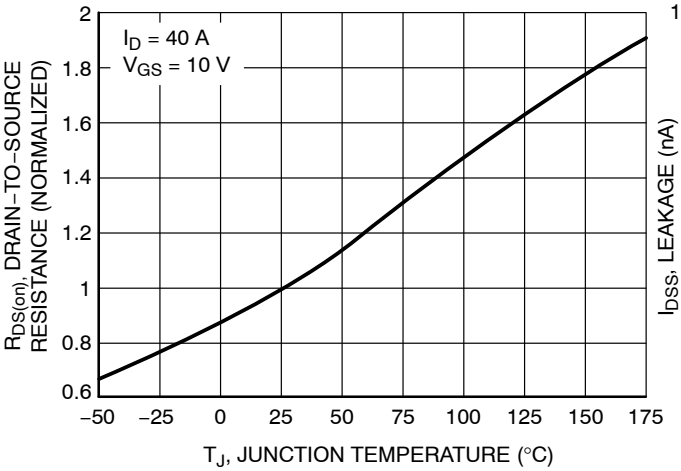


Figure 5. On−Resistance Variation with Temperature

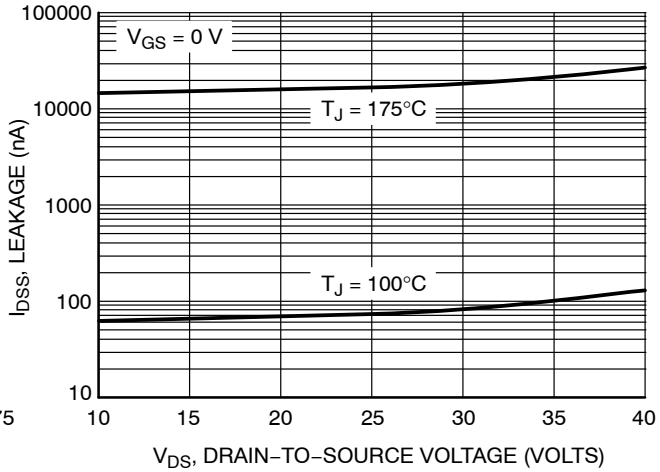


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

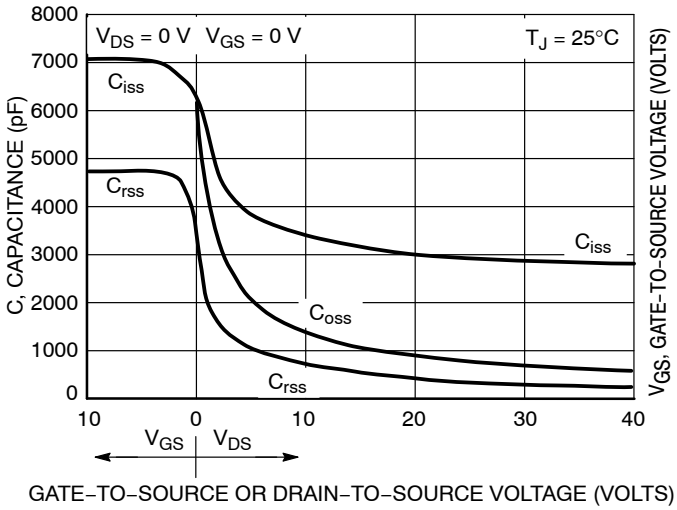


Figure 7. Capacitance Variation

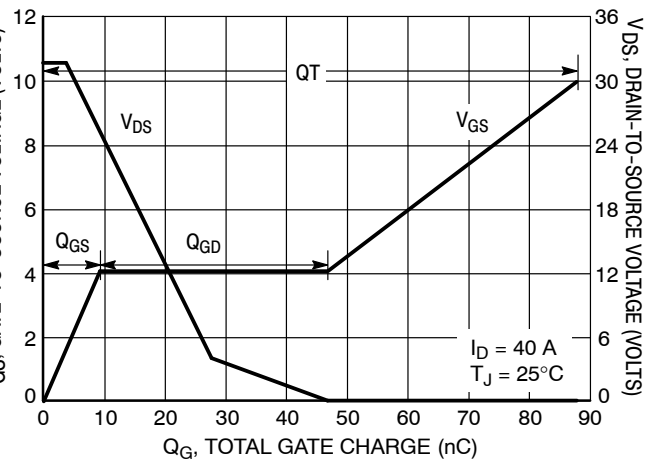


Figure 8. Gate−To−Source and Drain−To−Source Voltage vs. Total Charge

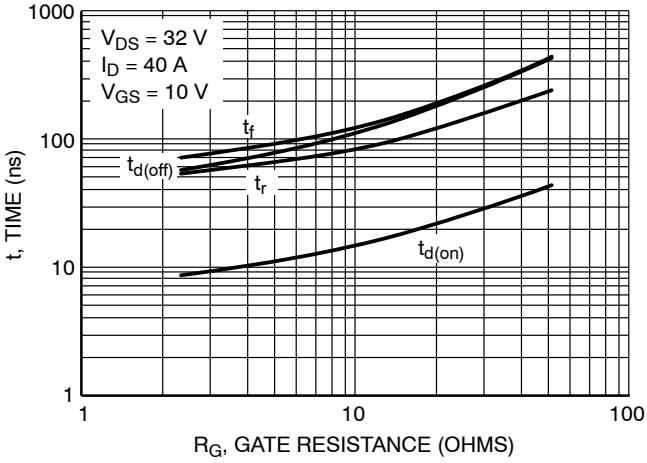


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

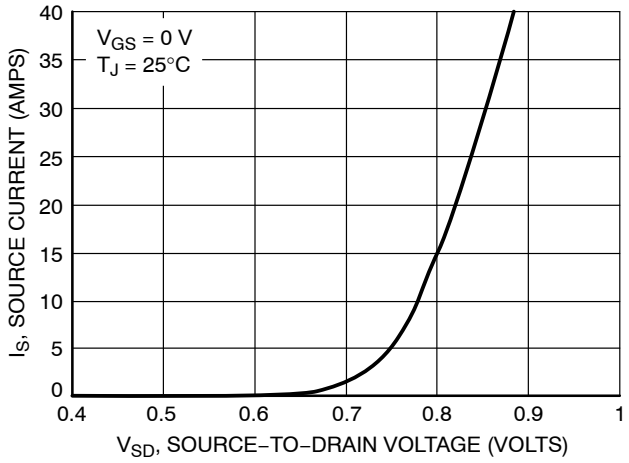


Figure 10. Diode Forward Voltage vs. Current

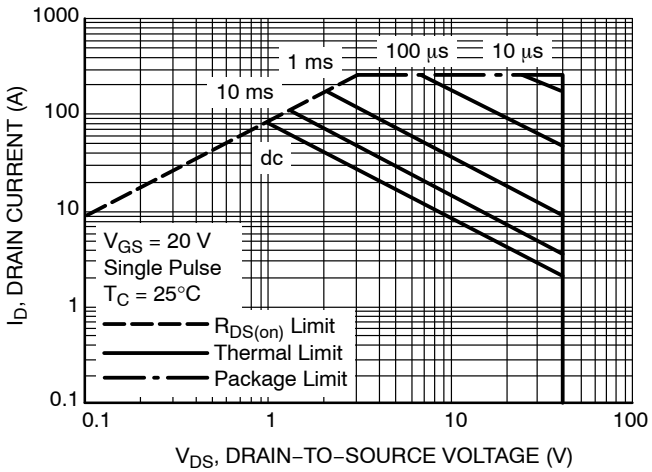


Figure 11. Maximum Rated Forward Biased Safe Operating Area

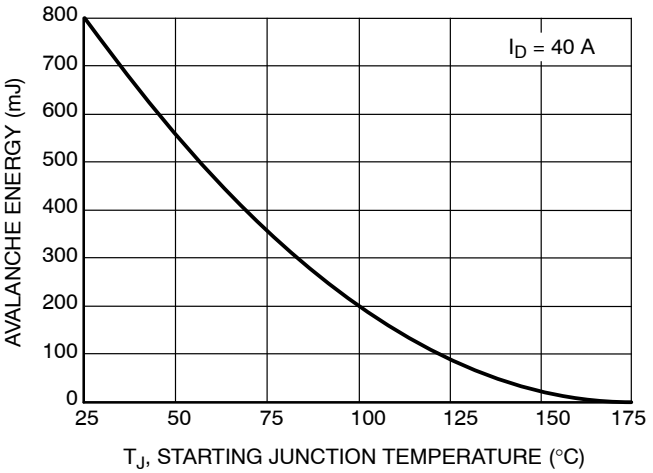


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

TYPICAL PERFORMANCE CURVES

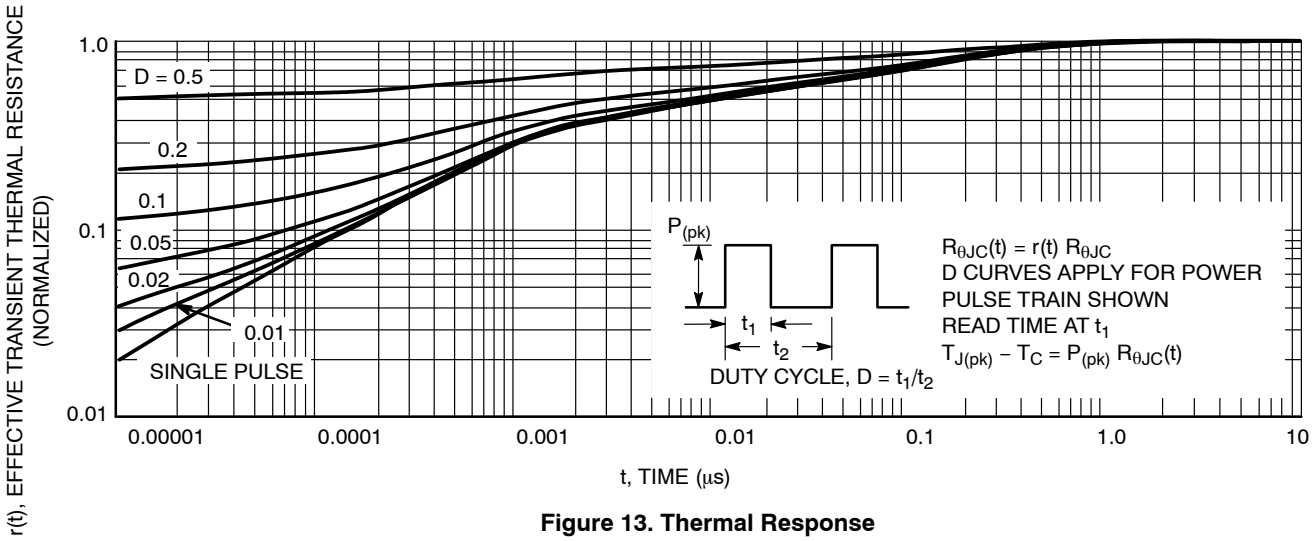
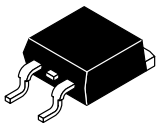


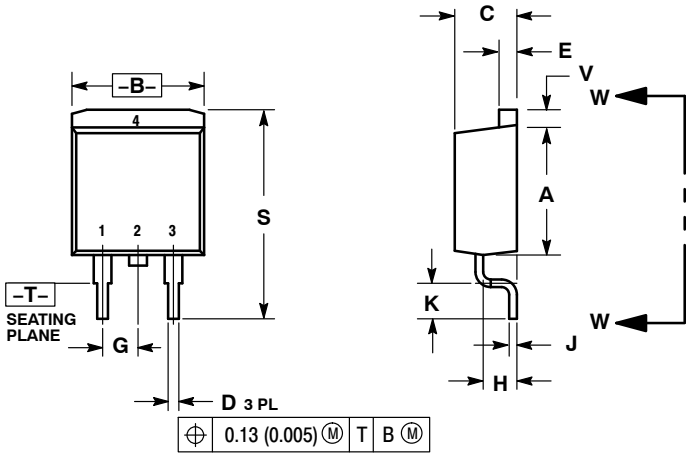
Figure 13. Thermal Response



D²PAK 3
CASE 418B–04
ISSUE L

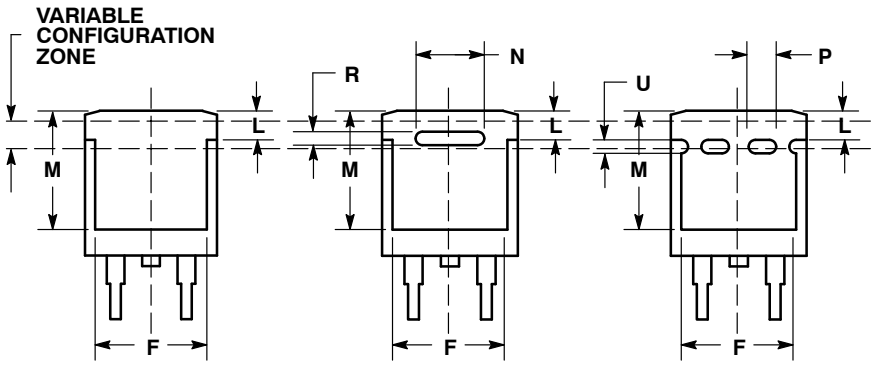
DATE 17 FEB 2015

SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B–01 THRU 418B–03 OBSOLETE, NEW STANDARD 418B–04.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197 REF		5.00 REF	
P	0.079 REF		2.00 REF	
R	0.039 REF		0.99 REF	
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40



VIEW W–W 1 | VIEW W–W 2 | VIEW W–W 3

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

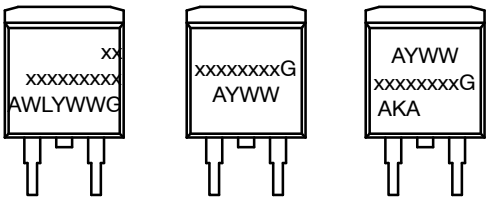
STYLE 6:
PIN 1. NO CONNECT
2. CATHODE
3. ANODE
4. CATHODE

MARKING INFORMATION AND FOOTPRINT ON PAGE 2

D²PAK 3
CASE 418B−04
ISSUE L

DATE 17 FEB 2015

GENERIC
MARKING DIAGRAM*

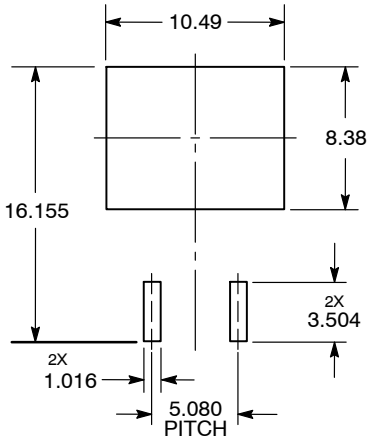


IC **Standard** **Rectifier**

xx	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package
AKA	= Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**D²PAK 3**		**PAGE 2 OF 2**

ADDITIONAL INFORMATION

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