

NTB5605P, NTB5605

MOSFET – Power, P-Channel, D²PAK

-60 V, -18.5 A

Features

- Designed for Low $R_{DS(on)}$
- Withstands High Energy in Avalanche and Commutation Modes
- AEC Q101 Qualified – NTB5605
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Power Supplies
- PWM Motor Control
- Converters
- Power Management

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	-60	V
Gate-to-Source Voltage			V_{GS}	± 20	V
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	I_D	-18.5	A
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	P_D	88	W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$		I_{DM}	-55	A
Operating Junction and Storage Temperature			T_J, T_{STG}	-55 to 175	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 25 \text{ V}, V_{GS} = 5.0 \text{ V}, I_{PK} = 15 \text{ A}, L = 3.0 \text{ mH}, R_G = 25 \Omega$)			E_{AS}	338	mJ
Lead Temperature for Soldering Purposes (1/8 in from case for 10 s)			T_L	260	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case (Drain) – Steady State	$R_{\theta JC}$	1.7	$^\circ\text{C}/\text{W}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

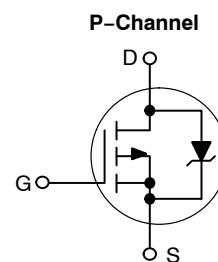
1. When surface mounted to an FR4 board using 1" pad size (Cu Area 1.127 in²).
2. When surface mounted to an FR4 board using the minimum recommended pad size (Cu Area 0.41 in²).



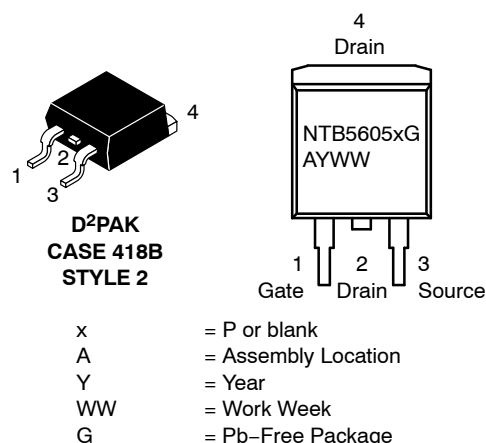
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<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
-60 V	120 m Ω @ -5.0 V	-18.5 A



MARKING DIAGRAM & PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
NTB5605PT4G	D ² PAK (Pb-Free)	800 / Tape & Reel
NTBV5605T4G	D ² PAK (Pb-Free)	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-60			V	
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			-64		mV/°C	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}$ $V_{DS} = -60\text{ V}$	$T_J = 25^\circ\text{C}$			-1.0	μA
			$T_J = 125^\circ\text{C}$			-10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA	

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = -250\ \mu\text{A}$	-1.0	-1.5	-2.0	V
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -5.0\text{ V}, I_D = -8.5\text{ A}$ $V_{GS} = -5.0\text{ V}, I_D = -17\text{ A}$		120 140	140	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = -10\text{ V}, I_D = -8.5\text{ A}$		12		S
Drain-to-Source On Voltage	$V_{DS(on)}$	$V_{GS} = -5.0\text{ V}, I_D = -8.5\text{ A}$			-1.3	V

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz},$ $V_{DS} = -25\text{ V}$		730	1190	pF
Output Capacitance	C_{oss}			211	300	
Reverse Transfer Capacitance	C_{rss}			67	120	
Total Gate Charge	$Q_G(TOT)$	$V_{GS} = -5.0\text{ V}, V_{DS} = -48\text{ V},$ $I_D = -17\text{ A}$		13	22	nC
Gate-to-Source Charge	Q_{GS}			4.0		
Gate-to-Drain Charge	Q_{GD}			7.0		

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -5.0\text{ V}, V_{DD} = -30\text{ V},$ $I_D = -17\text{ A}, R_G = 9.1\ \Omega$		12.5	25	ns
Rise Time	t_r			122	183	
Turn-Off Delay Time	$t_{d(off)}$			29	58	
Fall Time	t_f			75	150	

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}$ $I_S = -17\text{ A}$	$T_J = 25^\circ\text{C}$		-1.55	-2.5	V
			$T_J = 125^\circ\text{C}$		-1.4		
Reverse Recovery Time	t_{rr}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = -17\text{ A}$		60		ns	
Charge Time	t_a			39			
Discharge Time	t_b			21			
Reverse Recovery Charge	Q_{RR}			0.14			nC

3. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

4. Switching characteristics are independent of operating junction temperatures.

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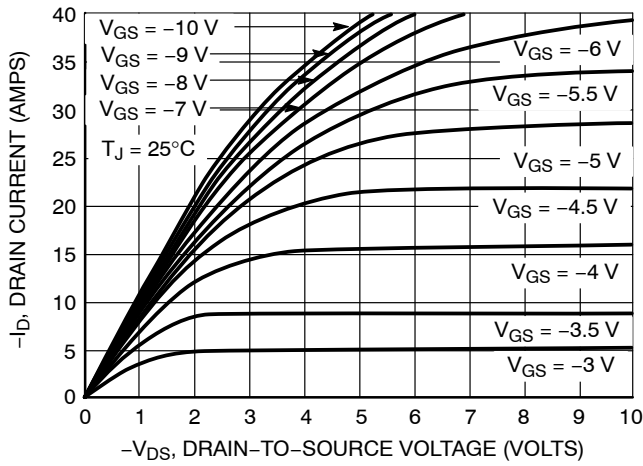


Figure 1. On-Region Characteristics

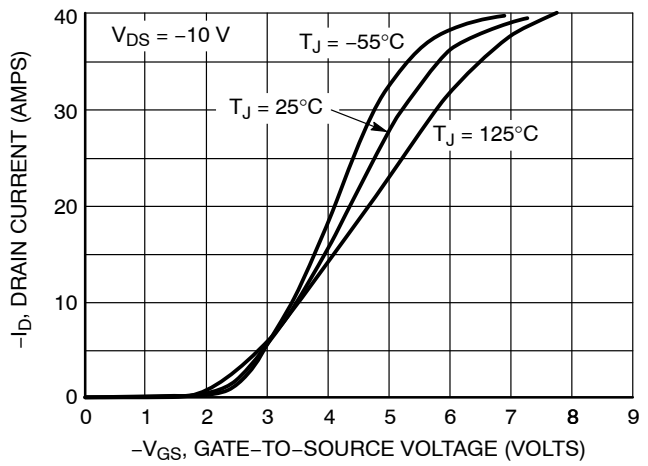


Figure 2. Transfer Characteristics

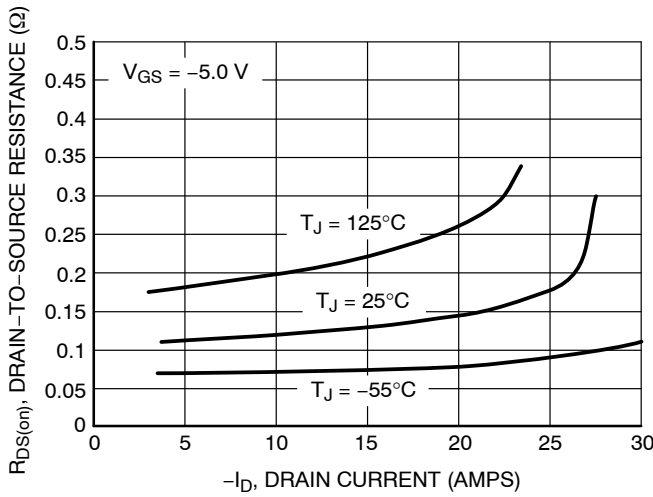


Figure 3. On-Resistance vs. Drain Current and Temperature

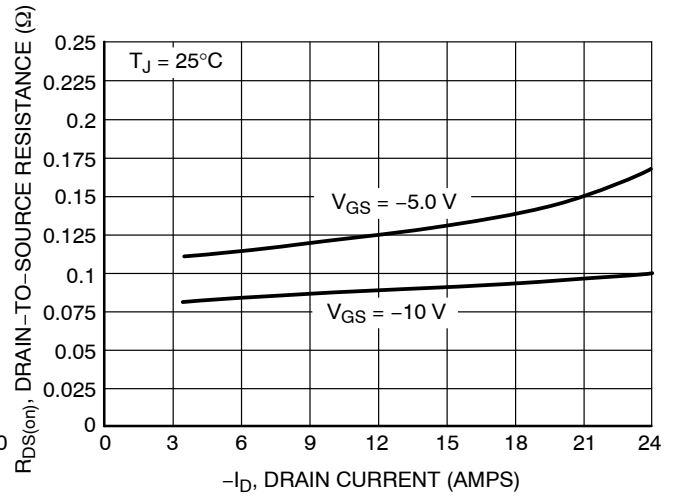


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

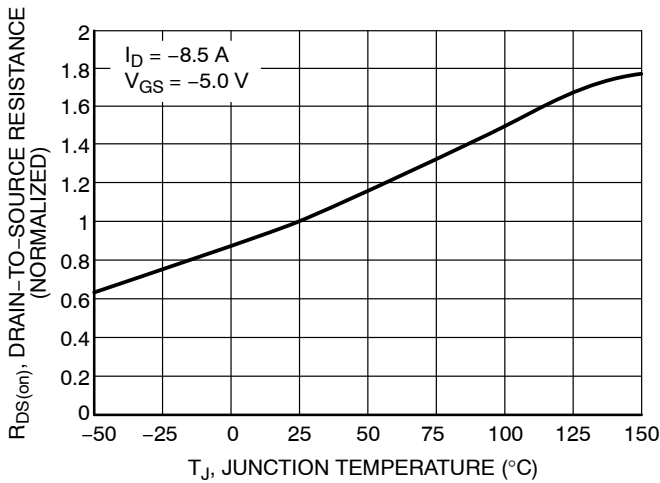


Figure 5. On-Resistance Variation with Temperature

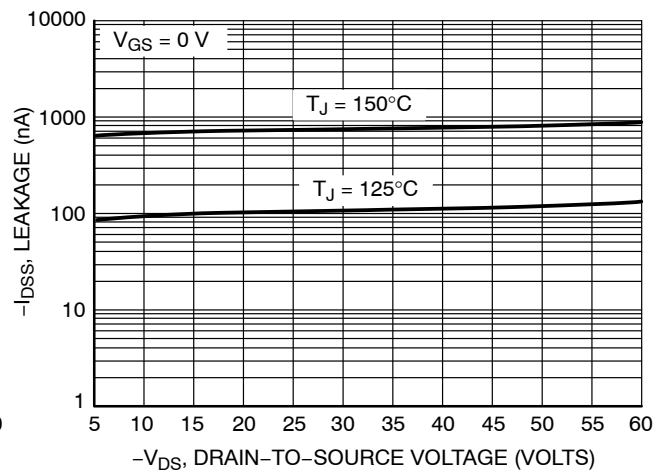


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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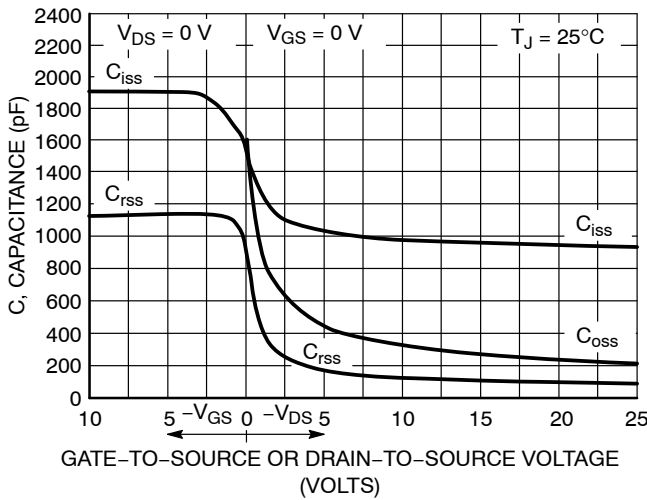


Figure 7. Capacitance Variation

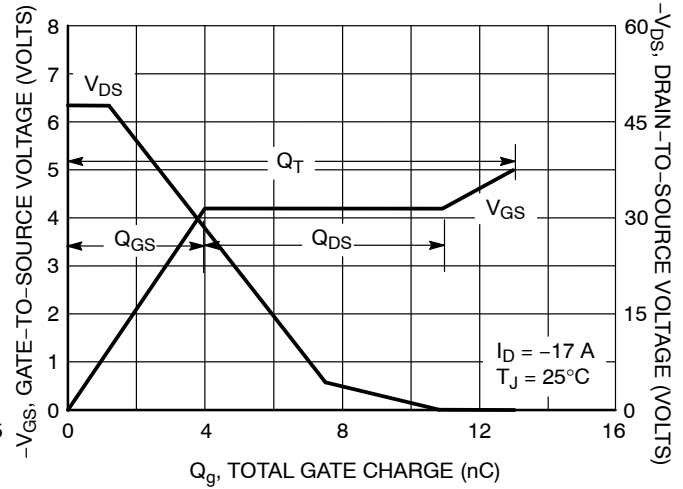


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

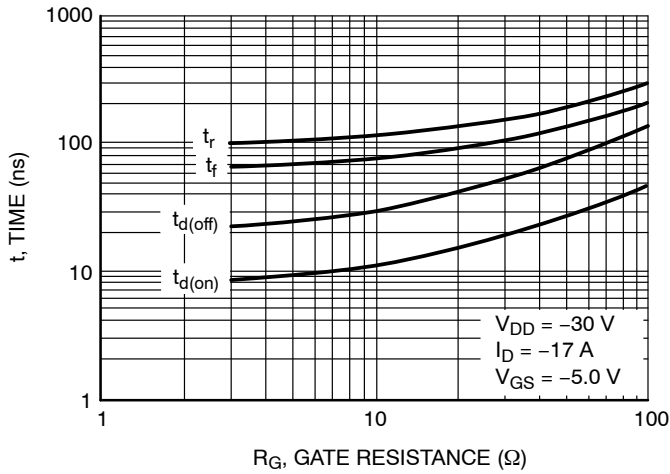


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

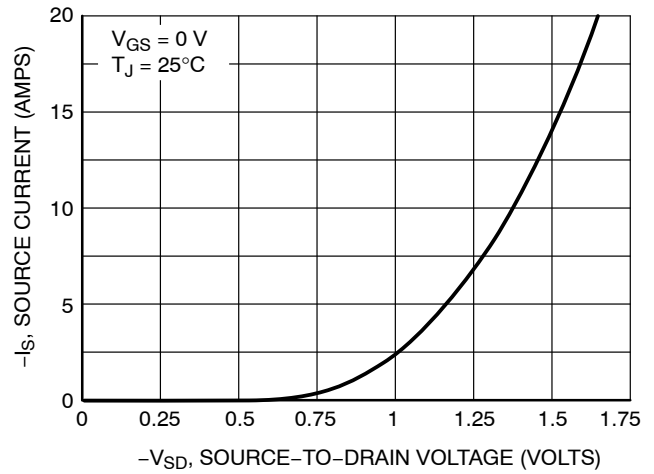


Figure 10. Diode Forward Voltage vs. Current

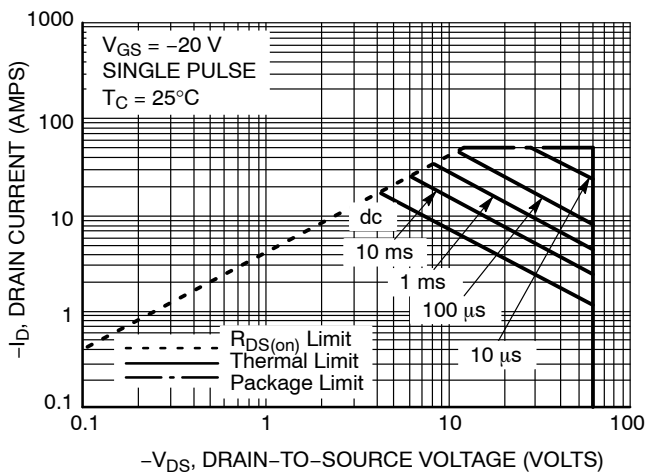


Figure 11. Maximum Rated Forward Biased Safe Operating Area

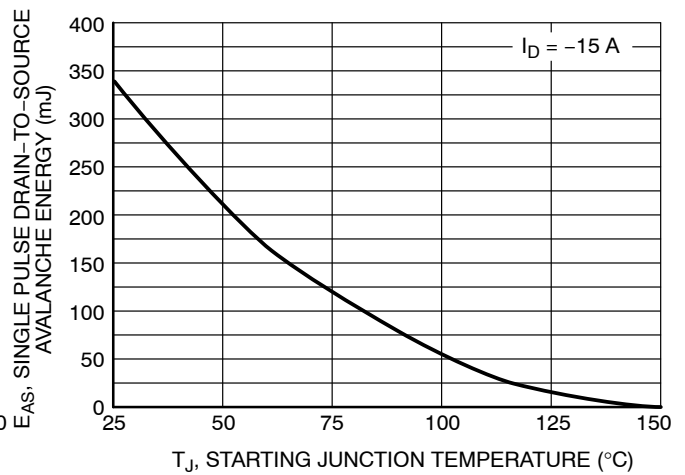


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

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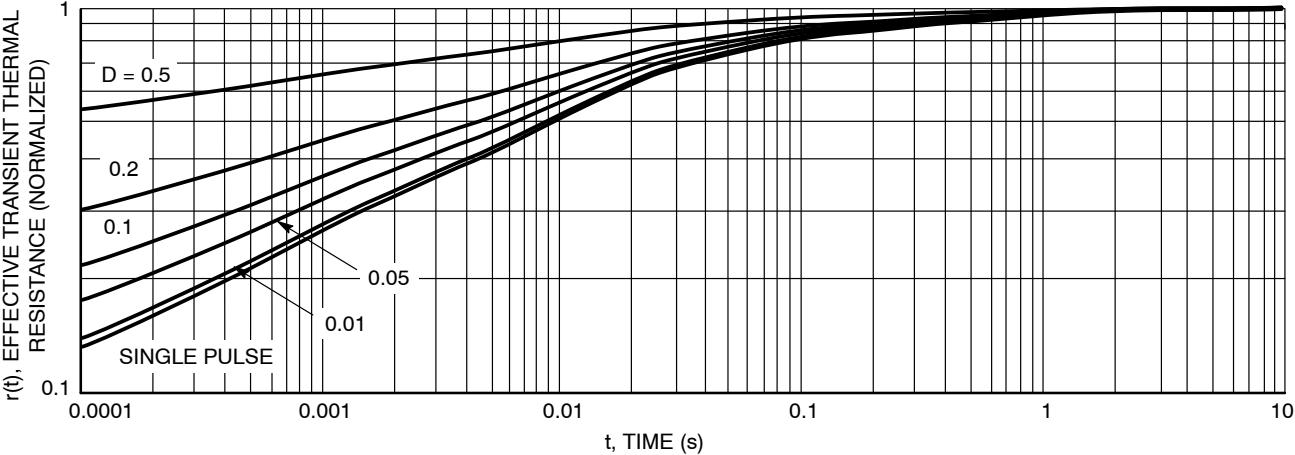


Figure 13. Thermal Response

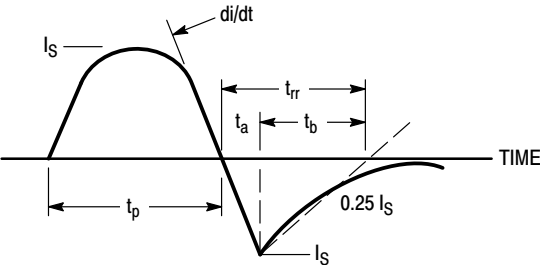
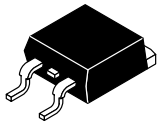


Figure 14. Diode Reverse Recovery Waveform

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

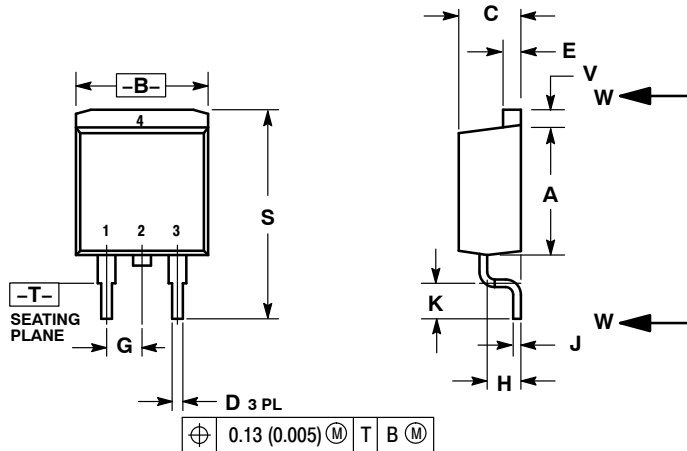
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D²PAK 3
CASE 418B-04
ISSUE L

DATE 17 FEB 2015

SCALE 1:1

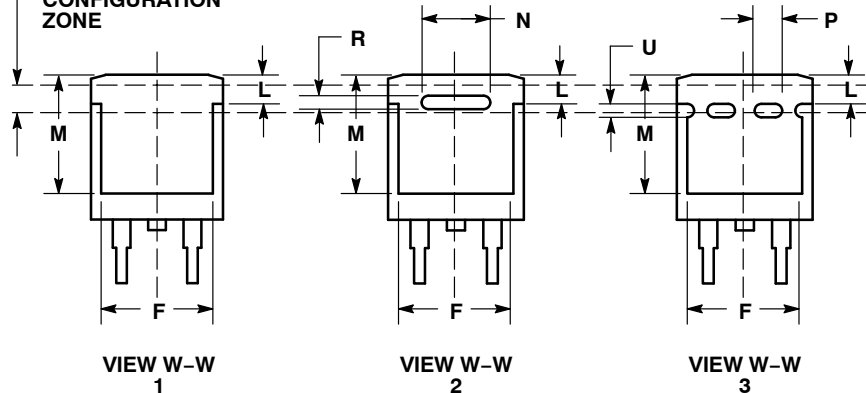


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100	BSC	2.54	BSC
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197	REF	5.00	REF
P	0.079	REF	2.00	REF
R	0.039	REF	0.99	REF
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

VARIABLE CONFIGURATION ZONE



- | | | | | | |
|--|---|---|--|---|--|
| STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN | STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE | STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 5:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE | STYLE 6:
PIN 1. NO CONNECT
2. CATHODE
3. ANODE
4. CATHODE |
|--|---|---|--|---|--|

MARKING INFORMATION AND FOOTPRINT ON PAGE 2

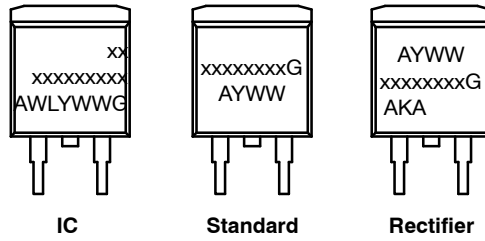
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ISSUE L

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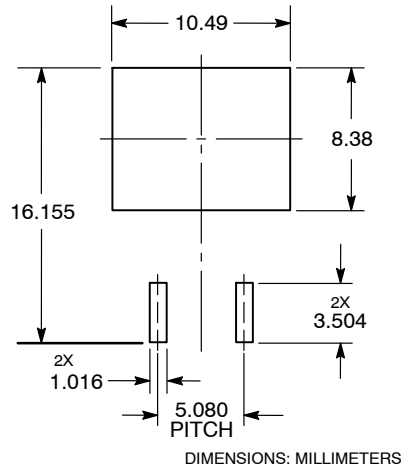
**GENERIC
MARKING DIAGRAM***



- xx = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package
- AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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