MOSFET - Power, N-Channel, DPAK
20 A, 30 V
NTD20N03L27, NVD20N03L27

20 A, 30 V, $R_{DS(on)}$ = 27 mΩ

This logic level vertical power MOSFET is a general purpose part that provides the "best of design" available today in a low cost power package. Avalanche energy issues make this part an ideal design in. The drain−to−source diode has a ideal fast but soft recovery.

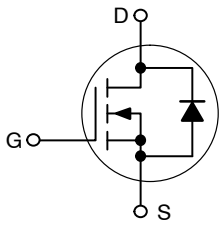
Features

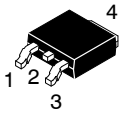
- Ultra−Low $R_{DS(on)}$, Single Base, Advanced Technology
- SPICE Parameters Available
- Diode is Characterized for use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperatures
- High Avalanche Energy Specified
- ESD JEDAC rated HBM Class 1, MM Class A, CDM Class 0
- NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Power Supplies
- Inductive Loads
- PWM Motor Controls
- Replaces MTD20N03L in many Applications

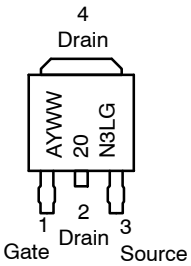
N−Channel





DPAK
CASE 369C
STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENTS



A = Assembly Location*
20N3L = Device Code
Y = Year
WW = Work Week
G = Pb−Free Package

* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	30	Vdc
Drain−to−Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	30	Vdc
Gate−to−Source Voltage − Continuous − Non−Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GS}	±20 ±24	Vdc
Drain Current − Continuous @ T_A = 25°C − Continuous @ T_A = 100°C − Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	20 16 60	Adc Apk
Total Power Dissipation @ T_A = 25°C Derate above 25°C Total Power Dissipation @ T_C = 25°C (Note 1)	P_D	74 0.6 1.75	W W/°CW
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = 30 Vdc, V_{GS} = 5 Vdc, L = 1.0 mH, $I_{L(pk)}$ = 24 A, V_{DS} = 34 Vdc)	E_{AS}	288	mJ
Thermal Resistance − Junction−to−Case − Junction−to−Ambient − Junction−to−Ambient (Note 1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.67 100 71.4	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using the minimum recommended pad size and repetitive rating; pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain−to−Source Breakdown Voltage (Note 2) (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)	$V_{(BR)DSS}$	 30 –	 – 43	 – –	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 30 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 30 Vdc, V_{GS} = 0 Vdc, T_J =150°C)	I_{DSS}	 – –	 – –	 10 100	μAdc
Gate−Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	–	–	±100	nAdc
ON CHARACTERISTICS (Note 2)					
Gate Threshold Voltage (Note 2) (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)	$V_{GS(th)}$	 1.0 –	 1.6 5.0	 2.0 –	Vdc mV/°C
Static Drain−to−Source On−Resistance (Note 2) (V_{GS} = 4.0 Vdc, I_D = 10 Adc) (V_{GS} = 5.0 Vdc, I_D = 10 Adc)	$R_{DS(on)}$	 – –	 28 23	 31 27	mΩ
Static Drain−to−Source On−Voltage (Note 2) (V_{GS} = 5.0 Vdc, I_D = 20 Adc) (V_{GS} = 5.0 Vdc, I_D = 10 Adc, T_J = 150°C)	$V_{DS(on)}$	 – –	 0.48 0.40	 0.54 –	Vdc
Forward Transconductance (Note 2) (V_{DS} = 5.0 Vdc, I_D = 10 Adc)	g_{FS}	–	21	–	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	–	1005	1260	pF
Output Capacitance		C_{oss}	–	271	420	
Transfer Capacitance		C_{rss}	–	87	112	
SWITCHING CHARACTERISTICS (Note 3)						
Turn−On Delay Time	(V_{DD} = 20 Vdc, I_D = 20 Adc, V_{GS} = 5.0 Vdc, R_G = 9.1 Ω) (Note 2)	$t_{d(on)}$	–	17	25	ns
Rise Time		t_r	–	137	160	
Turn−Off Delay Time		$t_{d(off)}$	–	38	45	
Fall Time		t_f	–	31	40	
Gate Charge	(V_{DS} = 48 Vdc, I_D = 15 Adc, V_{GS} = 10 Vdc) (Note 2)	Q_T	–	13.8	18.9	nC
		Q_1	–	2.8	–	
		Q_2	–	6.6	–	
SOURCE−DRAIN DIODE CHARACTERISTICS						
Forward On−Voltage	(I_S = 20 Adc, V_{GS} = 0 Vdc) (Note 2) (I_S = 20 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	 – –	 1.0 0.9	 1.15 –	Vdc
Reverse Recovery Time	(I_S =15 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (Note 2)	t_{rr}	–	23	–	ns
		t_a	–	13	–	
		t_b	–	10	–	
Reverse Recovery Stored Charge		Q_{RR}	–	0.017	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

ORDERING INFORMATION

Device	Package	Shipping†
NTD20N03L27T4G	DPAK (Pb−Free)	2500 / Tape & Reel
NVD20N03L27T4G*	DPAK (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable.

TYPICAL CHARACTERISTICS

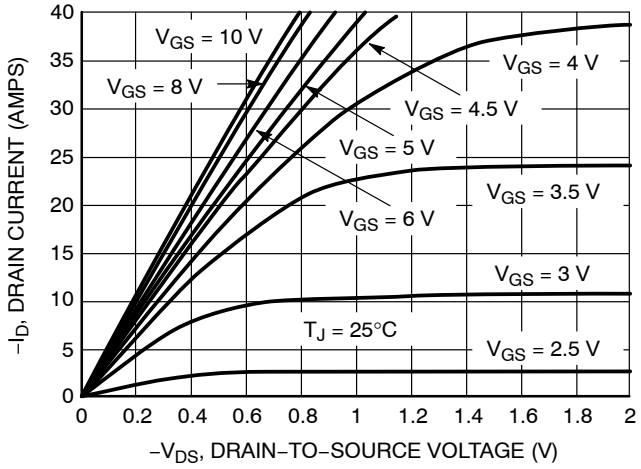


Figure 1. On−Region Characteristics

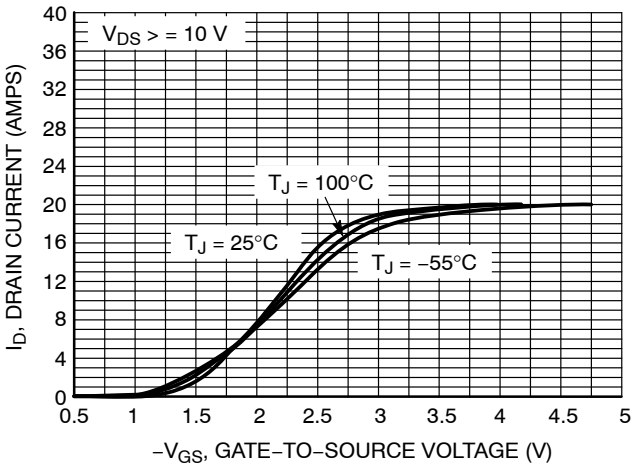


Figure 2. Transfer Characteristics

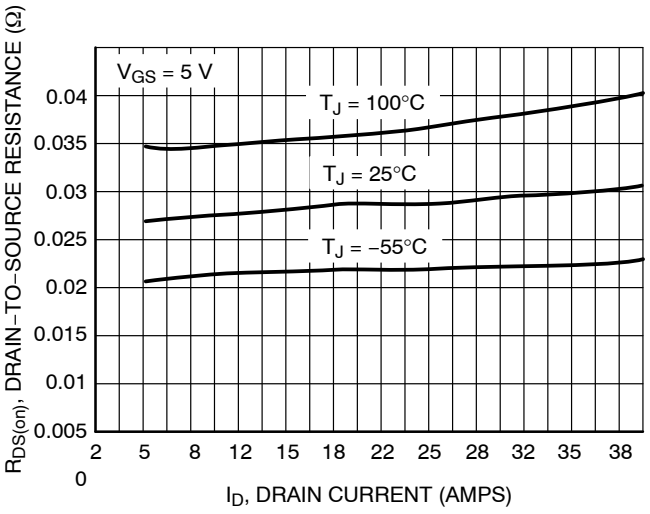


Figure 3. On−Resistance vs. Drain Current and Temperature

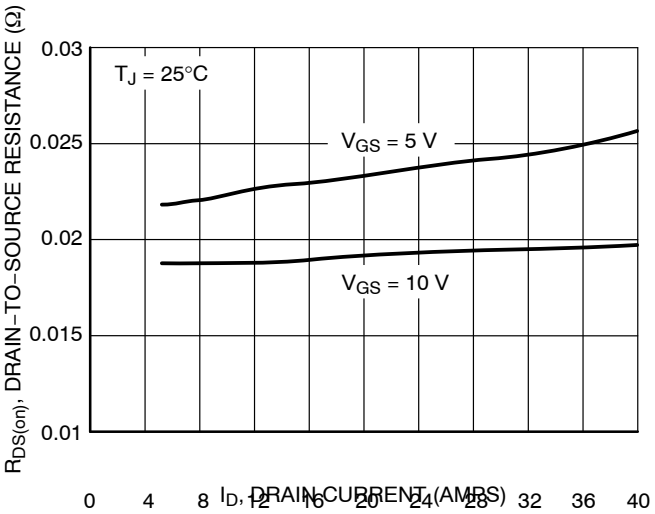


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

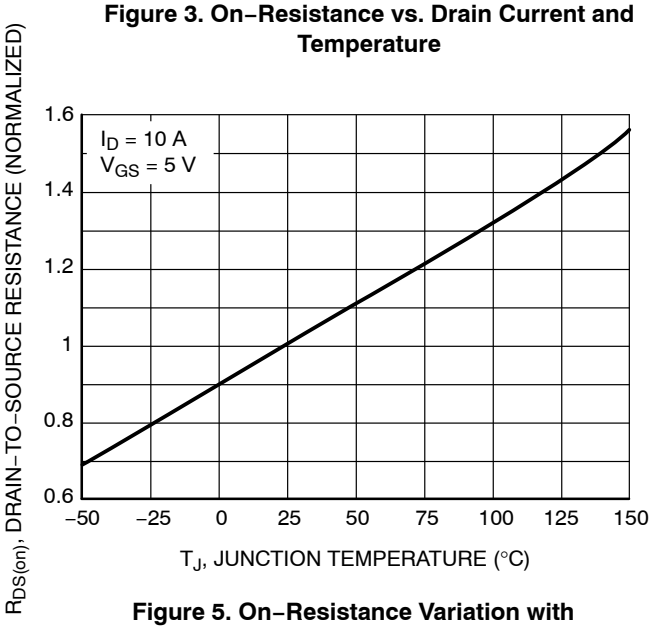


Figure 5. On−Resistance Variation with Temperature

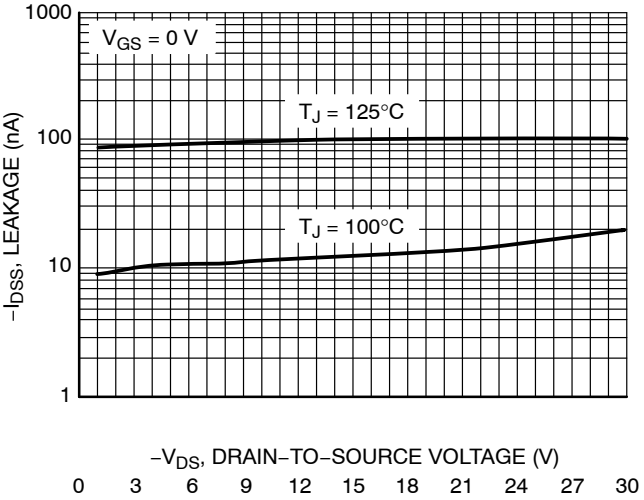


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

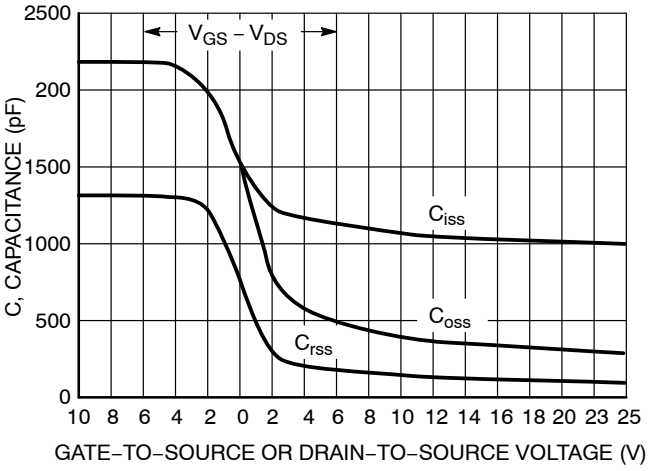


Figure 7. Capacitance Variation

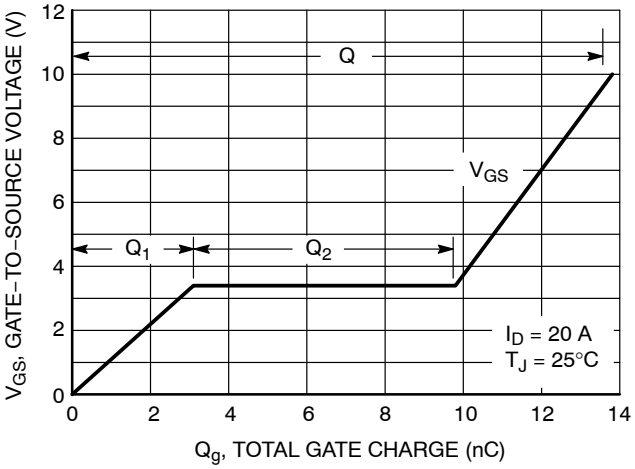


Figure 8. Gate–to–Source and Drain–to–Source Voltage vs. Total Charge

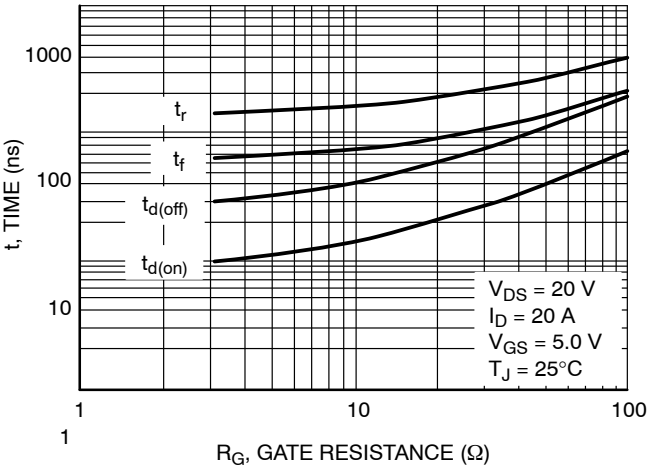


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

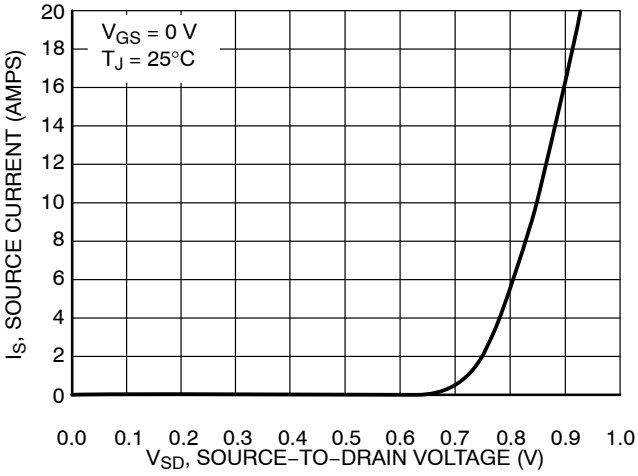


Figure 10. Diode Forward Voltage vs. Current

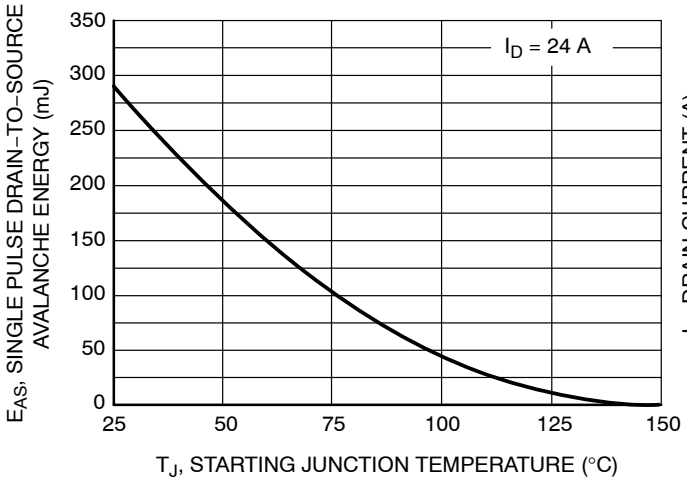


Figure 11. Maximum Avalanche Energy vs. Starting Junction Temperature

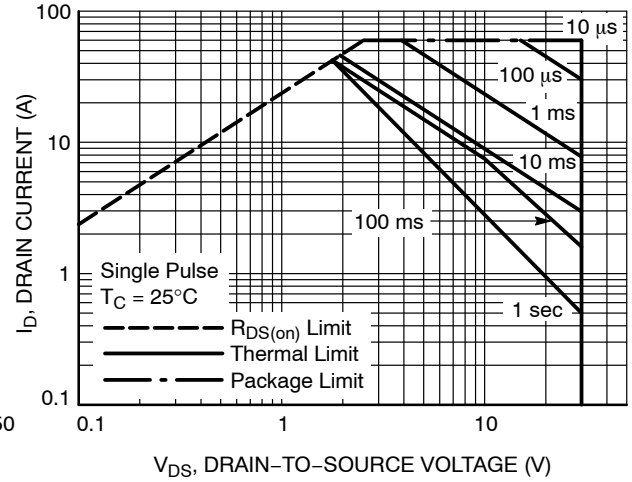


Figure 12. Safe Operating Area

TYPICAL CHARACTERISTICS

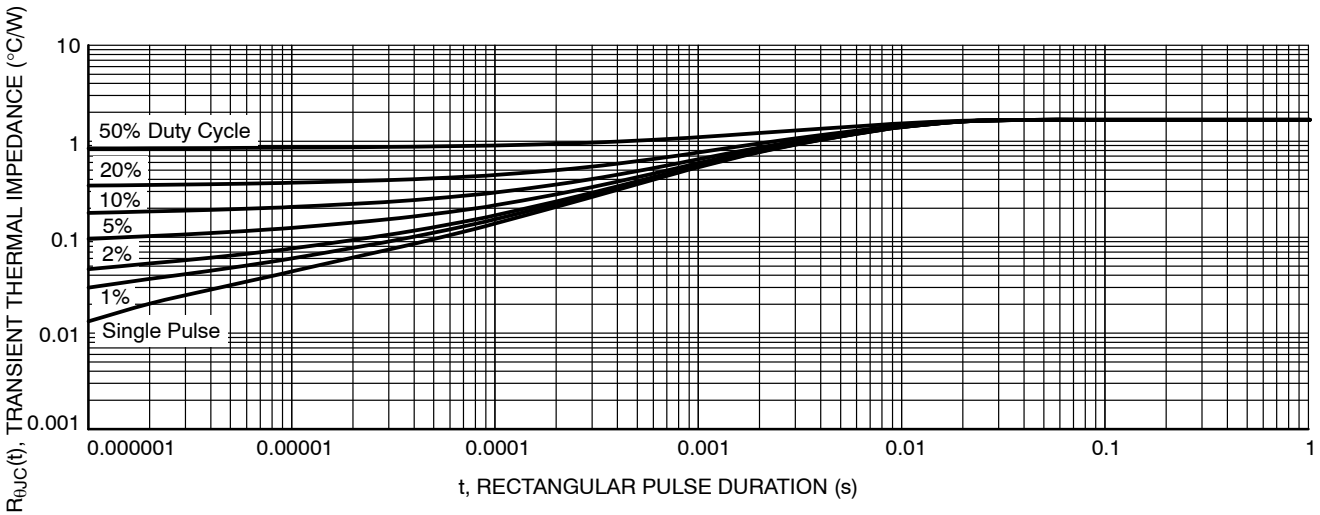
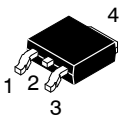


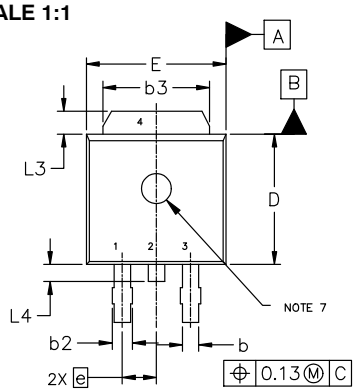
Figure 13. Thermal Response



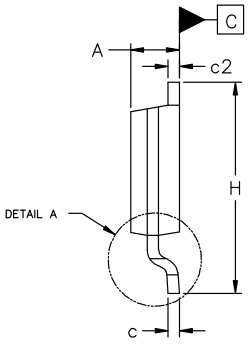
SCALE 1:1

DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE J

DATE 12 AUG 2025

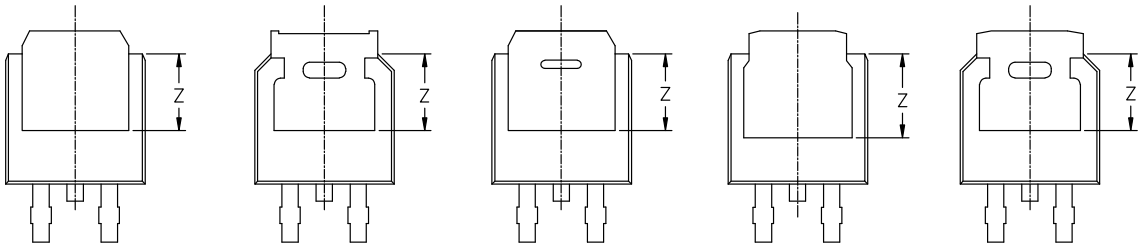


TOP VIEW



SIDE VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---

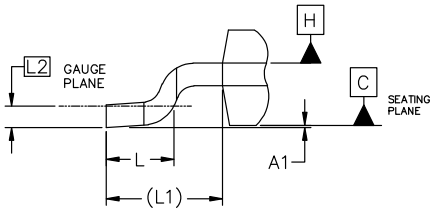


BOTTOM VIEW

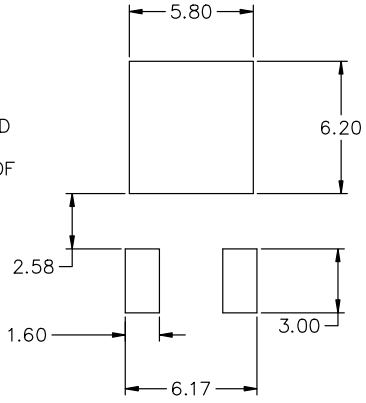
ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



DETAIL A
ROTATED 90° CW



RECOMMENDED MOUNTING FOOTPRINT*

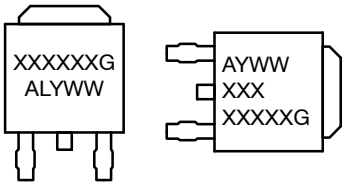
*FOR ADDITIONAL INFORMATION ON OUR PB–FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON10527D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**DPAK3 6.10x6.54x2.28, 2.29P**	**PAGE 1 OF 2**

DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE J

DATE 12 AUG 2025

GENERIC MARKING DIAGRAM*



IC **Discrete**

XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales