NTGS3A033PZ

MOSFET – Power, Single, P-Channel, TSOP-6
-20 V, -5.9 A

ON Semiconductor®

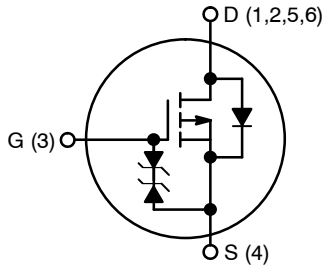
www.onsemi.com

$V_{(BR)DSS}$	$R_{DS(on)}$ Typ	I_D MAX
−20 V	22 mΩ @ −4.5 V	−5.9 A
	29 mΩ @ −2.5 V	
	40 mΩ @ −1.8 V	

Features
- Leading −20 V Trench for Low $R_{DS(on)}$
- −1.8 V Rated for Low Voltage Gate Drive
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications
- Power Load Switch
- High Side Load Switch
- Charging Circuits and Battery Protection

P−Channel MOSFET



MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	−20	V
Gate−to−Source Voltage			V_{GS}	±8	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	−5.1	A
		T_A = 85°C		−3.7	
	t ≤ 5 s	T_A = 25°C		−5.9	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	1.19	W
	t ≤ 5 s			1.58	
Continuous Drain Current (Note 2)	Steady State	T_A = 25°C	I_D	−3.8	A
		T_A = 85°C		−2.7	
Power Dissipation (Note 2)		T_A = 25°C	P_D	0.65	W
Pulsed Drain Current	t_p = 10 μs		I_{DM}	−20	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Lead Temperature for Soldering Purposes (1/8 in from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

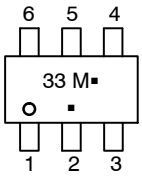
Parameter	Symbol	Max	Unit
Junction−to−Ambient – Steady State (Note 1)	$R_{\theta JA}$	105	°C/W
Junction−to−Ambient – t ≤ 5 s (Note 1)	$R_{\theta JA}$	79	
Junction−to−Ambient – Steady State (Note 2)	$R_{\theta JA}$	192	

1. Surface−mounted on FR4 board using 1 in sq. pad size (Cu area = 1.127 in sq., 2 oz).
2. Surface−mounted on FR4 board using minimum pad size (Cu area = 0.0775 in sq.).

1

TSOP−6
CASE 318G

MARKING DIAGRAM



33 = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTGS3A033PZT1G	TSOP−6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

© Semiconductor Components Industries, LLC, 2016

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 μA		−20			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = −250 μA, ref to 25°C			21		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = −20 V	T_J = 25°C			−1	μA
			T_J = 85°C			−10	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8 V				±10	μA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = −250 μA		−0.4		−1.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				3		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = −4.5 V	I_D = −5.1 A		22	33	mΩ
		V_{GS} = −2.5 V	I_D = −4.5 A		29	40	
		V_{GS} = −1.8 V	I_D = −1.5 A		40	55	
Forward Transconductance	g_{FS}	V_{DS} = −5 V, I_D = −5.1 A			23		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = −10 V			1870		pF
Output Capacitance	C_{oss}				203		
Reverse Transfer Capacitance	C_{rss}				174		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −4.5 V, V_{DS} = −10 V, I_D = −5.1 A			18.8		nC
Threshold Gate Charge	$Q_{G(TH)}$				1.0		
Gate−to−Source Charge	Q_{GS}				2.7		
Gate−to−Drain Charge	Q_{GD}				5.0		
SWITCHING CHARACTERISTICS (Note 4)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = −4.5 V, V_{DS} = −10 V, I_D = −1.0 A, R_G = 6.0 Ω			9.4		ns
Rise Time	t_r				9.3		
Turn−Off Delay Time	$t_{d(off)}$				131		
Fall Time	t_f				56		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = −1.7 A	T_J = 25°C		−0.7	−1.2	V
			T_J = 125°C		−0.6		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_{SD}/dt = 100 A/μs, I_S = −1.7 A			26		ns
Charge Time	t_a				9.0		
Discharge Time	t_b				17		
Reverse Recovery Charge	Q_{RR}				11		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width ≤ 300 ms, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

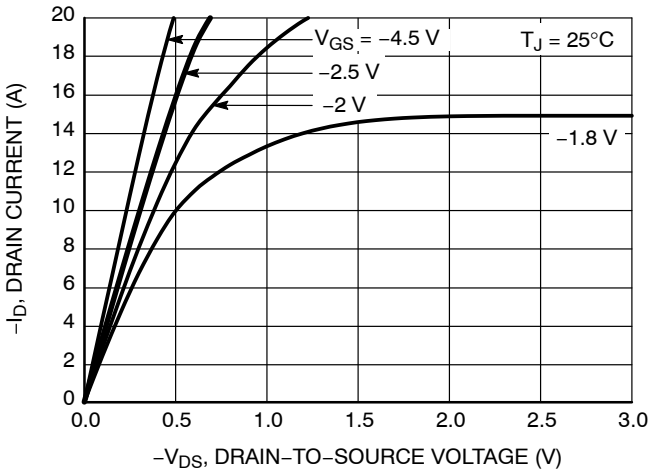


Figure 1. On−Region Characteristics

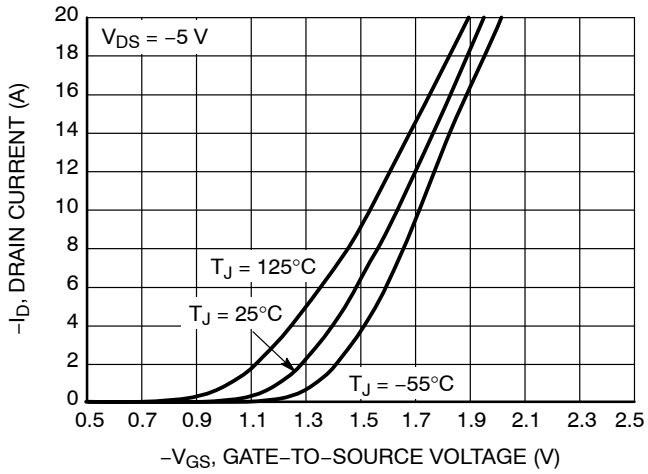


Figure 2. Transfer Characteristics

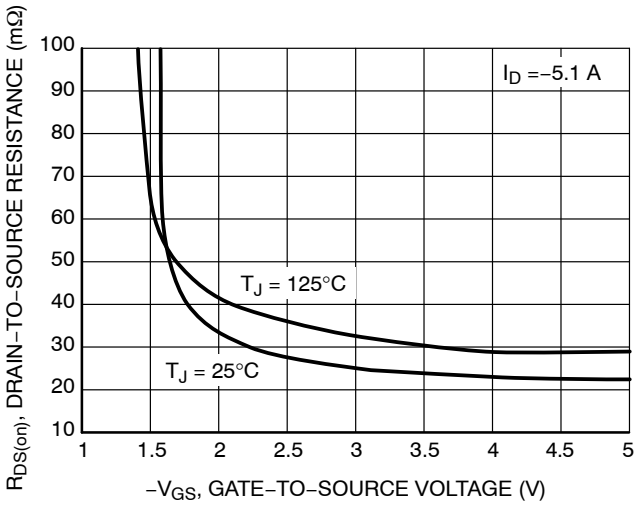


Figure 3. On−Resistance vs. Gate−to−Source Voltage

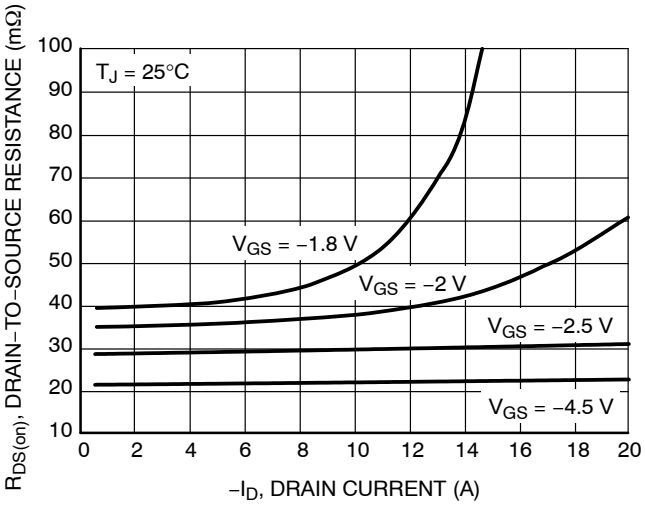


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

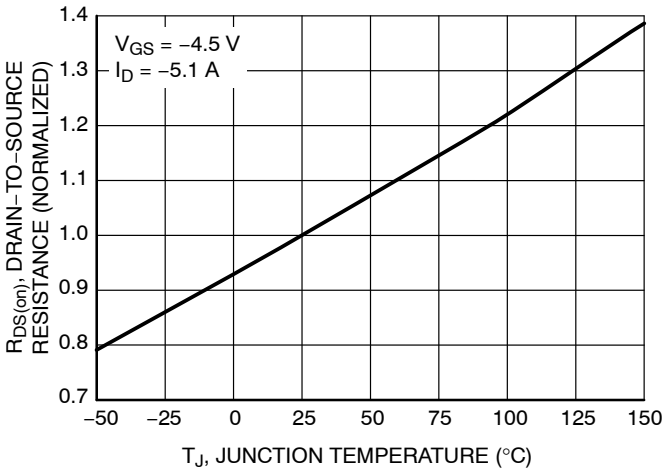


Figure 5. On−Resistance Variation with Temperature

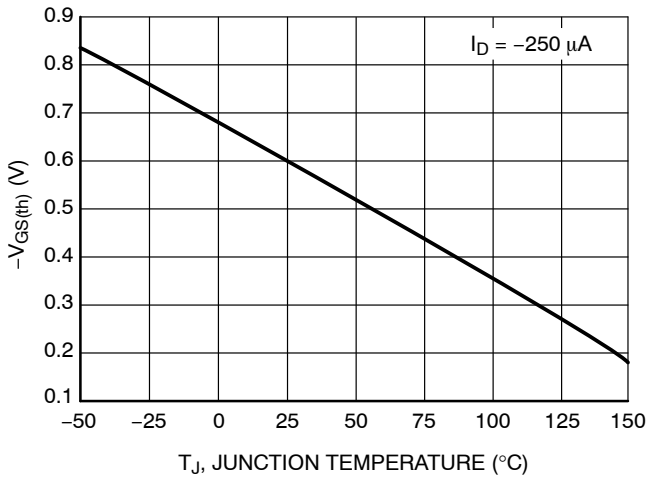


Figure 6. Threshold Voltage Variation with Temperature

TYPICAL CHARACTERISTICS

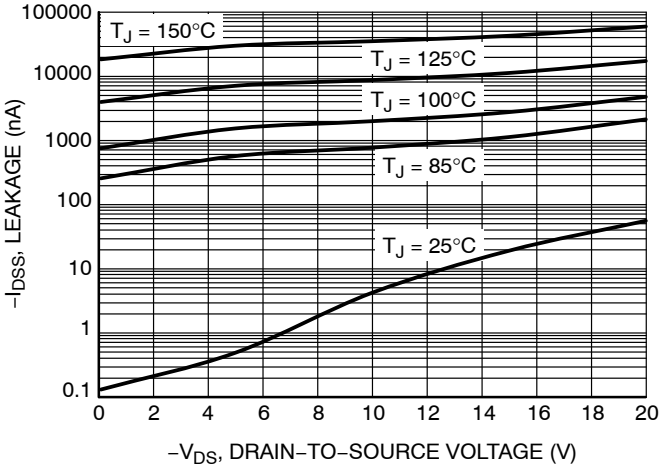


Figure 7. Drain−to−Source Leakage Current vs. Voltage

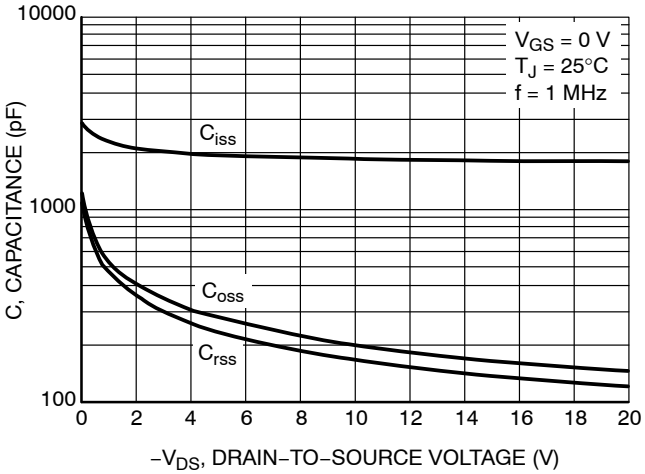


Figure 8. Capacitance Variation

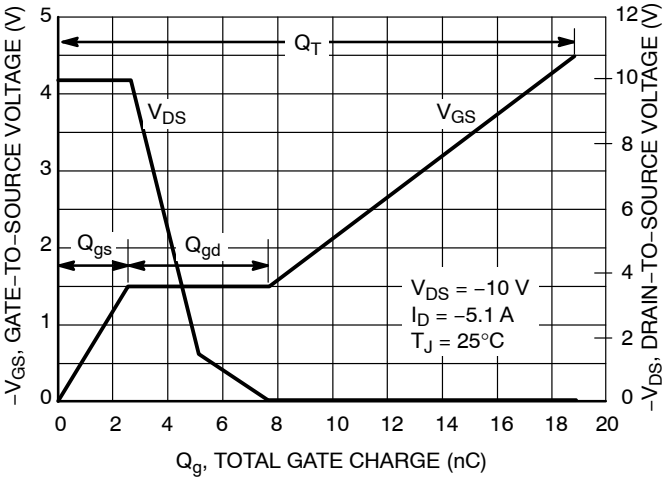


Figure 9. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

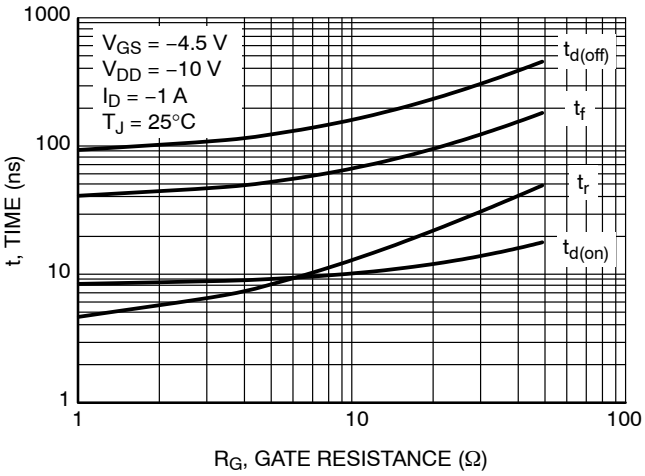


Figure 10. Resistive Switching Time Variation vs. Gate Resistance

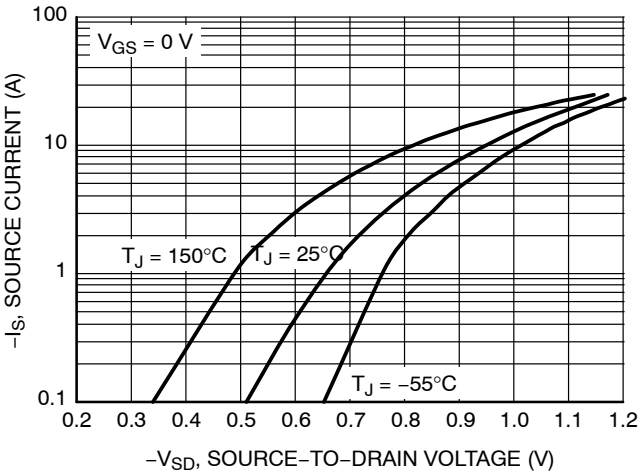


Figure 11. Diode Forward Voltage vs. Current

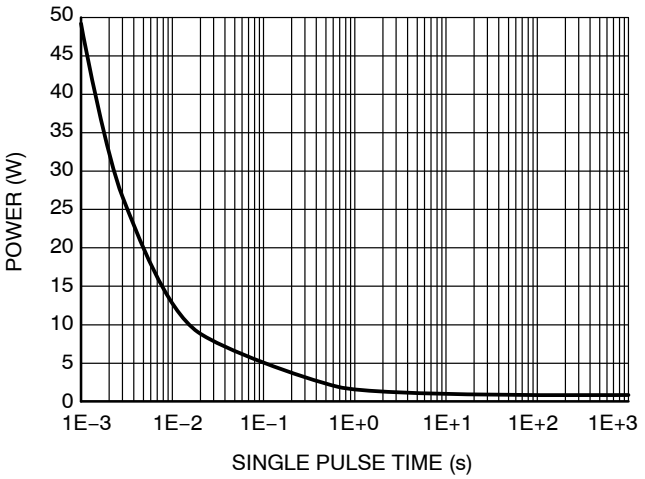


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS

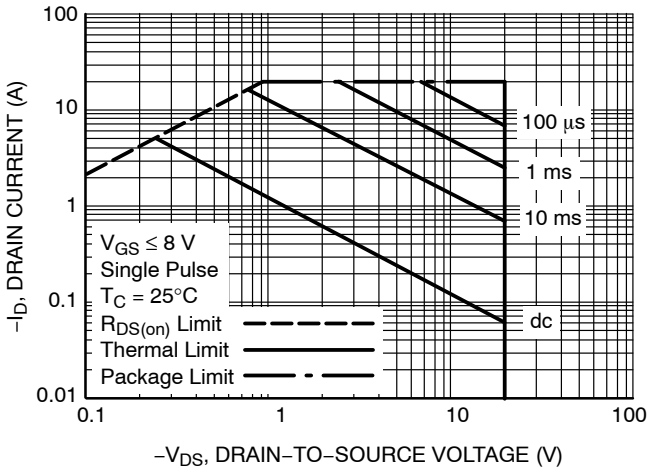


Figure 13. Maximum Rated Forward Biased Safe Operating Area

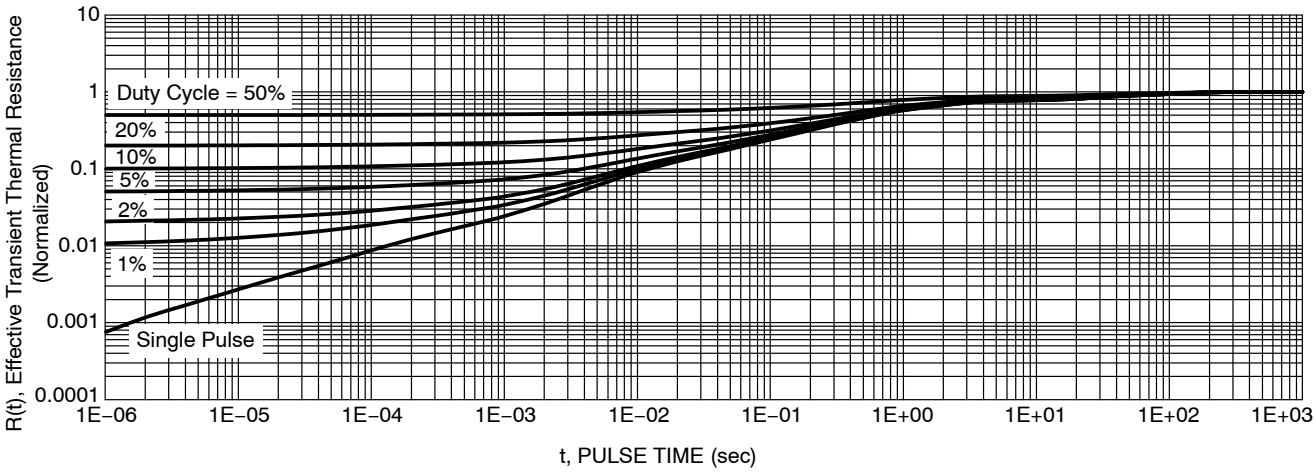
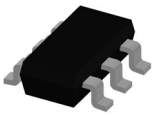
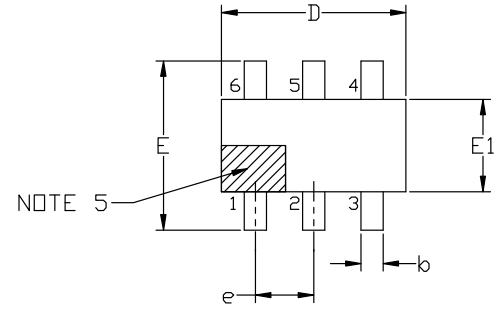


Figure 14. Thermal Response



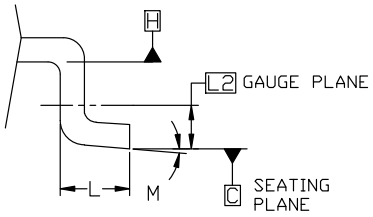
TSOP−6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

DATE 26 FEB 2024

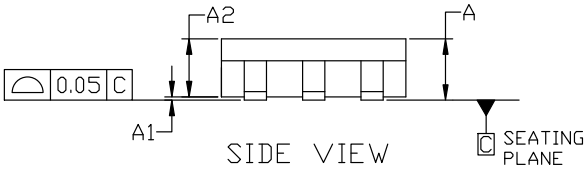


TOP VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE

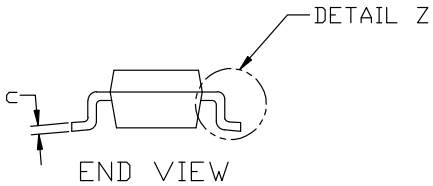


DETAIL Z
SCALE 3:1

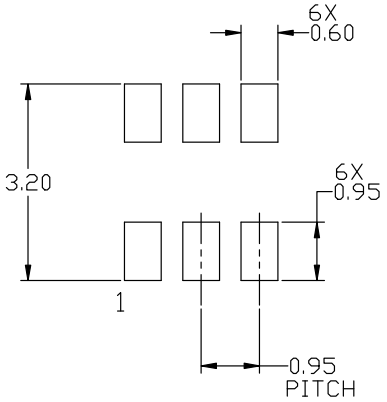


SIDE VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	---	10°



END VIEW



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download th e ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

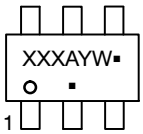
DOCUMENT NUMBER:	**98ASB14888C**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**TSOP−6 3.00x1.50x0.90, 0.95P**	**PAGE 1 OF 2**

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

TSOP−6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

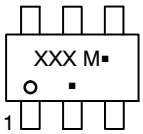
DATE 26 FEB 2024

GENERIC MARKING DIAGRAM*



IC

XXX = Specific Device Code
A =Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package



STANDARD

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

DOCUMENT NUMBER:	98ASB14888C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	TSOP−6 3.00x1.50x0.90, 0.95P	PAGE 2 OF 2

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, onsemi, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales