

NTMD6N04, NVMD6N04

MOSFET – Power, Dual N-Channel, SOIC-8 40 V, 5.8 A

Features

- Designed for use in low voltage, high speed switching applications
- Ultra Low On-Resistance Provides Higher Efficiency and Extends Battery Life
 - $R_{DS(on)} = 0.027 \Omega$, $V_{GS} = 10 \text{ V}$ (Typ)
 - $R_{DS(on)} = 0.034 \Omega$, $V_{GS} = 4.5 \text{ V}$ (Typ)
- Miniature SOIC-8 Surface Mount Package Saves Board Space
- Diode is Characterized for Use in Bridge Circuits
- Diode Exhibits High Speed, with Soft Recovery
- NVMD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable*
- These Devices are Pb-Free and are RoHS Compliant

Applications

- DC-DC Converters
- Computers
- Printers
- Cellular and Cordless Phones
- Disk Drives and Tape Drives

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	40	V
Gate-to-Source Voltage – Continuous	V_{GS}	± 20	V
Drain Current (Note 1)	I_D	5.8	Adc
– Continuous @ $T_A = 25^\circ\text{C}$			
– Single Pulse ($t_p \leq 10 \mu\text{s}$)	I_{DM}	29	Apk
Drain Current (Note 2)	I_D	4.6	Adc
– Continuous @ $T_A = 25^\circ\text{C}$			
Total Power Dissipation	P_D		W
@ $T_A = 25^\circ\text{C}$ (Note 1)		2.0	
@ $T_A = 25^\circ\text{C}$ (Note 2)		1.29	
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 40 \text{ Vdc}$, $V_{GS} = 5.0 \text{ Vdc}$, V_{dc} , Peak $I_L = 7.0 \text{ Apk}$, $L = 10 \text{ mH}$, $R_G = 25 \Omega$)	E_{AS}	245	mJ
Thermal Resistance	$R_{\theta JA}$		$^\circ\text{C/W}$
– Junction-to-Ambient (Note 1)		62.5	
– Junction-to-Ambient (Note 2)		97	
Maximum Lead Temperature for Soldering Purposes for 10 Sec	T_L	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. When surface mounted to an FR4 board using 1" pad size, $t \leq 10 \text{ s}$

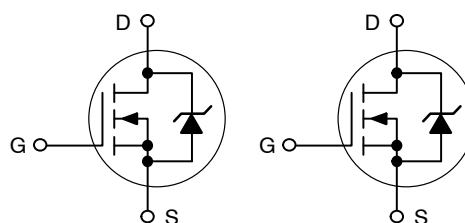


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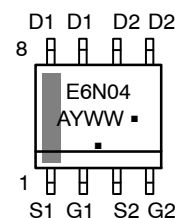
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V_{DSS}	$R_{DS(on)}$ Typ	I_D Max
40 V	27 m Ω @ $V_{GS} = 10 \text{ V}$	5.8 A

N-Channel



MARKING DIAGRAM & PIN ASSIGNMENT



E6N04 = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTMD6N04R2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
NVMD6N04R2G*	SOIC-8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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2. When surface mounted to an FR4 board using 1" pad size, $t = \text{steady state}$

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 250 μA) Temperature Coefficient (Positive)	$V_{(BR)DSS}$ $V_{(BR)DSS}/T_J$	40 -	47 45	- -	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{DS} = 40 Vdc, V _{GS} = 0 Vdc, T _J = 25°C) (V _{DS} = 40 Vdc, V _{GS} = 0 Vdc, T _J = 125°C)	I _{DSS}	- -	- -	1.0 10	μAdc
Gate-Body Leakage Current (V _{GS} = ±20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	-	-	± 100	nAdc

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 250 μAdc) Temperature Coefficient (Negative)	$V_{GS(th)}$ $V_{GS(th)}/T_J$	1.0 -	1.9 4.7	3.0 -	Vdc mV/°C
Static Drain-to-Source On-State Resistance (V _{GS} = 10 Vdc, I _D = 5.8 Adc) (V _{GS} = 4.5 Vdc, I _D = 3.9 Adc)	R _{DS(on)}	- -	0.027 0.034	0.034 0.043	Ω
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 5.8 Adc)	g _{FS}	-	8.12	-	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 32 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{iss}	-	723	900	pF
Output Capacitance		C _{oss}	-	156	225	
Reverse Transfer Capacitance		C _{rss}	-	53	75	

SWITCHING CHARACTERISTICS (Notes 3 & 4)

Turn-On Delay Time	(V _{DD} = 20 Vdc, I _D = 5.8 A, V _{GS} = 10 V, R _G = 6 Ω)	t _{d(on)}	-	10	18	ns
Rise Time		t _r	-	20	35	
Turn-Off Delay Time		t _{d(off)}	-	45	70	
Fall Time		t _f	-	40	65	
Turn-On Delay Time	(V _{DD} = 20 Vdc, I _D = 5.8 A, V _{GS} = 4.5 V, R _G = 6 Ω)	t _{d(on)}	-	15	-	ns
Rise Time		t _r	-	55	-	
Turn-Off Delay Time		t _{d(off)}	-	30	-	
Fall Time		t _f	-	35	-	
Gate Charge	(V _{DS} = 20 Vdc, V _{GS} = 10 Vdc, I _D = 5.8 A)	Q _T	-	20	30	nC
		Q _{gs}	-	2.5	-	
		Q _{gd}	-	5.5	-	

BODY-DRAIN DIODE RATINGS (Note 3)

Diode Forward On-Voltage	(I _S = 1.7 Adc, V _{GS} = 0 V) (I _S = 1.7 Adc, V _{GS} = 0 V, T _J = 150°C)	V _{SD}	- -	0.76 0.56	1.1 -	Vdc
Reverse Recovery Time	(I _S = 1.7 A, V _{GS} = 0 V, di _S /dt = 100 A/μs)	t _{rr}	-	23	-	ns
		t _a	-	16	-	
		t _b	-	7	-	
Reverse Recovery Stored Charge (I _S = 1.7 A, di _S /dt = 100 A/μs, V _{GS} = 0 V)		Q _{RR}	-	20	-	nC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperature.

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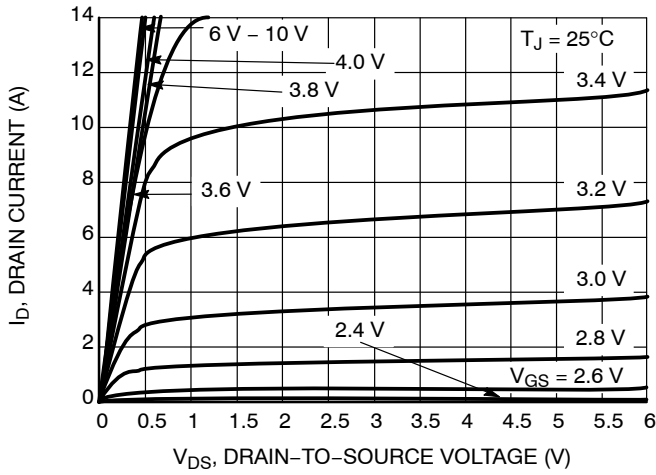


Figure 1. On-Region Characteristics

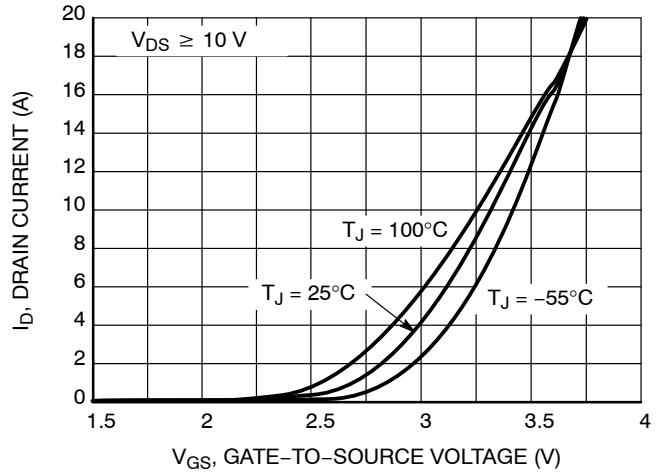


Figure 2. Transfer Characteristics

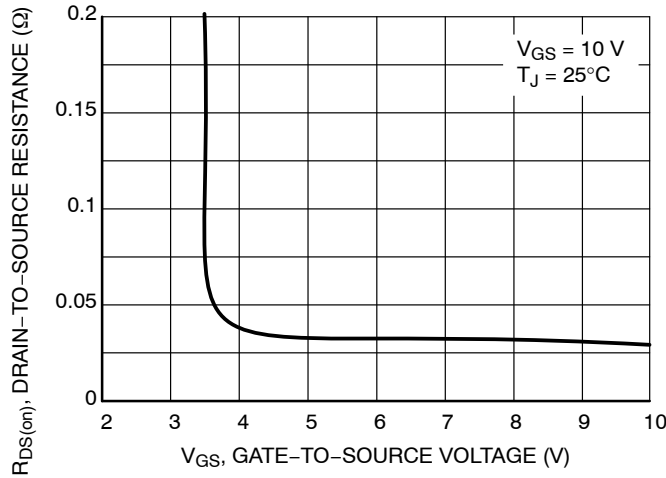


Figure 3. On-Resistance vs. Gate-to-Source Voltage

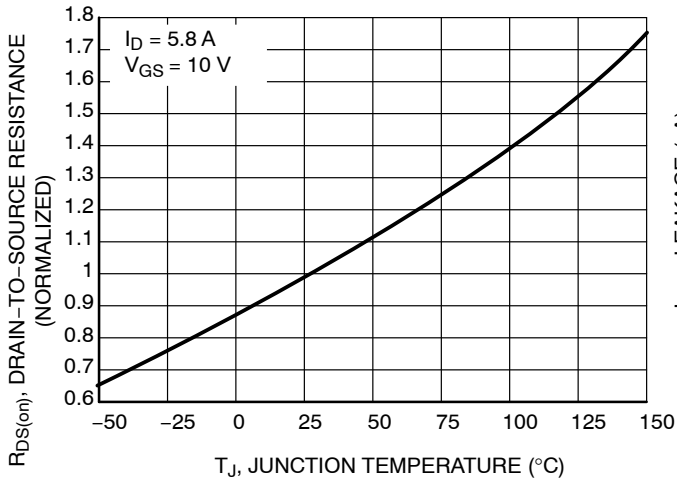


Figure 4. On Resistance Variation with Temperature

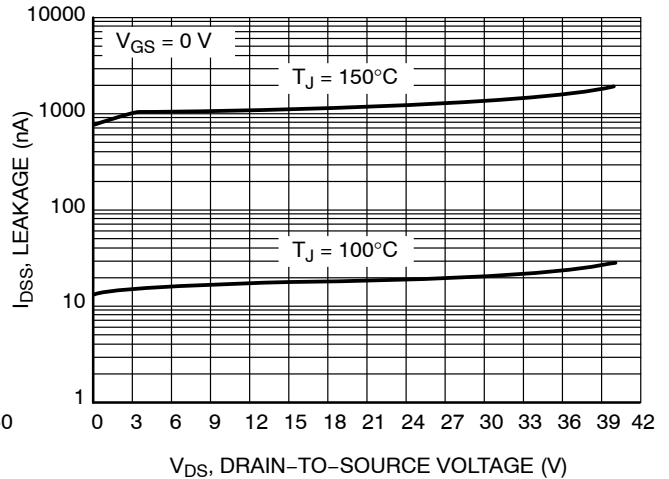


Figure 5. Drain-to-Source Leakage Current vs. Voltage

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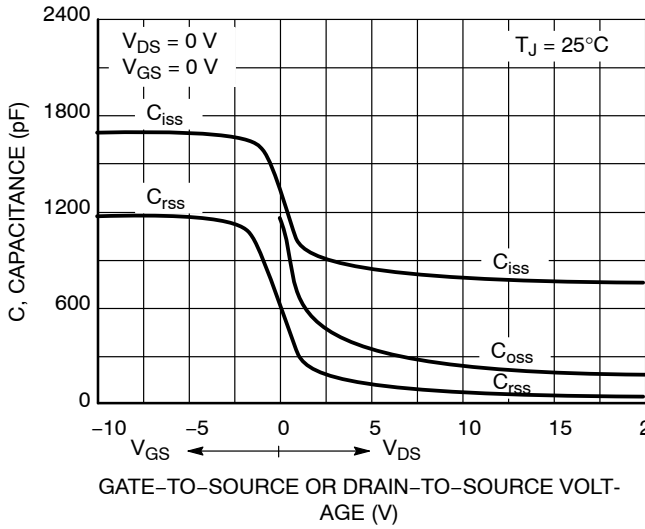


Figure 6. Capacitance Variation

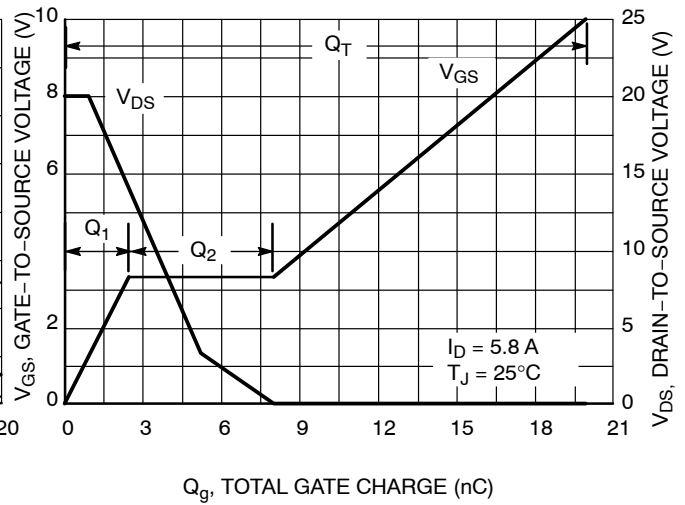


Figure 7. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

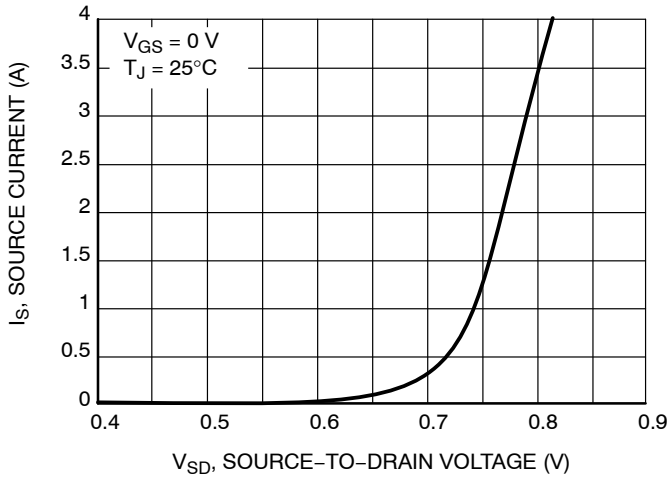


Figure 8. Diode Forward Voltage vs. Current

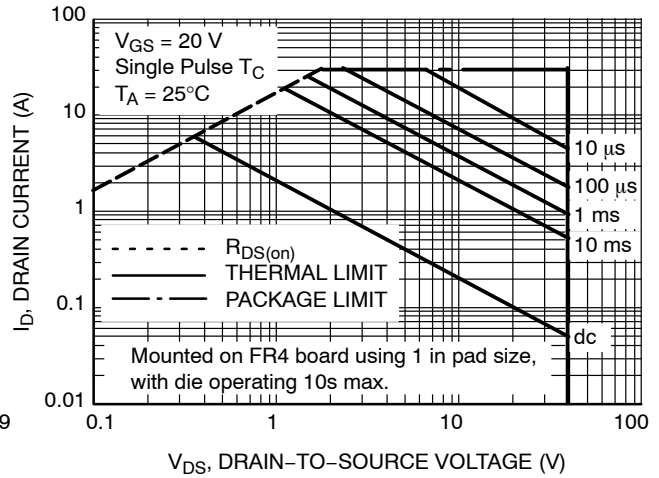


Figure 9. Maximum Rated Forward Biased Safe Operating Area

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

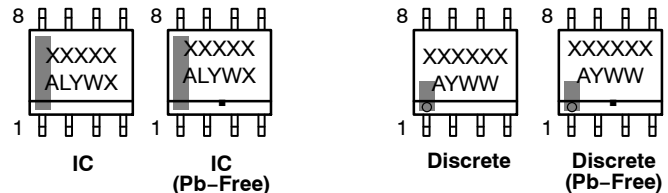
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- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|--|---|---|---|
| <p>STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. COLLECTOR
 4. EMITTER
 5. EMITTER
 6. BASE
 7. BASE
 8. EMITTER</p> | <p>STYLE 2:
 PIN 1. COLLECTOR, DIE, #1
 2. COLLECTOR, #1
 3. COLLECTOR, #2
 4. COLLECTOR, #2
 5. BASE, #2
 6. EMITTER, #2
 7. BASE, #1
 8. EMITTER, #1</p> | <p>STYLE 3:
 PIN 1. DRAIN, DIE #1
 2. DRAIN, #1
 3. DRAIN, #2
 4. DRAIN, #2
 5. GATE, #2
 6. SOURCE, #2
 7. GATE, #1
 8. SOURCE, #1</p> | <p>STYLE 4:
 PIN 1. ANODE
 2. ANODE
 3. ANODE
 4. ANODE
 5. ANODE
 6. ANODE
 7. ANODE
 8. COMMON CATHODE</p> |
| <p>STYLE 5:
 PIN 1. DRAIN
 2. DRAIN
 3. DRAIN
 4. DRAIN
 5. GATE
 6. GATE
 7. SOURCE
 8. SOURCE</p> | <p>STYLE 6:
 PIN 1. SOURCE
 2. DRAIN
 3. DRAIN
 4. SOURCE
 5. SOURCE
 6. GATE
 7. GATE
 8. SOURCE</p> | <p>STYLE 7:
 PIN 1. INPUT
 2. EXTERNAL BYPASS
 3. THIRD STAGE SOURCE
 4. GROUND
 5. DRAIN
 6. GATE 3
 7. SECOND STAGE Vd
 8. FIRST STAGE Vd</p> | <p>STYLE 8:
 PIN 1. COLLECTOR, DIE #1
 2. BASE, #1
 3. BASE, #2
 4. COLLECTOR, #2
 5. COLLECTOR, #2
 6. EMITTER, #2
 7. EMITTER, #1
 8. COLLECTOR, #1</p> |
| <p>STYLE 9:
 PIN 1. EMITTER, COMMON
 2. COLLECTOR, DIE #1
 3. COLLECTOR, DIE #2
 4. EMITTER, COMMON
 5. EMITTER, COMMON
 6. BASE, DIE #2
 7. BASE, DIE #1
 8. EMITTER, COMMON</p> | <p>STYLE 10:
 PIN 1. GROUND
 2. BIAS 1
 3. OUTPUT
 4. GROUND
 5. GROUND
 6. BIAS 2
 7. INPUT
 8. GROUND</p> | <p>STYLE 11:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. DRAIN 2
 7. DRAIN 1
 8. DRAIN 1</p> | <p>STYLE 12:
 PIN 1. SOURCE
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 13:
 PIN 1. N.C.
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> | <p>STYLE 14:
 PIN 1. N-SOURCE
 2. N-GATE
 3. P-SOURCE
 4. P-GATE
 5. P-DRAIN
 6. P-DRAIN
 7. N-DRAIN
 8. N-DRAIN</p> | <p>STYLE 15:
 PIN 1. ANODE 1
 2. ANODE 1
 3. ANODE 1
 4. ANODE 1
 5. CATHODE, COMMON
 6. CATHODE, COMMON
 7. CATHODE, COMMON
 8. CATHODE, COMMON</p> | <p>STYLE 16:
 PIN 1. EMITTER, DIE #1
 2. BASE, DIE #1
 3. EMITTER, DIE #2
 4. BASE, DIE #2
 5. COLLECTOR, DIE #2
 6. COLLECTOR, DIE #2
 7. COLLECTOR, DIE #1
 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:
 PIN 1. VCC
 2. V2OUT
 3. V1OUT
 4. TXE
 5. RXE
 6. VEE
 7. GND
 8. ACC</p> | <p>STYLE 18:
 PIN 1. ANODE
 2. ANODE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. CATHODE
 8. CATHODE</p> | <p>STYLE 19:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. MIRROR 2
 7. DRAIN 1
 8. MIRROR 1</p> | <p>STYLE 20:
 PIN 1. SOURCE (N)
 2. GATE (N)
 3. SOURCE (P)
 4. GATE (P)
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 21:
 PIN 1. CATHODE 1
 2. CATHODE 2
 3. CATHODE 3
 4. CATHODE 4
 5. CATHODE 5
 6. COMMON ANODE
 7. COMMON ANODE
 8. CATHODE 6</p> | <p>STYLE 22:
 PIN 1. I/O LINE 1
 2. COMMON CATHODE/VCC
 3. COMMON CATHODE/VCC
 4. I/O LINE 3
 5. COMMON ANODE/GND
 6. I/O LINE 4
 7. I/O LINE 5
 8. COMMON ANODE/GND</p> | <p>STYLE 23:
 PIN 1. LINE 1 IN
 2. COMMON ANODE/GND
 3. COMMON ANODE/GND
 4. LINE 2 IN
 5. LINE 2 OUT
 6. COMMON ANODE/GND
 7. COMMON ANODE/GND
 8. LINE 1 OUT</p> | <p>STYLE 24:
 PIN 1. BASE
 2. EMITTER
 3. COLLECTOR/ANODE
 4. COLLECTOR/ANODE
 5. CATHODE
 6. CATHODE
 7. COLLECTOR/ANODE
 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25:
 PIN 1. VIN
 2. N/C
 3. REXT
 4. GND
 5. IOUT
 6. IOUT
 7. IOUT
 8. IOUT</p> | <p>STYLE 26:
 PIN 1. GND
 2. dv/dt
 3. ENABLE
 4. ILIMIT
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. VCC</p> | <p>STYLE 27:
 PIN 1. ILIMIT
 2. OVLO
 3. UVLO
 4. INPUT+
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. DRAIN</p> | <p>STYLE 28:
 PIN 1. SW_TO_GND
 2. DASIC_OFF
 3. DASIC_SW_DET
 4. GND
 5. V_MON
 6. VBULK
 7. VBULK
 8. VIN</p> |
| <p>STYLE 29:
 PIN 1. BASE, DIE #1
 2. EMITTER, #1
 3. BASE, #2
 4. EMITTER, #2
 5. COLLECTOR, #2
 6. COLLECTOR, #2
 7. COLLECTOR, #1
 8. COLLECTOR, #1</p> | <p>STYLE 30:
 PIN 1. DRAIN 1
 2. DRAIN 1
 3. GATE 2
 4. SOURCE 2
 5. SOURCE 1/DRAIN 2
 6. SOURCE 1/DRAIN 2
 7. SOURCE 1/DRAIN 2
 8. GATE 1</p> | | |

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