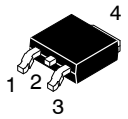
# MOSFET – Power, Single, P-Channel

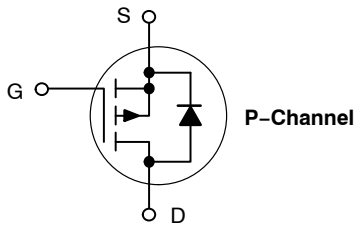
## -60 V, -61 A, 16 mΩ

# NVD5117PL

| $V_{(BR)DSS}$ | $R_{DS(on)}$ | $I_D$ |
|---|---|---|
| −60 V | 16 mΩ @ −10 V | −61 A |
| | 22 mΩ @ −4.5 V | |




**DPAK**
**CASE 369C**
**STYLE 2**




### Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- High Current Capability
- Avalanche Energy Specified
- AEC−Q101 Qualified
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

### MAXIMUM RATINGS ($T_J$ = 25°C unless otherwise noted)

| Symbol | Parameter | | | Value | Unit |
|---|---|---|---|---|---|
| $V_{DSS}$ | Drain−to−Source Voltage | | | −60 | V |
| $V_{GS}$ | Gate−to−Source Voltage | | | ±20 | V |
| $I_D$ | Continuous Drain Current $R_{\theta JC}$ (Note 1) | Steady State | $T_C$ = 25°C | −61 | A |
| | | | $T_C$ = 100°C | −43 | |
| $P_D$ | Power Dissipation $R_{\theta JC}$ (Note 1) | | $T_C$ = 25°C | 118 | W |
| | | | $T_C$ = 100°C | 59 | |
| $I_D$ | Continuous Drain Current $R_{\theta JA}$ (Notes 1 & 2) | Steady State | $T_A$ = 25°C | −11 | A |
| | | | $T_A$ = 100°C | −8 | |
| $P_D$ | Power Dissipation $R_{\theta JA}$ (Notes 1 & 2) | | $T_A$ = 25°C | 4.1 | W |
| | | | $T_A$ = 100°C | 2.1 | |
| $I_{DM}$ | Pulsed Drain Current | $T_A$ = 25°C, $t_p$ = 10 μs | | −419 | A |
| $I_{Dmaxpkg}$ | Current Limited by Package (Note 3) | $T_A$ = 25°C | | 60 | A |
| $T_J$, $T_{stg}$ | Operating Junction and Storage Temperature | | | −55 to 175 | °C |
| $I_S$ | Source Current (Body Diode) | | | −118 | A |
| $E_{AS}$ | Single Pulse Drain−to−Source Avalanche Energy ($T_J$ = 25°C, $V_{DD}$ = 50 V, $V_{GS}$ = 10 V, $I_{L(pk)}$ = 40 A, L = 0.3 mH, $R_G$ = 25 Ω) | | | 240 | mJ |
| $T_L$ | Lead Temperature for Soldering Purposes (1/8″ from case for 10 s) | | | 260 | °C |

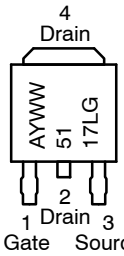
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{\theta JC}$ | Junction−to−Case − Steady State (Drain) | 1.3 | °C/W |
| $R_{\theta JA}$ | Junction−to−Ambient − Steady State (Note 2) | 37 | |

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 $mm^2$, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

### MARKING DIAGRAMS & PIN ASSIGNMENT




A = Assembly Location*
Y = Year
WW = Work Week
5117L = Device Code
G = Pb−Free Package

* The Assembly Location Code (A) is front side optional. In cases where the Assembly Location is stamped in the package bottom (molding ejecter pin), the front side assembly code may be blank.

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Symbol | Parameter | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| $V_{(BR)DSS}$ | Drain−to−Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = −250 μA | | −60 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{GS}$ = 0 V, $V_{DS}$ = −60 V | $T_J$ = 25°C | | | −1.0 | μA |
| | | | $T_J$ = 125°C | | | −100 | |
| $I_{GSS}$ | Gate−to−Source Leakage Current | $V_{DS}$ = 0 V, $V_{GS}$ = ±20 V | | | | ±100 | nA |
| **ON CHARACTERISTICS** (Note 4) | | | | | | | |
| $V_{GS(TH)}$ | Gate Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = −250 μA | | −1.5 | | −2.5 | V |
| $R_{DS(on)}$ | Drain−to−Source On Resistance | $V_{GS}$ = −10 V, $I_D$ = −29 A | | | 12 | 16 | mΩ |
| | | $V_{GS}$ = −4.5 V, $I_D$ = −29 A | | | 16 | 22 | |
| $g_{FS}$ | Froward Transconductance | $V_{DS}$ = −15 V, $I_D$ = −15 A | | | 30 | | S |
| **CHARGES AND CAPACITANCES** | | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$ = 0 V, f = 1.0 MHz, $V_{DS}$ = −25 V | | | 4800 | | pF |
| $C_{oss}$ | Output Capacitance | | | | 480 | | |
| $C_{rss}$ | Reverse Transfer Capacitance | | | | 320 | | |
| $Q_{G(TOT)}$ | Total Gate Charge | $V_{DS}$ = −48 V, $I_D$ = −29 A | $V_{GS}$ = −4.5 V | | 49 | | nC |
| | | | $V_{GS}$ = −10 V | | 85 | | |
| $Q_{G(TH)}$ | Threshold Gate Charge | $V_{GS}$ = −4.5 V, $V_{DS}$ = −48 V, $I_D$ = −29 A | | | 3 | | |
| $Q_{GS}$ | Gate−to−Source Charge | | | | 13 | | |
| $Q_{GD}$ | Gate−to−Drain Charge | | | | 28 | | |
| $V_{GP}$ | Plateau Voltage | | | | 3.2 | | V |
| **SWITCHING CHARACTERISTICS** (Notes 4) | | | | | | | |
| $t_{d(on)}$ | Turn−On Delay Time | $V_{GS}$ = −4.5 V, $V_{DS}$ = −48 V, $I_D$ = −29 A, $R_G$ = 2.5 Ω | | | 22 | | ns |
| $t_r$ | Rise Time | | | | 195 | | |
| $t_{d(off)}$ | Turn−Off Delay Time | | | | 50 | | |
| $t_f$ | Fall Time | | | | 132 | | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | | |
| $V_{SD}$ | Forward Diode Voltage | $V_{GS}$ = 0 V, $I_S$ = −29 A | $T_J$ = 25°C | | −0.86 | −1.0 | V |
| | | | $T_J$ = 125°C | | −0.74 | | |
| $t_{RR}$ | Reverse Recovery Time | $V_{GS}$ = 0 V, $dI_S/dt$ = 100 A/μs, $I_s$ = −29 A | | | 36 | | ns |
| $t_a$ | Charge Time | | | | 19 | | |
| $t_b$ | Discharge Time | | | | 17 | | |
| $Q_{RR}$ | Reverse Recovery Charge | | | | 44 | | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

## TYPICAL CHARACTERISTICS

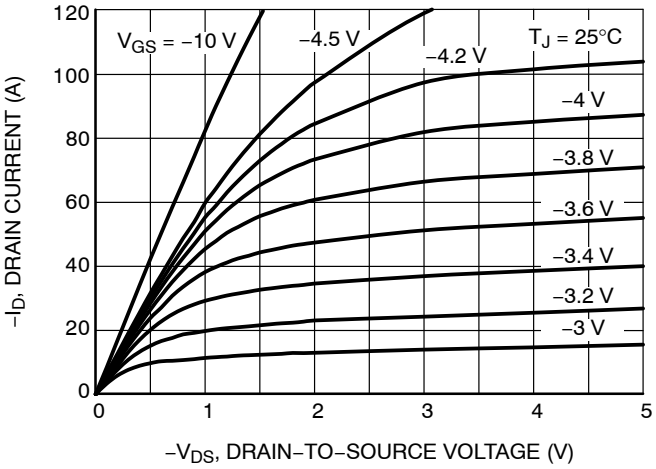



**Figure 1. On−Region Characteristics**

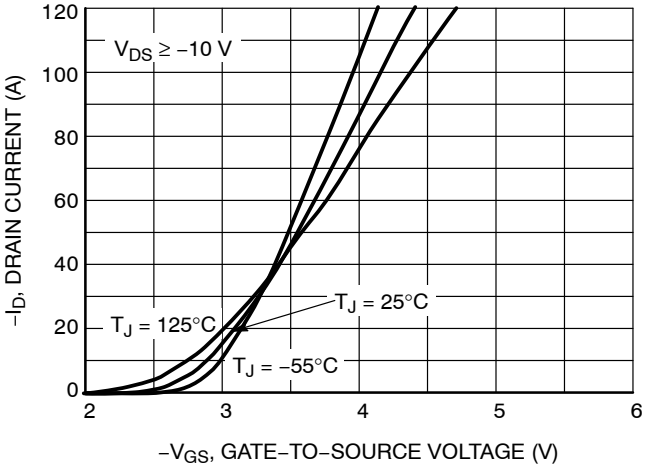



**Figure 2. Transfer Characteristics**

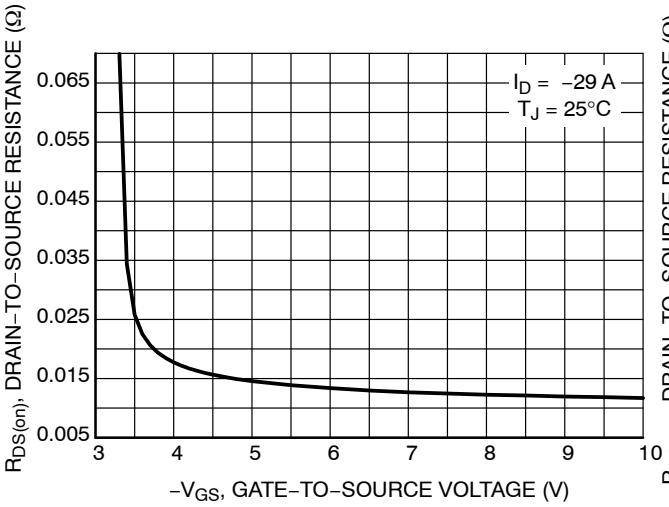



**Figure 3. On−Resistance vs. Gate−to−Source Voltage**

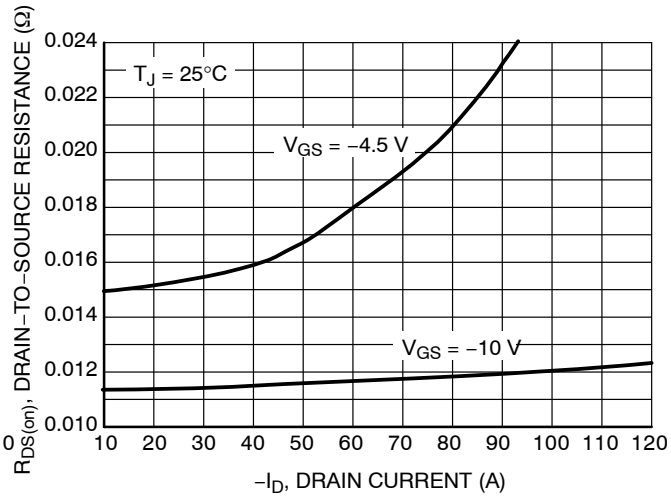



**Figure 4. On−Resistance vs. Drain Current and Gate Voltage**

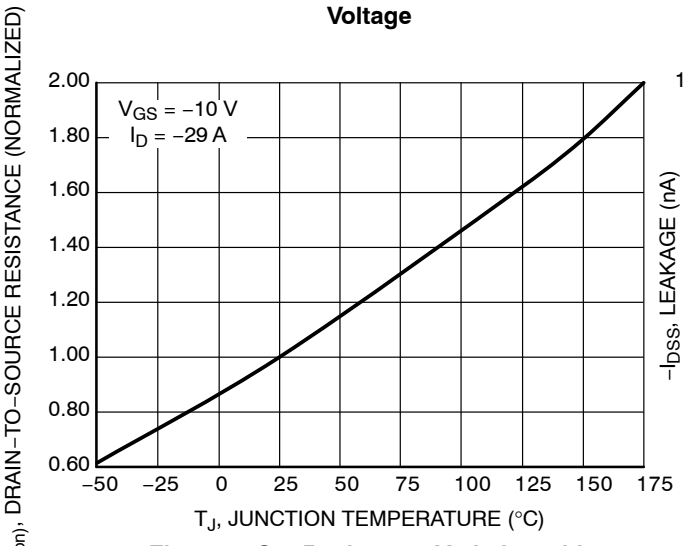



**Figure 5. On−Resistance Variation with Temperature**

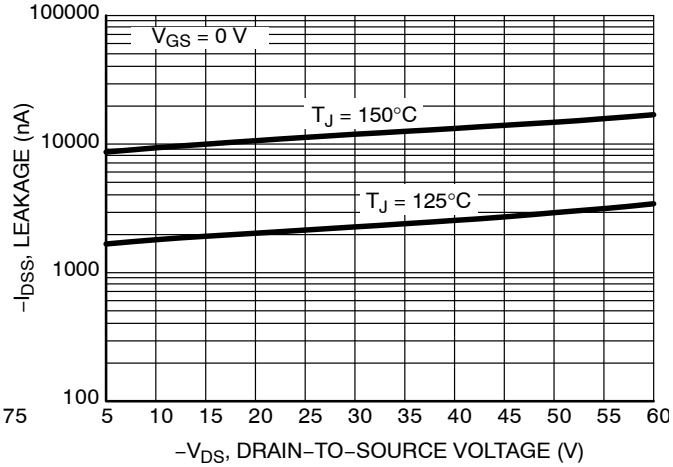



**Figure 6. Drain−to−Source Leakage Current vs. Voltage**

## TYPICAL CHARACTERISTICS (continued)

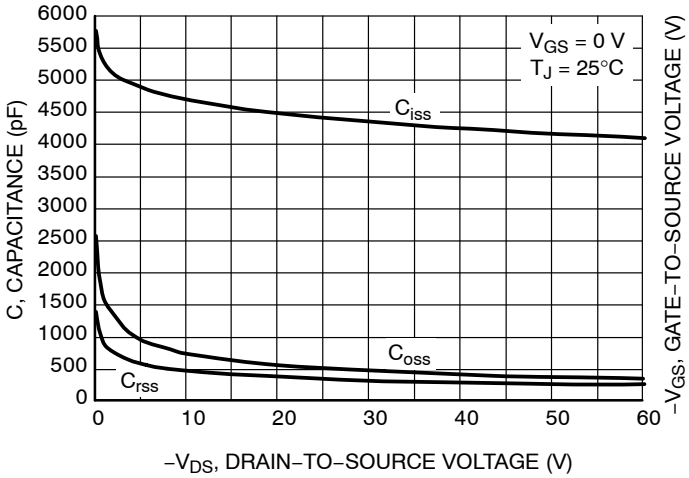



**Figure 7. Capacitance Variation**

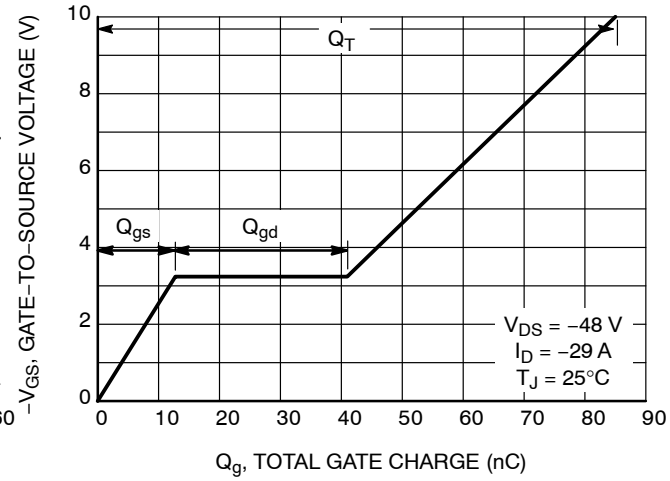



**Figure 8. Gate−to−Source vs. Total Charge**

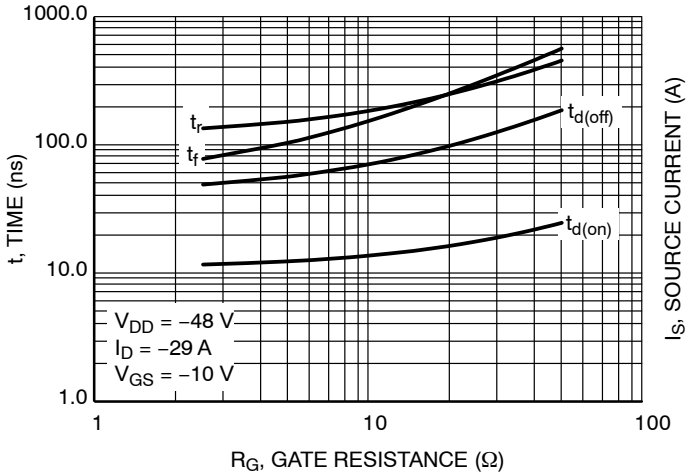



**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

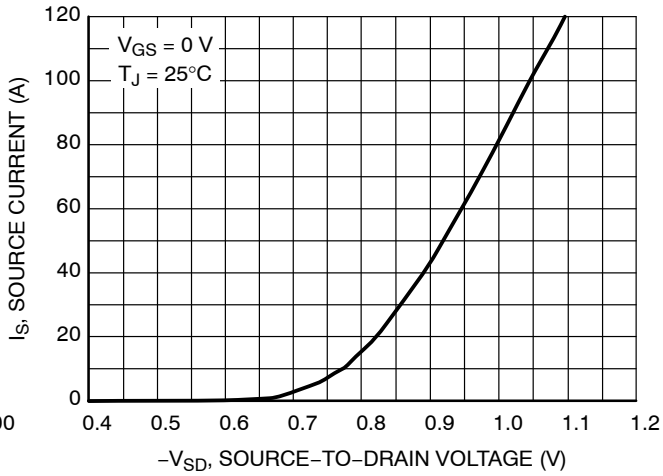



**Figure 10. Diode Forward Voltage vs. Current**

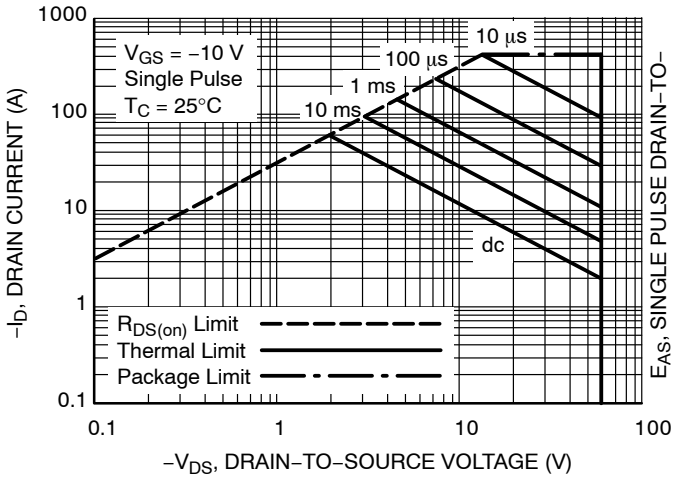



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

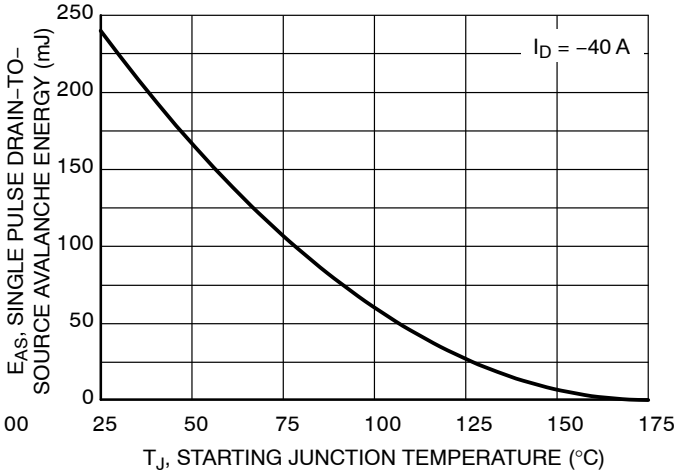



**Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature**

## TYPICAL CHARACTERISTICS (continued)

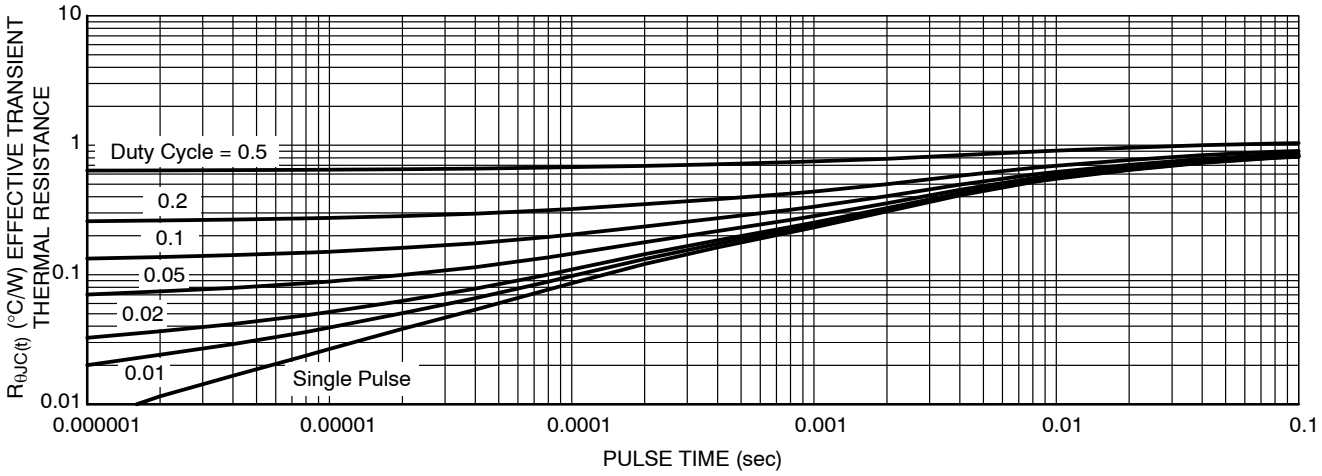



**Figure 13. Thermal Response**

### DEVICE ORDERING INFORMATION

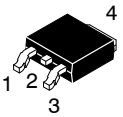
| Device | Package | Shipping† |
|---|---|---|
| NVD5117PLT4G−VF01 | DPAK (Pb−Free) | 2500 / Tape & Reel |

**DISCONTINUED** (Note 5)

| | | |
|---|---|---|
| NVD5117PLT4G | DPAK (Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

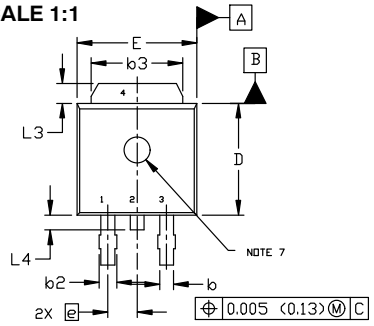
5. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.



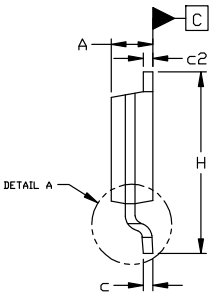

**DPAK (SINGLE GAUGE)**
CASE 369C
ISSUE G

DATE 31 MAY 2023

**SCALE 1:1**




TOP VIEW

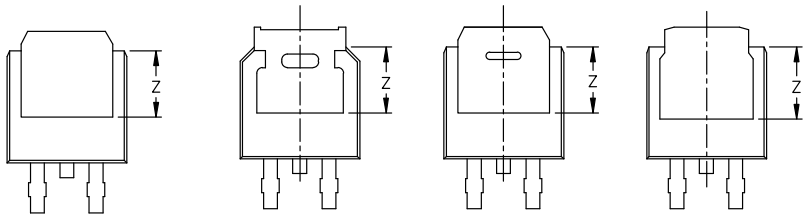



SIDE VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

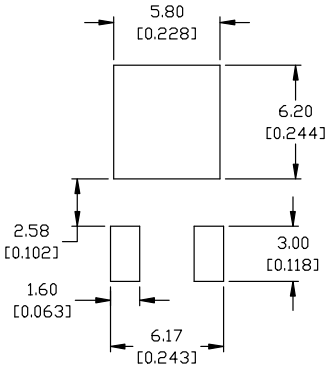
| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. |
| A | 0.086 | 0.094 | 2.18 | 2.38 |
| A1 | 0.000 | 0.005 | 0.00 | 0.13 |
| b | 0.025 | 0.035 | 0.63 | 0.89 |
| b2 | 0.028 | 0.045 | 0.72 | 1.14 |
| b3 | 0.180 | 0.215 | 4.57 | 5.46 |
| c | 0.018 | 0.024 | 0.46 | 0.61 |
| c2 | 0.018 | 0.024 | 0.46 | 0.61 |
| D | 0.235 | 0.245 | 5.97 | 6.22 |
| E | 0.250 | 0.265 | 6.35 | 6.73 |
| e | 0.090 BSC | | 2.29 BSC | |
| H | 0.370 | 0.410 | 9.40 | 10.41 |
| L | 0.055 | 0.070 | 1.40 | 1.78 |
| L1 | 0.114 REF | | 2.90 REF | |
| L2 | 0.020 BSC | | 0.51 BSC | |
| L3 | 0.035 | 0.050 | 0.89 | 1.27 |
| L4 | ---- | 0.040 | --- | 1.01 |
| Z | 0.155 | ---- | 3.93 | --- |




BOTTOM VIEW

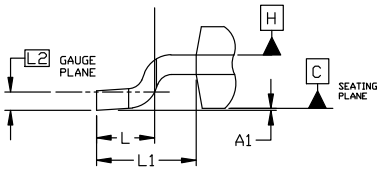
BOTTOM VIEW

ALTERNATE CONSTRUCTIONS



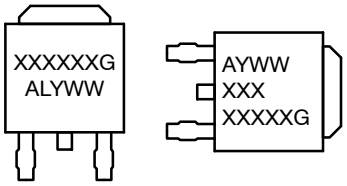

RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.




DETAIL A
ROTATED 90° CW

**GENERIC MARKING DIAGRAM***




**IC** **Discrete**

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

| DOCUMENT NUMBER: | 98AON10527D | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
|---|---|---|
| DESCRIPTION: | DPAK (SINGLE GAUGE) | PAGE 1 OF 1 |

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