AX8052F143 ERRATA

Errata

Silicon Errata for AX8052F143

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Introduction

This document lists silicon erratas, as well as features of the AX8052F143 that may be unexpected to the user.

The issues listed in this document are for the silicon revisions listed in the table below.

Table 1.

Revision	REVISION Register	SILICONREV Register
AX8052F143−2	0x51	0x8F
AX8052F143−3	0x51	0x90

The reader is requested to also consult the AX8052 and AX5043 Silicon Errata for additional information.

Issues

GPIOENABLE = 0 Disables TCXO Oscillator Control on PB2

The radio state machine may control switching on and off an external TCXO through pin PB2 by setting AX5043_PINFUNCPWRAMP[3:0] = 7 and PALTRADIO[6] = 1. This is commonly used in Wake−on−Radio (WOR) mode. This function is disabled by setting GPIOENABLE = 0. Libmf library routine enter_sleep() sets GPIOENABLE = 0 to avoid glitches on the microcontroller I/O pins during wakeup.

There are two options In order to retain TCXO enable control by the receiver state machine during microcontroller sleep:

1. Wake up the microcontroller whenever the radio switches on the TCXO. This can be achieved with the following register settings, which cause the radio to raise an interrupt when powering up the TCXO:
   AX5043_IRQMASK0 |= 0x80;
   AX5043_POWIRQMASK = 0x90;
   The additional current consumption is usually negligible, as typical TCXO consumption is around 1 mA
2. Do not set GPIOENABLE = 0 when entering sleep. This is not recommended in most cases, as glitches may be observed on the I/O pins during wakeup.

Affected Revisions: AX8052F143−2, AX8052F143−3

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