



安森美半导体
ON Semiconductor[®]

一体式计算机电源参考设计

All-in-One PC Power Supply Reference Design

议程 Agenda

- EPA能效要求 EPA efficiency requirements
- 参考设计目标 Reference design goals
- 拓扑结构选择 Topology selection
- PFC段设计 PFC stage design
- LLC段设计 LLC stage design
- 同步整流(SR)设计 SR design
- 待机管理及协调 Standby management and handshaking
- 参考设计性能 Reference design performance
- 后续工作 Future work
- 总结 Summary

规范机构的能效目标 Energy Efficiency: Regulatory Agencies Targets

• 降低待机(空载)能耗 Standby (no load) Power Reduction

- 通过电源的总电能中约有25%是在待机模式下消耗的 ~25% of total energy passing through power supplies is in standby mode^[13]
- 世界各地的规范机构纷纷瞄准降低待机能耗 Concerted effort by worldwide regulatory agencies

• 提升工作能效 Active Mode Efficiency Improvement

- 通过电源的总电能中约有75%是在工作模式下消耗的 ~75% of total energy passing through power supplies is in active mode^[13]

• 功率因数校正(PFC)(或谐波减少) Power Factor Correction (or Harmonic Reduction)

- 遵从IEC61000-3-2规范(欧盟、日本) Applicable with IEC61000-3-2^[11] (Europe, Japan)
- 某些能效规范也要求功率因数(PF)>0.9 Some efficiency specifications also require >0.9 PF.
→例如: “能源之星”4.0版计算机规范 example: computers (ENERGY STAR® rev. 4^[12])



China CSC^[6]
(ex-CECP),



Japan Top Runner^[9]
program



Japan Eco Mark^[10]
program



Australian Government
Department of the Environment
and Water Resources
Australian Greenhouse Office

Australia AGO^[7]



California CEC^[5]



Korea e-Standby
program^[8]



Europe
COC^[4]



ENERGY
STAR^[3]

高能效规范最新进展-计算机

Update on Energy Efficiency Regulations - Computing

计算机 Computing

•台式机 Desktops:

- “能源之星”5.0版规范，2009年7月1日生效
[ENERGY STAR® 5.0](#) effective on Jul. 1, 2009



- “80 PLUS”及计算产业气候拯救行动(CSCI)
[80 PLUS](#) & [Climate Savers Computing Initiative](#)

- 分级能效等级 [Tiered efficiency levels](#)



•膝上型(更多信息参见“能源之星”2.0版外部电源规范)

Laptops (More information at [ENERGY STAR® 2.0 for External Power Supplies](#))

- 能效 Efficiency: $\geq 87\%$
- 待机(空载)能耗 Standby (no load) power: $\leq 500 \text{ mW}$
- 功率因数 PF ≥ 0.9



高能效规范最新进展-机顶盒

Update on Energy Efficiency Regulations - STB

机顶盒(STB) Set-Top Boxes



- “能源之星”2.0版，2009年1月1日生效
ENERGY STAR® 2.0 effective on Jan 1, 2009



- 欧盟行为指令第7版，2009年1月1日生效
Europe Code of Conduct version 7 effective Jan 1, 2009



- 标准基于最大允许总能耗TEC(千瓦时/年)或容限 Standard is based on maximum allowable TEC (Total Energy Consumption in kWh/year) or allowance
- 基础容限取决于机顶盒类型(有线、卫星等) Base Allowance depends on the type of STB (Cable, Satellite, etc...)
- 附加功能容限(DVR等) Additional functionalities allowance (DVR, etc...)
- 每年能耗容限(千瓦时/年)=基础功能容限+附加功能容限 Annual Energy Allowance (kWh/year) = Base Functionality Allowance + Additional Functionalities Allowance



高能效规范最新进展-固态照明

Update on Energy Efficiency Regulations - SSL

固态照明(SSL)灯具 Solid State Lighting Luminaires

- “能源之星”1.1版自2009年2月1日开始生效
ENERGY STAR® 1.1 effective on Feb. 1, 2009



- 关态能耗为零 Off-state power: 0
- 最低能效(流明/瓦)要求根据应用的不同(聚光灯、户外灯等)而不同
Minimum efficacy (Lumen/Watt) requirements by applications (downlights, outdoor lights, etc...)
- 功率因数 $PF \geq 0.9$ 针对商业应用 for Commercial
 ≥ 0.7 针对住宅应用 for Residential

- “能源之星”1.2版自2009年下半年开始生效
ENERGY STAR® 1.2 effective in 2H2009



- “能源之星”针对LED灯泡的其它要求 ENERGY STAR® additional requirements for LED bulbs
 - 功率因数 $PF \geq 0.7$
 - 高系统能效→高能效电源 High system efficacy → high efficiency power supply

更详尽及最新的能效机构及规范信息，请访问www.pdma.com，参见PSMA能效规范数据库
For exhaustive and up-to-date information on agencies and regulations, check the PSMA energy efficiency data base at: www.pdma.com

单路输出计算机电源能效目标(服务器, 刀片式服务器, 一体机)

Efficiency Targets for Single-output Computing Power Supplies (Servers, Blades, All-in-1)

Single-Output	Efficiency (%)					Effective Date
	Levels	Specification	20% of rated output power	50% of rated output power	100% of rated output power	
	 CSCI Bronze	- Single-Output - Non-Redundant - PFC 0.9 at 50%	81%	85%	81%	
	 CSCI Silver	- Single-Output - Non-Redundant - PFC 0.9 at 50%	85%	89%	85%	
	 CSCI Gold	- Single-Output - Non-Redundant - PFC 0.9 at 50%	88%	92%	88%	
	CSCI Platinum	- Single-Output - Non-Redundant - PFC 0.9 at 50%	90%	94%	91%	Target



All in 1 PC

本参考设计的能效目标
Target for this reference design

Sources:

- 80 PLUS® : <http://www.80plus.org/>
- Climate Savers® Computing Initiative: <http://www.climatesaverscomputing.org/>
- ENERGY STAR®: http://www.energystar.gov/index.cfm?c=revisions.computer_spec

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参考设计目标 Reference design goals

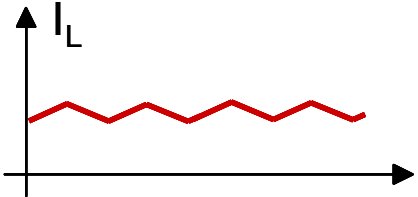
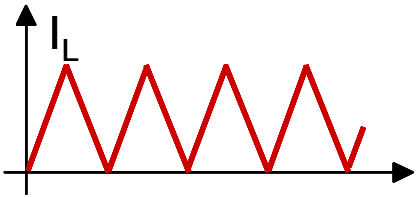
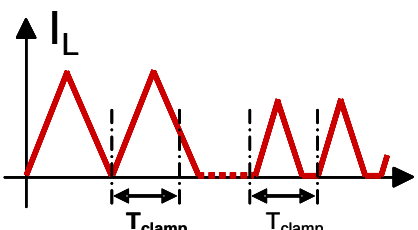
- 必须满足美国环保署(EPA)最高能效要求(80 PLUS银级或金级)
Must meet highest EPA eff. requirements (80+ silver or gold)
- 必须适合一体机(苹果iMac-0.23 dm³) Must fit into All-in-1 PC (Apple iMAC – 0.23 dm³)
- 输入电压范围为90至265 Vac Input voltage range 90-265 Vac
- 单路输出 --12 V分为2个端子 Single output – 12 V divided into two terminals:
 - => 待机端子: 持续提供功率 Standby terminal: delivers power all the time
 - 关态电流消耗50 mA 50 mA in off mode
 - 休眠模式100 mA 100 mA in sleep mode
 - 工作模式最大5 A 5 A maximum in active mode
 - => 电源端子: 工作模式下提供功率(最大15 A) Power terminal: delivers power in active mode (15 A max.)
- 最大总输出功率216 W Total maximum output power 216 W

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PFC段选择 PFC stage selection

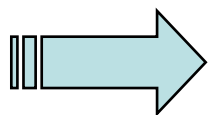
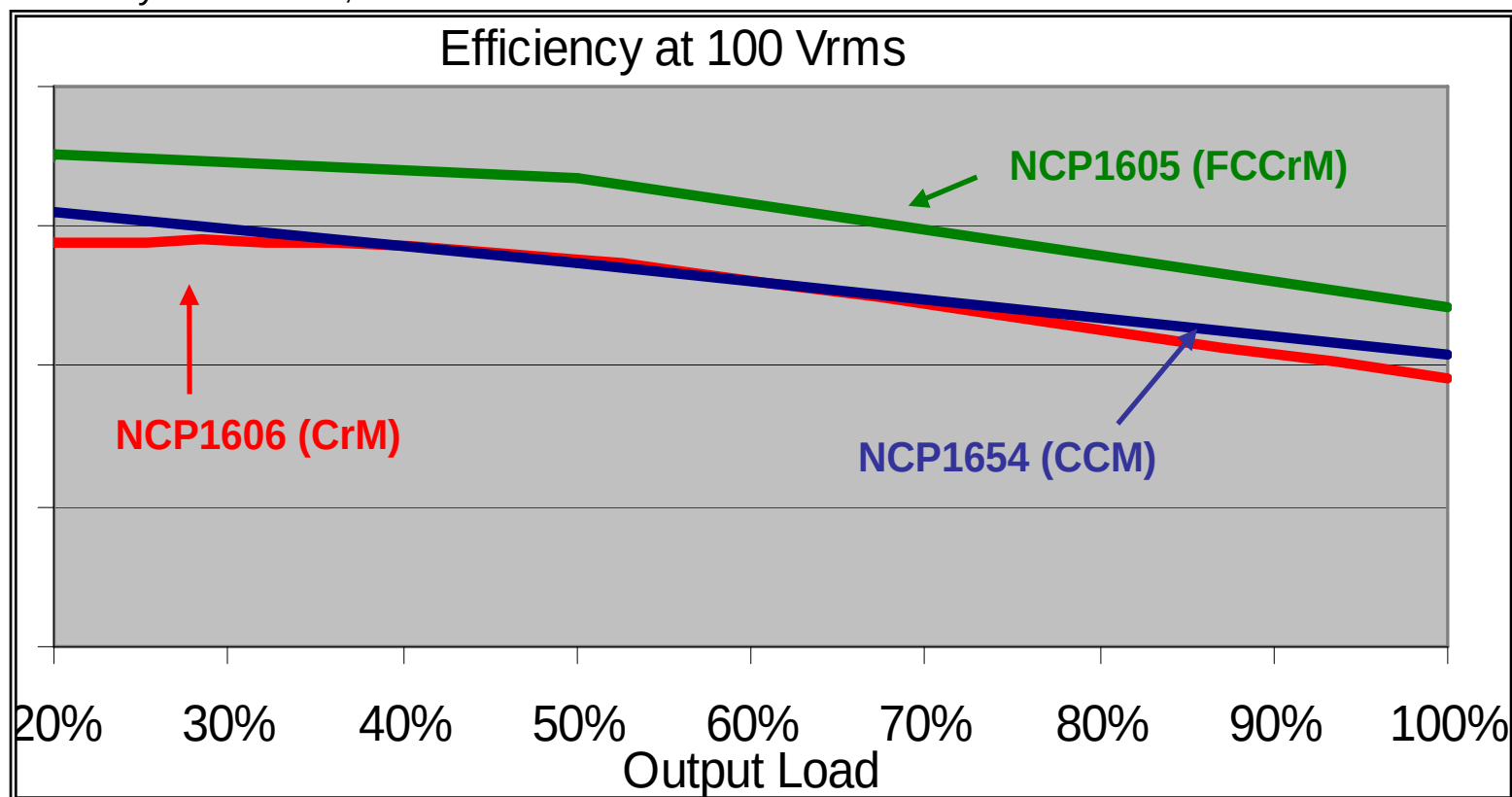
- 本应用的输入功率大于75 W，故需要PFC Input power for this application is > 75 W => need a PFC
- 安森美半导体提供3种模式的方案 ON Semiconductor offers solutions for three modes:

	工作模式 Operating Mode	主要特征 Main Feature
	连续导电模式 (CCM)	总是硬开关 Always hard switching 电感值最大 Inductor value is largest 均方根电流最小 Minimized rms current 如: NCP1654
	临界导电模式 (CrM)	大均方根电流 Large rms current 开关频率不固定 Switching frequency is not fixed 如: NCP1606
	频率钳位临界导电模式 (FCCrM)	大均方根电流 Large rms current 频率受限 Frequency is limited 线圈电感降低 Reduced coil inductance 如: NCP1605

PFC段选择-FCCrM PFC stage selection - FCCrM

300 W、宽主电压输入范围PFC能效测量结果

Efficiency of a 300-W, wide mains PFC has been measured:



依照此图，FCCrM是能效最高、同时保持合理成本的方案

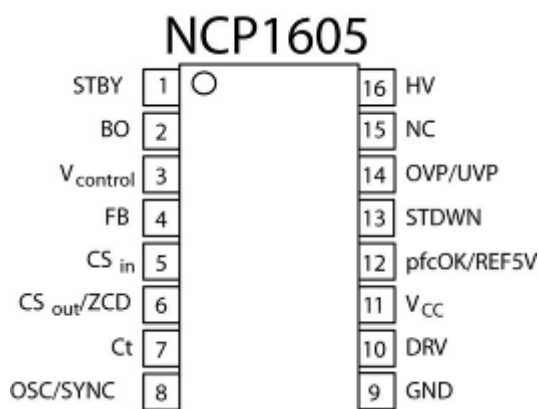
Frequency Clamped CrM seems the most efficient solution while keeping reasonable cost

PFC段选择-控制器

PFC stage selection – controller

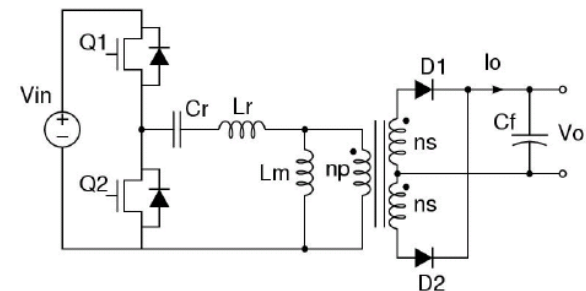
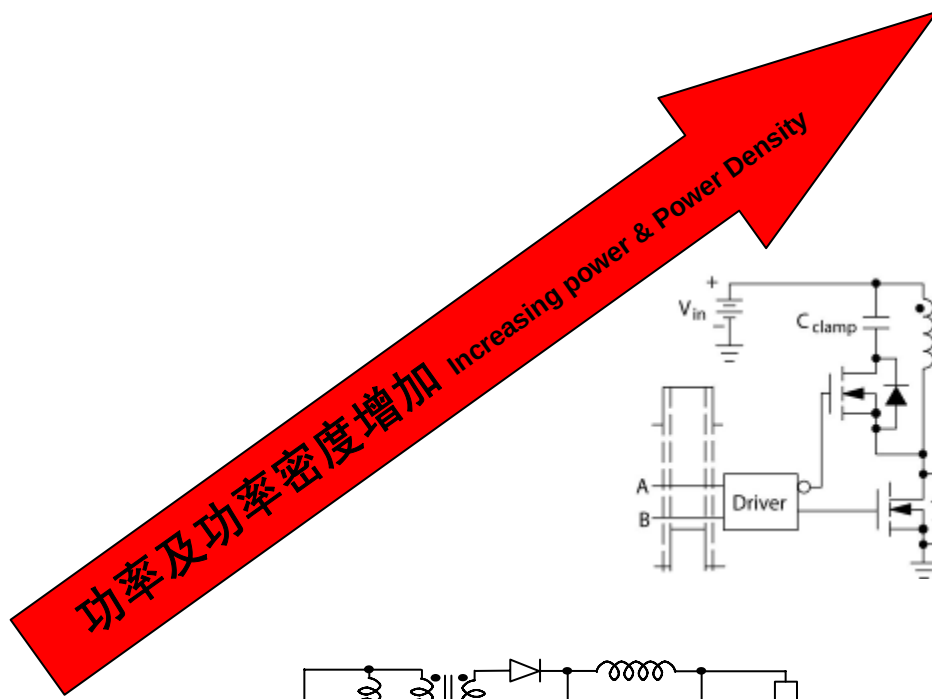
我们应用中的一些有用特性 Some features useful in our application:

- 频率钳位临界导电模式(FCCrM) Frequency Clamped Critical Conduction Mode
- 无损耗高压启动电流源 Lossless High Voltage Current Source for Startup
- 软跳周期用于低能耗待机模式 Soft Skip Cycle for Low Power Standby Mode
- 快速交流线路/负载瞬态补偿 Fast Line / Load Transient Compensation
- “pfcOK”信号提示PFC已就绪 Signal to Indicate that the PFC is Ready “pfcOK”
- VCC范围：10 V至20 V VCC range: from 10 V to 20 V
- 输出欠压保护(UVP)及过压保护(OVP) Output Under and Overvoltage Protection
- 输入欠压(BO)检测 Brown-Out Detection

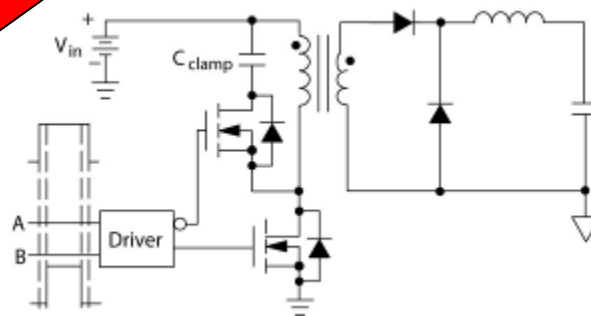


NCP1605集成了一体机电源所需全部特性，因此降低总成本 NCP1605 integrates all needed features for all-in-one power supply and thus reduces overall cost

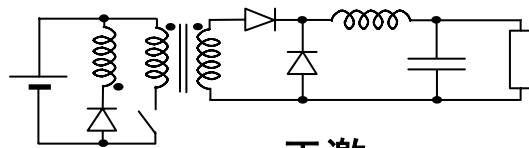
电源段选择 Power stage selection



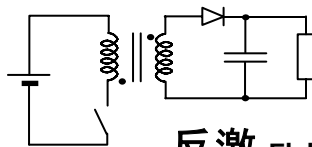
半桥双电感
加单电容
Half-bridge LLC



有源钳位正激
Active clamp forward



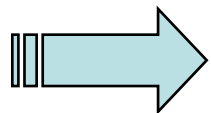
正激
Forward



反激 Flyback

电源段选择-LLC优势 Power stage selection – LLC benefits

- 串联型谐振转换器支持在相对较宽的输入电压和输出负载范围下工作 Series type of resonant converter that allows operation over relatively wide input voltage and output load ranges
- 元器件数量有限：谐振储能元件能部分或全部集成在主变压器中 Limited number of components: resonant tank can be partially or fully integrated into main transformer
- 初级开关管在所有负载条件下零电压开关(ZVS)
 - Zero Voltage Switching (ZVS) condition for the primary switches under all load conditions
- 次级整流器在所有负载条件下零电流开关(ZCS)
 - Zero Current Switching (ZCS) for secondary rectifier under all load conditions
- 应用简单的同步整流(SR) Simple synchronous rectification (SR) implementation



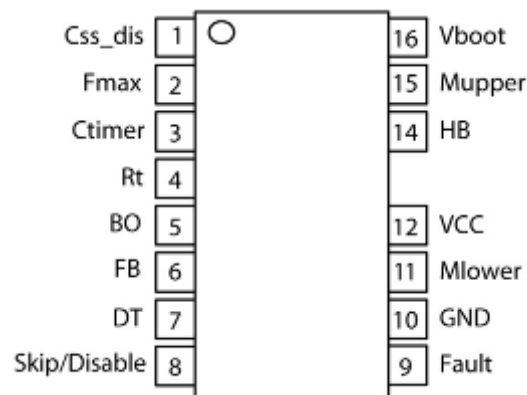
高性价比、高效、容易处理电磁干扰(EMI)的方案
Cost effective, highly efficient and EMI friendly solution

电源段选择-控制器 Power stage selection – controller

特性 Features:

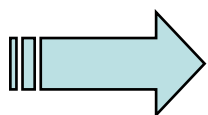
- 50 kHz至500 kHz的高频工作 High-frequency operation from 50 kHz up to 500 kHz
- 600 V高压浮动驱动器 600 V high-voltage floating driver
- 可调节最小开关频率(3%精度) Adjustable minimum switching frequency (3% accuracy)
- 100 ns至2 μ s的可调节死区时间 Adjustable deadtime from 100 ns to 2 μ s
- 藉外部可调节软启动提供的启动序列 Startup sequence via an externally adjustable soft-start
- 输入欠压保护结合闩锁输入 Brown-out protection combined with latch input
- 基于定时器的自动恢复及立即闩锁过流保护 Timer-based auto-recovery and immediate latched OCP
- 可藉导通/关闭控制来关闭输入(跳周期模式) Disable input for ON/OFF control (skip mode)
- 300 μ A的低待机电流 Low startup current of 300 μ A
- 1 A/0.5 A峰值电流汲极/源极驱动能力 1 A / 0.5 A peak current sink / source drive capability
- 共用集极或射极光耦合器连接 Common collector or emitter optocoupler connections

NCP1397



NCP1397用于一体机应用的优势 Benefits for all-in-1 application:

- 不需要驱动变压器=>满足尺寸限制 No driver transformer needed => size restrictions
- 简单应用跳周期模式=>适合待机所需 Simple skip mode implementation => needed for standby
- 简单应用过流保护=>降低成本 Simple OCP implementation => cost impact

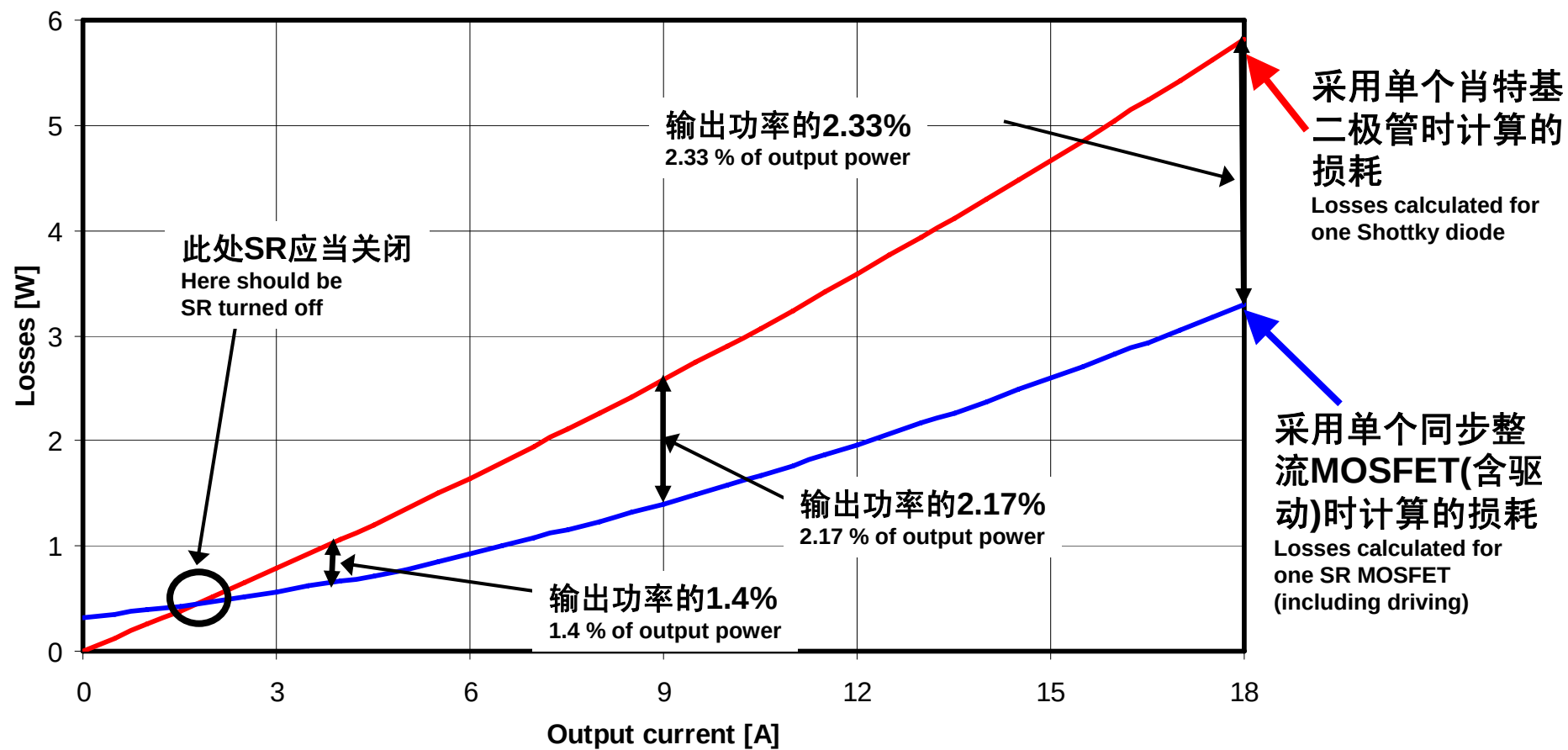


NCP1397是LLC电源段的高性价比及可靠方案

NCP1397 is cost effective and reliable solution for LLC power stage

电源段选择-同步整流好处

Power stage selection – SR justification

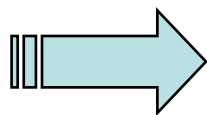
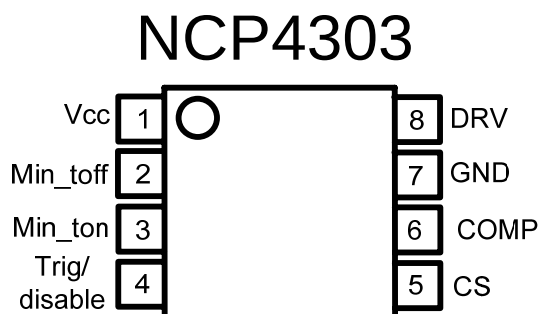


高于特定输出功率时，同步整流(SR)技术能大幅提升能效
Synchronous Rectification can significantly improve efficiency above certain output power

电源段选择-SR控制器 Power stage selection – SR controller

我们应用中的一些有用特性 Some features useful in our application:

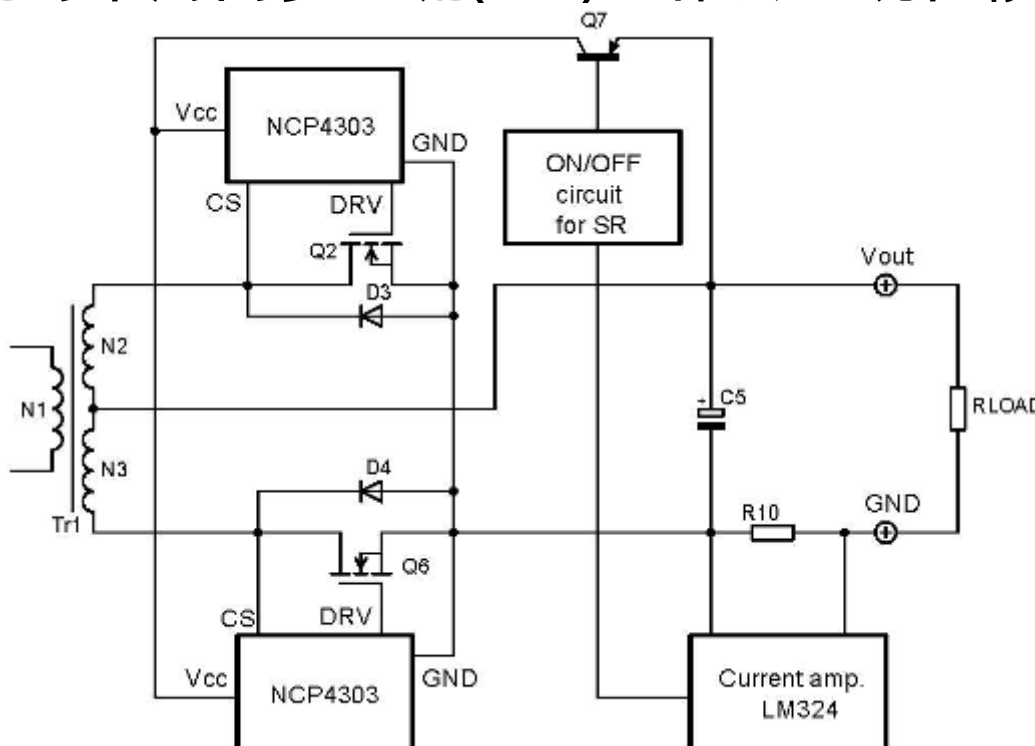
- 工作在CCM及DCM应用 Operates in CCM and DCM Applications
- 真正的次级零电流检测(ZCD)，带可调节阈值 True Secondary ZCD with Adjustable Threshold
- 自动寄生电感补偿 Automatic Parasitic Inductance Compensation
- 从电流感测(CS)到驱动器的50 ns关闭时间延迟 50 ns Turn off Delay from CS to Driver
- 提供外部信号接口，以用于CCM模式 Interface to External Signal for CCM Mode
- 触发器输入以进入待机模式 Trigger Input to enter Standby Mode
- 与Vcc电平无关的可调节最小导通时间 Adjustable Min Ton Independent of Vcc Level
- 与Vcc电平无关的可调节最小关闭时间 Adjustable Min Toff Independent of Vcc Level
- 5 A/2.5 A峰值电流驱动能力 5 A / 2.5 A Peak Current Drive Capability
- 电压范围高达28 V Voltage range up to 28 V
- 12 V或5 V的门驱动钳位 Gate drive clamp of either 12 V or 5 V
- 低启动及待机电流消耗 Low startup and standby current consumption
- 最高工作频率达500 kHz Maximum Frequency of Operation up to 500 kHz



NCP4303是适合任何同步整流(SR)系统的高性能驱动器
NCP4303 is high performance driver for any SR system

次级同步整流导通/关闭 Secondary SR turn on/off

- 仅在高于特定功率时使用同步整流(SR)来提升能效 Usage of SR boosts efficiency above certain power only
- 低输出电流时采用同步整流(SR)工作会呈现低能效 Operation of SR for low output

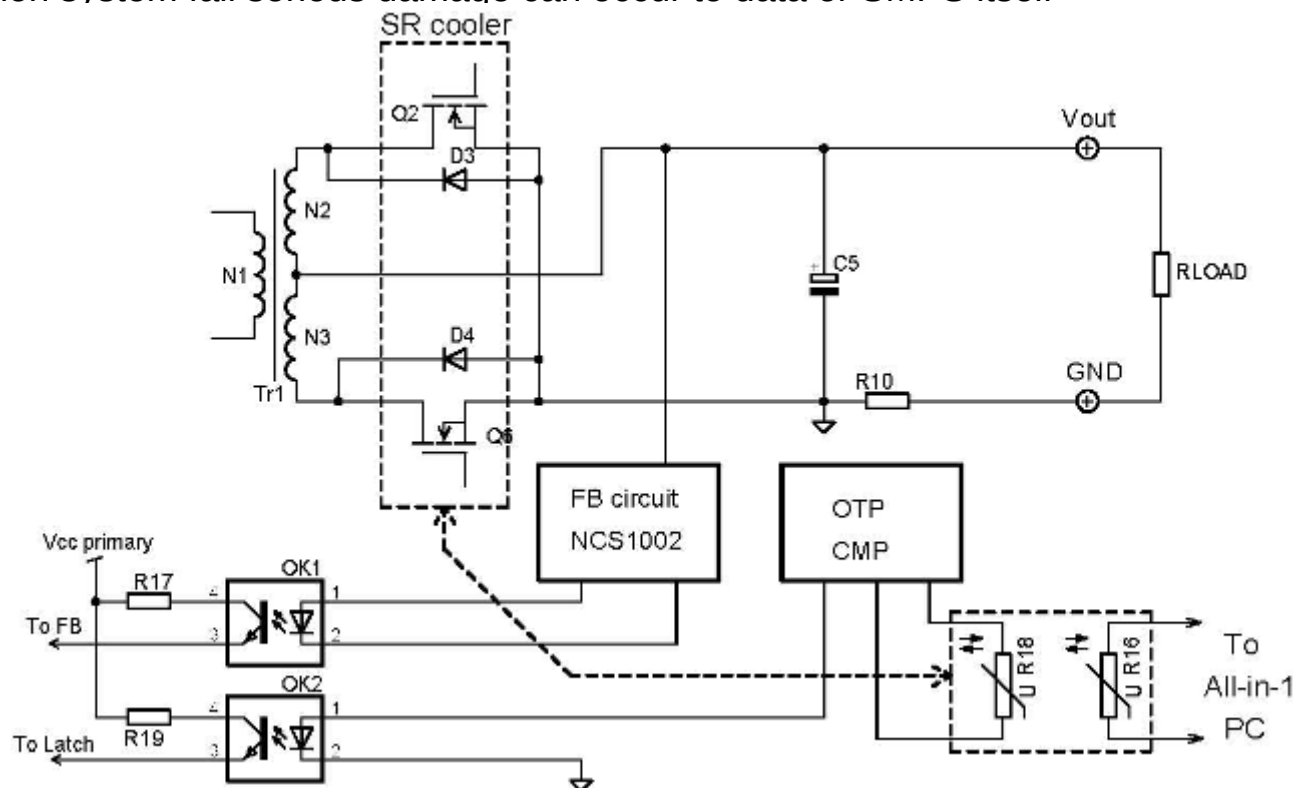


需要根据输出电流信息来关闭同步整流(SR)

SR needs to be turned off based on the output current information

次级整流器过温保护 OTP for secondary rectifiers

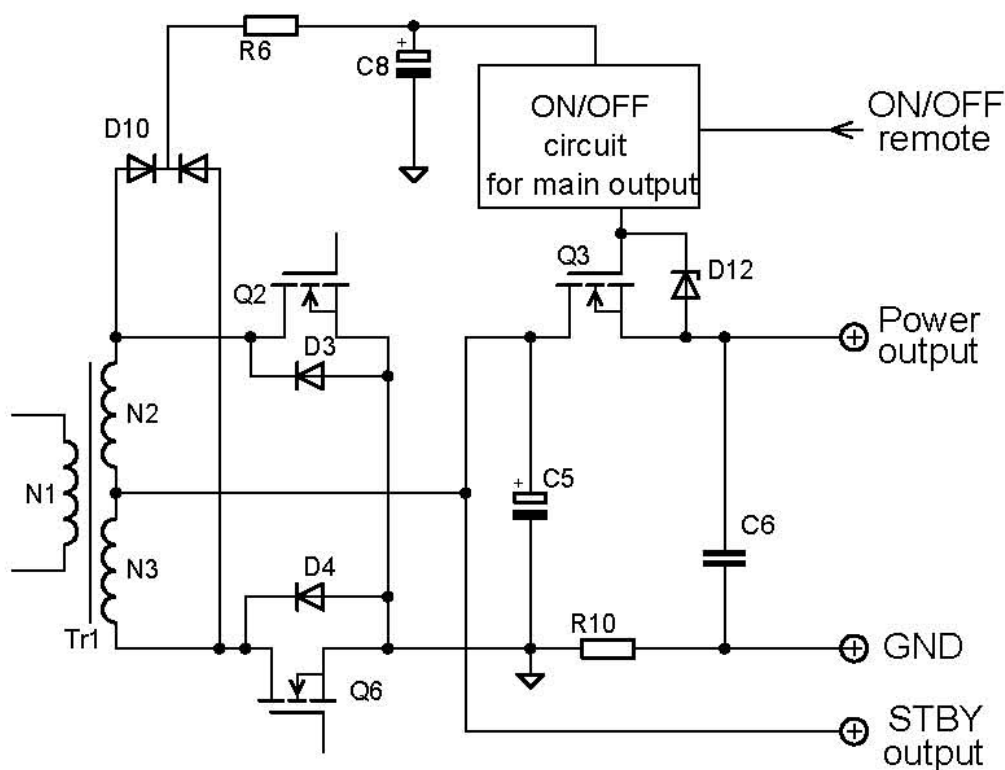
- 最大输出电流是18 A。散热风扇或次级整流系统故障时，数据或开关电源本身可能遭遇严重损坏 Max output current is 18 A. In case of fan or secondary rectification system fail serious damage can occur to data or SMPS itself



需要保护开关电源，防止温度过高，并提供信号给电脑用于风扇速度控制，及在开关电源可能出现故障前关闭电脑 SMPS needs to be protected against over temperature and provide a signal to PC for fan speed control and to shut down prior the SMPS would fail

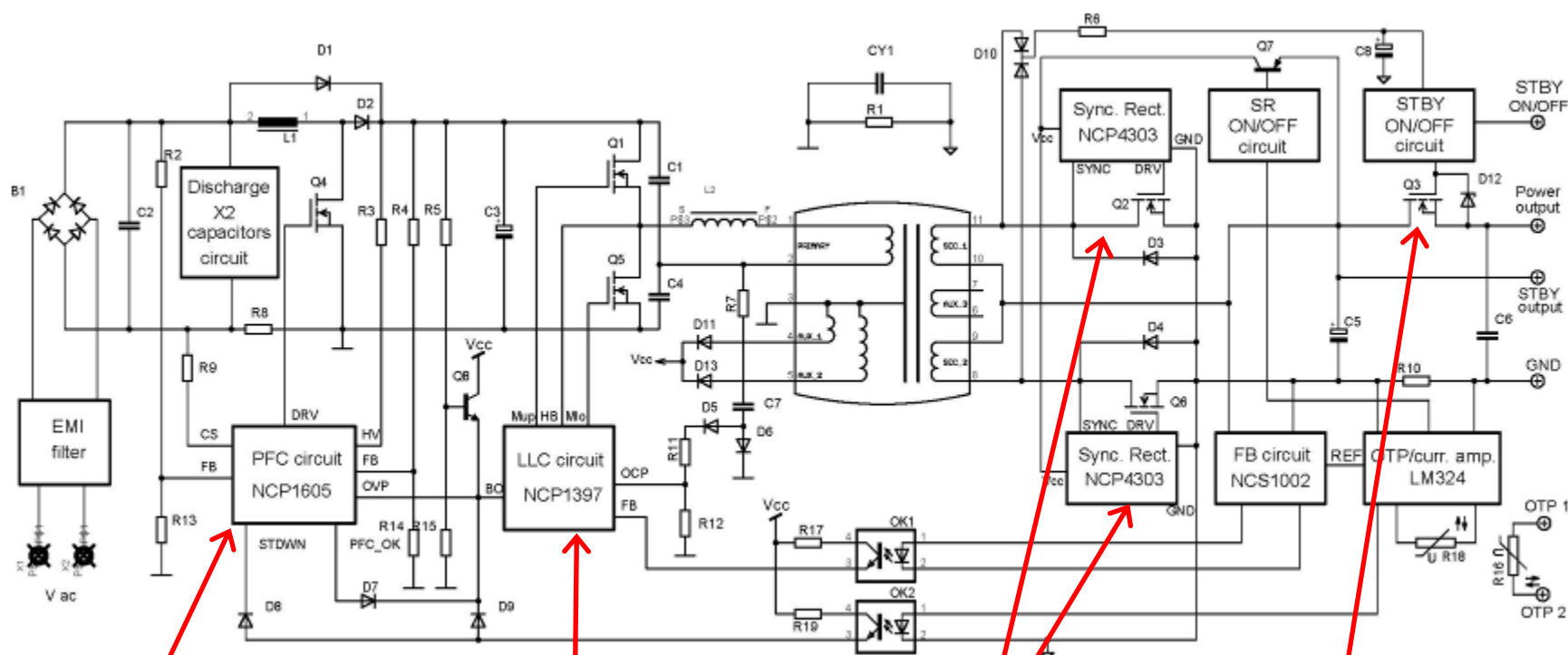
待机管理 Standby management

- 根据一体机规范，待机模式下电源端子必须采用外部开关来关闭
According to All-in-1 spec the power terminal has to be turned off during standby mode by an external switch



与PFET相比，NFET提供较低的导通阻抗
NFET provides low $R_{ds\ on}$ compare to PFET

完整功能框图 Complete block diagram



FCCrM将前段能效
提至最高，减小
PFC线圈尺寸

FCCrM maximize eff. of front
stage, reduces PFC coil size

ZVS提升能效至最高，
LLC拓扑结构将尺寸减
至最小

ZVS maximizes efficiency, LLC topology
minimizes dimensions

SR提升中、高
负载时的能效

SR improves eff. under
Medium and high loads

待机时断开电
源输出连接

Disconnects pwr. output
during STBY

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NCP1605设计工作表 NCP1605 design worksheet

J. Turchi / January 2007

NCP1605 Excel Spreadsheet

Please enter your specification

f _{ac}	(Hz)	50	Ac line frequency
V _{acL}	(V)	90	Ac line rms lowest level (generally 85 V or 90 V in wide mains applications)
V _{acH}	(V)	255	Ac line rms highest level (generally 255 V in wide or European mains applications)
V _{out,nom}	(V)	350	Wished regulation level for the output voltage (generally 300 V or 400 V in wide mains apps)
V _{out,L}	(V)	350	Minimum Output Voltage you can accept in normal operation - Use V _{out,L} =V _{out} as a default value if you don't know
V _{ovp}	(V)	410	Over-Voltage Protection Level
eff	(%)	94	Expected efficiency at low line, full load - use 92 % as a default value if you don't know
P _{out}	(W)	230	Maximum output power
f _{sw}	(kHz)	25	Switching frequency
R _{ds(on)}	(Ω)	0.19	MOSFET on-time resistance @ 25 °C
T _{hold-up}	(ms)	10	Hold-up time. Put 0 if no hold-up time is specified or if you don't know
V _{hold(min)}	(V)	350	Minimum output Voltage you can accept at the end of the hold-up time - Don't fill this cell or put any value if no hold-up time is specified
ΔV _{ripple}	(%)	7	Peak to peak low frequency ripple that is acceptable across the bulk capacitor as a percentage of the regulation output voltage ("V _{out} "). Choose 7% if p.
V _{cc}	(V)	15	V _{cc} voltage provided to the NCP1605
V _{cc,boH}	(V)	83	rms line amplitude above which the PFC stage starts operation
f _c	(Hz)	0.1	compensation corner frequency

Bulk Capacitor and Coil specification

C _{bulk}	(μF)	500	Minimum C _{bulk} capacitance meeting the low frequency ripple and hold-up time constraints (*)
L _{coil}	(μH)	172	Proposed inductor coil inductance not to have permanent DCM operation (recommended)
L ₁	(μH)	200	Your inductance choice (should be higher or equal to "L _{coil} ")
I _{coil(rms)}	(A)	2.7	Max peak coil current resulting from your inductance choice
I _{coil(pk)}	(A)	3.1	Maximum rms coil current

Conduction Losses

Input bridge	(W)	4.0	Assuming the forward voltage of each diode is 1 V
MOSFET	(W)	2.7	Assuming that R _{ds(on)} doubles at the highest junction temperature of your application
Diode	(W)	0.6	Assuming that the diode forward voltage is 1 V

Oscillator Capacitor

C _{osc}	(pF)	155	
------------------	------	-----	--

On-time Adjust Circuitry

C ₂	(nF)	7.6	
R _{drv2}	(kΩ)	5.5	

Feed-back and OVP arrangements

R _{b2} , R _{ovp2}	(kΩ)	27	You can choose 27 k by default
r ₁ , R ₁	(kΩ)	1000	
r ₂ , R ₂	(kΩ)	1000	
R ₃	(kΩ)	500	
R _{b1}	(kΩ)	4100	
R ₄	(kΩ)	500	
R _{ovp1}	(kΩ)	4400	
C _{comp}	(nF)	500	

Input Voltage Sensing

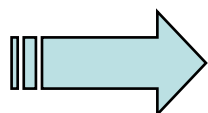
R _{ds2}	(kΩ)	82	
r ₇	(kΩ)	1000	
r ₈	(kΩ)	1000	
r ₉	(kΩ)	1000	
r ₁₀	(kΩ)	1000	
R _{drv1}	(kΩ)	7210	
C _{bo}	(nF)	150	

Current Sense Network

R _{sense}	(Ω)	0.15	Value that makes the Reverse dissipation = 0.5% * P _{out}
R _{drv1}	(Ω)	0.15	Your "Reverse" choice
P _{Reverse}	(W)	1.0	Losses resulting from your Reverse choice
R _{drv2}	(Ω)	3.1	Value resulting from your Reverse choice
R _{drv1}	(Ω)	9	Value resulting from your Reverse choice
R _{drv1}	(Ω)	25	Value resulting from your Reverse choice

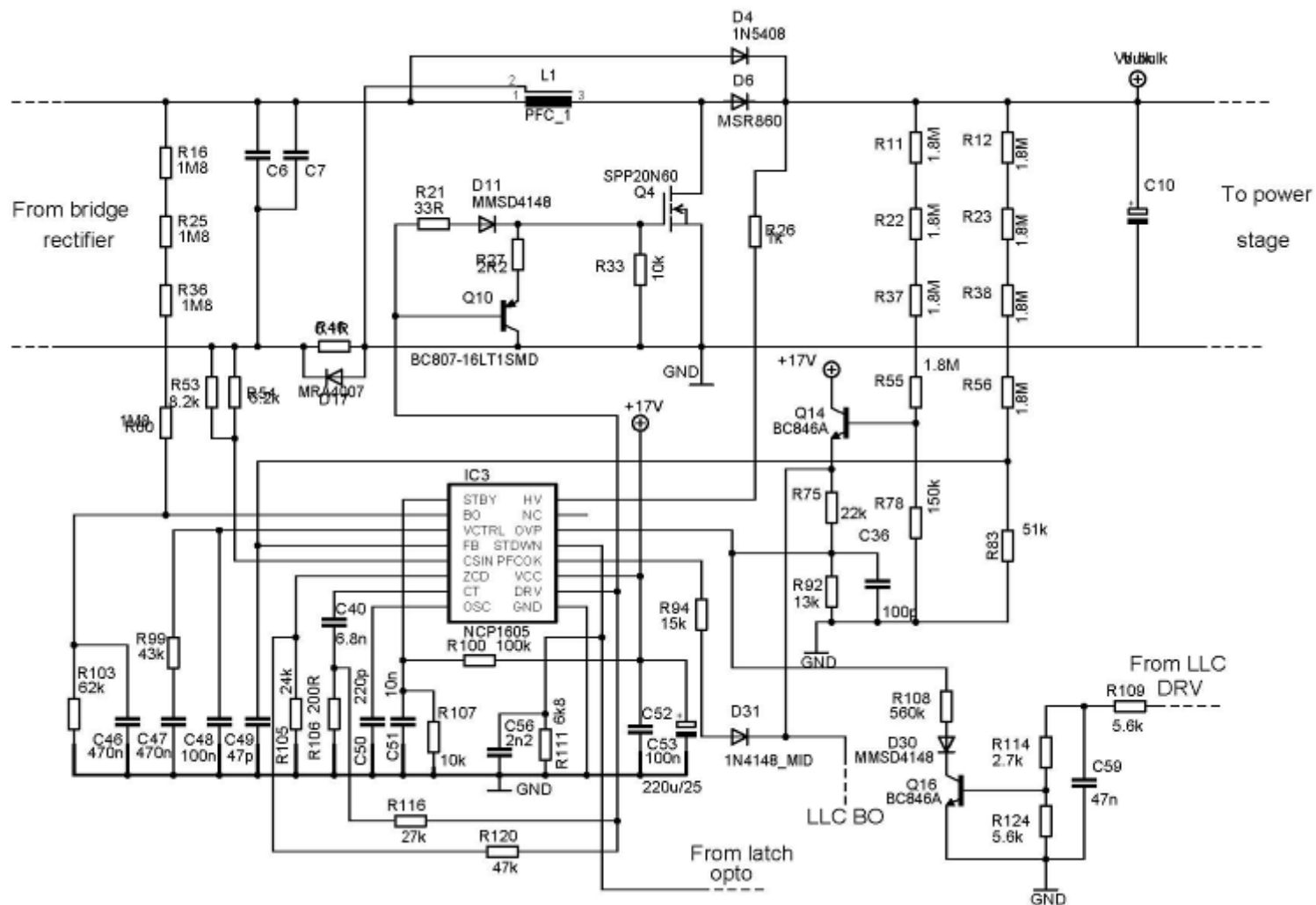
Generic NCP1605 Application Schematic

The schematic diagram illustrates the NCP1605 application. It features an AC input line connected to a bridge rectifier. The positive output of the bridge is connected to an EMI filter, which then feeds into a power MOSFET (M1) through an inductor L1. The MOSFET's drain is connected to the output filter capacitor Cbulk and the output diode D1. The MOSFET's gate is driven by a driver circuit (DRV) that includes a current sense resistor R_{sense} and a feedback network consisting of resistors R_{b1}, R_{b2}, R_{ovp1}, R_{ovp2}, and R_{drv1}, R_{drv2}. The MOSFET's source is connected to the negative terminal of the bulk capacitor Cbulk and the negative output terminal. The MOSFET's body diode is connected to the negative output terminal. The MOSFET's gate is also connected to a feedback network consisting of resistors R_{b1}, R_{b2}, R_{ovp1}, R_{ovp2}, and R_{drv1}, R_{drv2}. The MOSFET's gate is also connected to a feedback network consisting of resistors R_{b1}, R_{b2}, R_{ovp1}, R_{ovp2}, and R_{drv1}, R_{drv2}.



200 μH PFC电感保持低工作频率=>减小电磁干扰
200 μH PFC inductor keeps low operating frequency => EMI impact

PFC段电路图 PFC stage schematic



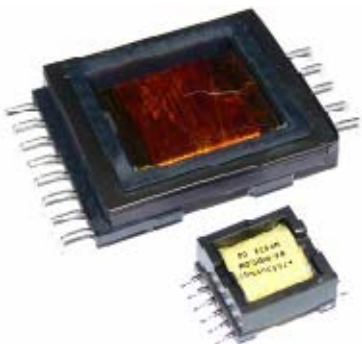
议程 Agenda

- EPA能效要求 EPA efficiency requirements
- 参考设计目标 Reference design goals
- 拓扑结构选择 Topology selection
- PFC段设计 PFC stage design
- **LLC段设计** LLC stage design
- 同步整流(SR)设计 SR design
- 待机管理及协调 Standby management and handshaking
- 参考设计性能 Reference design performance
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谐振电感位置？

Resonant inductance location?

外部电感 External inductance



优势 Benefits:

- 设计灵活性更高 Greater design flexibility
- EMI辐射更低 Lower radiated EMI emission
- 利用变压器绕组 Transformer winding utilization
- 有可能使用谐振线圈上的辅助绕组来感测初级电流，用于过流保护 Possibility to use aux. winding on resonant coil to sense primary current for OCP

不足 Drawbacks:

- 绕组冷却条件较差 Worse windings cooling
- 初级至次级绝缘的实现更复杂 Primary to secondary insulation is more complex to achieve

内部泄漏电感 Internal leakage inductance

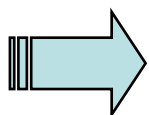


优势 Benefits:

- 初级至次级绝缘易于实现 Primary to secondary insulation is easy to achieve
- 绕组冷却条件更佳 Better cooling for windings
- 仅一颗元件 One component only

不足 Drawbacks:

- 设计灵活性较低 Less design flexibility
- 存在EMI辐射问题 EMI radiation
- 漂移磁通导致开关电源金属表面涡流问题 Eddy currents in SMPS metal cover due to stray flux
- 单纯的绕组窗口利用 Pure winding window utilization



外部谐振线圈更适合超薄设计 External resonant coil is better for ultra slim design

LLC谐振储能元件参数 LLC resonant tank parameters

选择方案：标准变压器+外部谐振电感

Selected solution: Standard transformer + external resonant inductance

变压器Transformer: 初级电感 Primary inductance $L_m = 430 \mu\text{H}$

漏电感 Leakage inductance $L_{lk} = 55 \mu\text{H}$

初级与次级匝数比 Turn ratio prim. to sec. $n = 17.5$

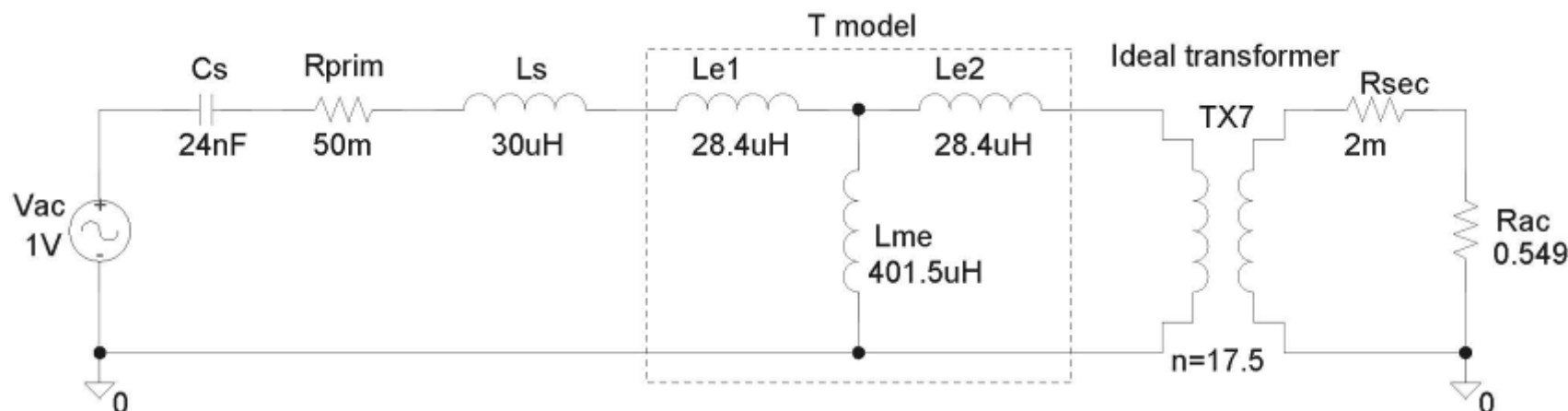
初级与辅助绕组匝数比 Turn ratio prim. to aux. $n_{aux} = 11.6$

谐振线圈 Resonant coil: $L_s = 30 \mu\text{H}$

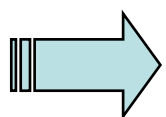
谐振电容 Resonant capacitor: $C_s = 2 \times 12 \text{ nF}$

LLC谐振储能元件模型 LLC resonant tank model

- 这设计使用变压器泄漏及外部线圈作为谐振电感 This design uses transformer leakage and external coil as resonant inductance
- 能使用T模型 T model can be used



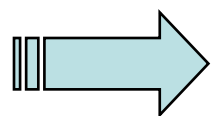
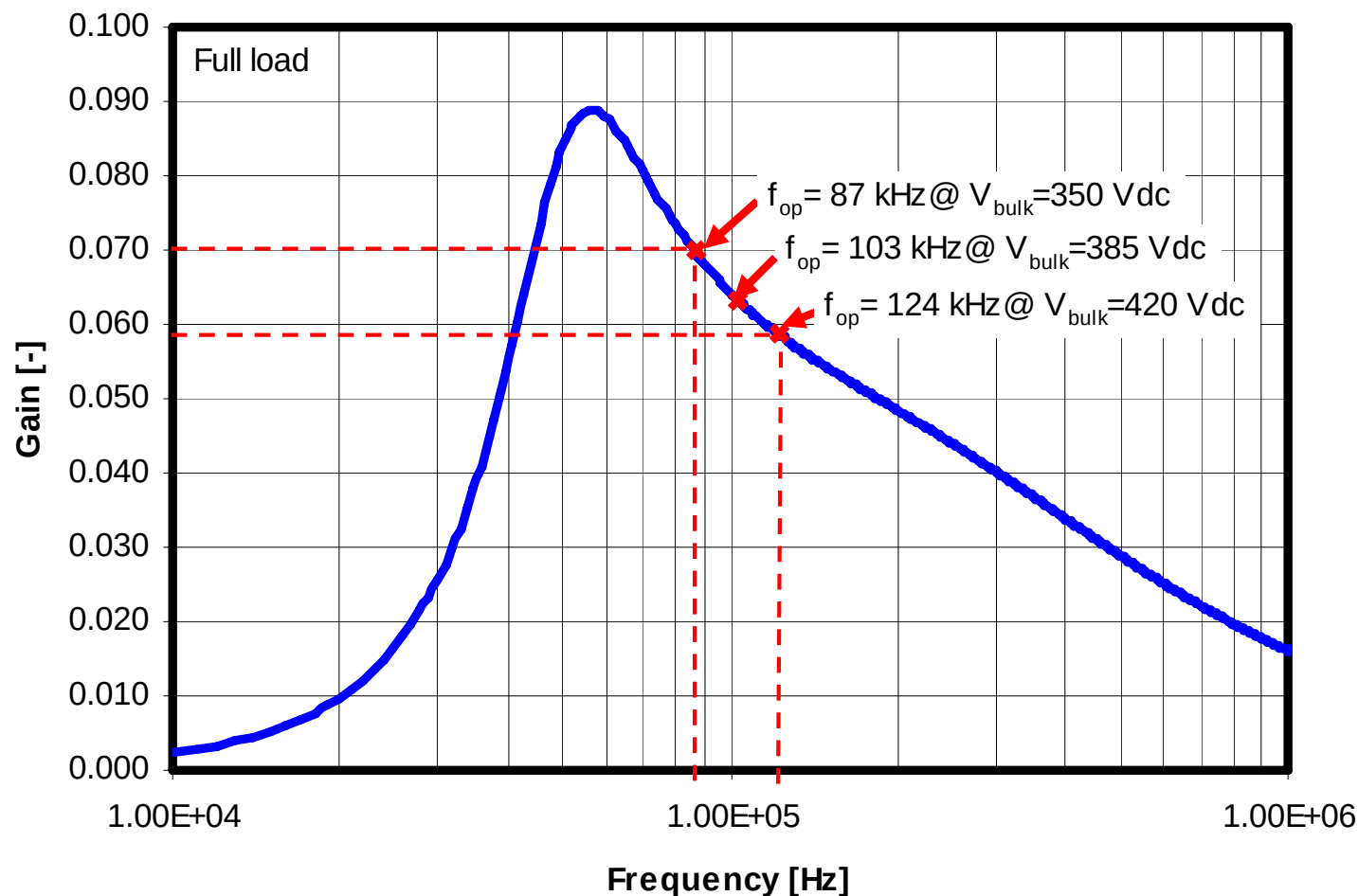
$$k = \sqrt{1 - \frac{L_{lk}}{L_m}} \quad \begin{aligned} L_{e1} &= L_{e2} = (1 - k) \cdot L_m \\ L_{me} &= k \cdot L_m \end{aligned}$$



T模型反映的事实是Lm也参与谐振=>变压器增益下降

T model reflects the fact that Lm also participates on resonance => transformer gain impact

LLC段增益特性曲线 LLC stage gain characteristic

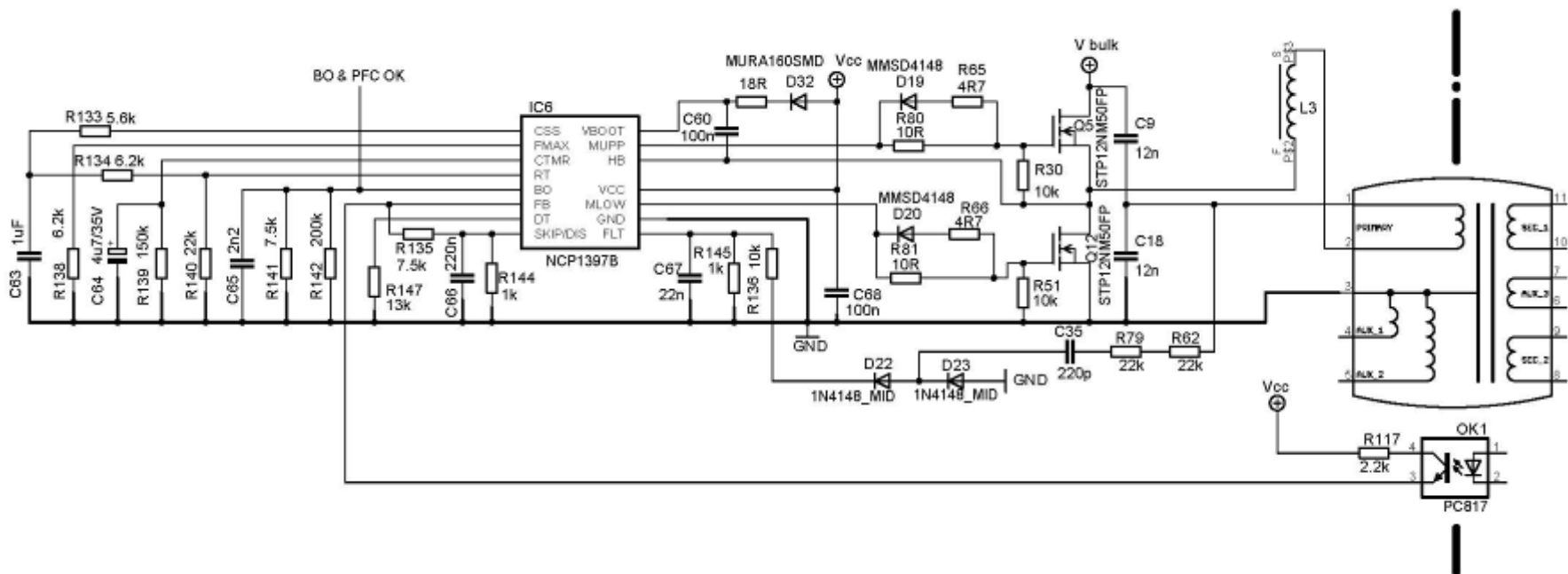


所选谐振储能元件提供狭窄的工作频率范围

Selected resonant tank provides narrow operating frequency range

LLC初级端电路图

LLC primary side schematic



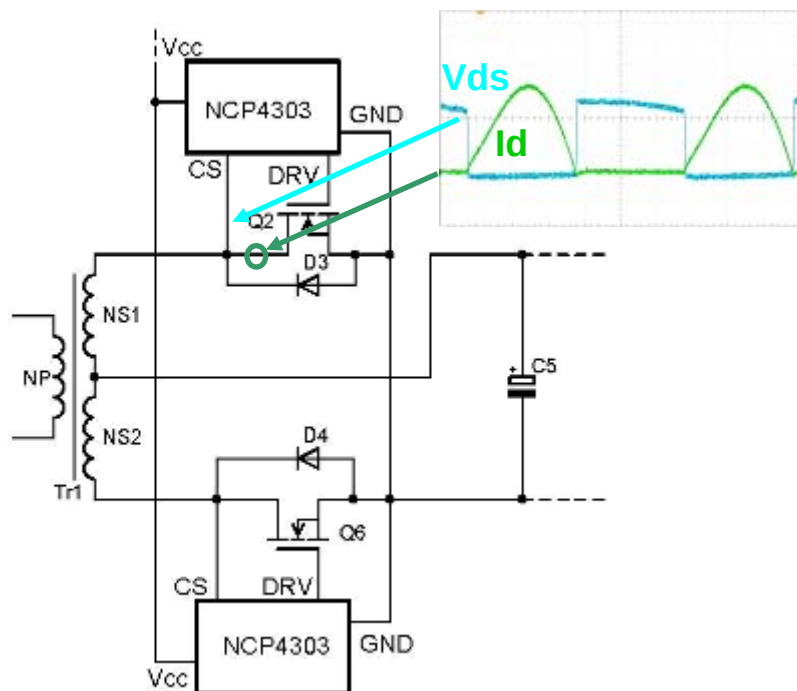
NCP1397应用双过流保护(OCP)及跳周期模式简化LLC段设计

NCP1397 simplifies LLC stage design by implementing dual OCP and skip mode

议程 Agenda

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同步整流(SR)设计 SR design



同步整流(SR)控制器在待机模式下的能耗及门极驱动损耗可能影响待机能耗 SR controllers consumption and gate drive losses in standby would hamper standby efficiency

⇒在待机模式关闭整个同步整流系统很重要
It is critical to turn off whole SR system in standby mode

同步整流MOSFET损耗 SR MOSFET losses:

- 导电损耗 Conduction losses

$$P_{cond} = \left(I_{out} \cdot \frac{\pi}{4} \right)^2 \cdot R_{ds_on}$$

⇒ 选择导通阻抗 R_{ds_on} selection

- 门驱动损耗 Gate drive losses

$$P_{drv} = Q_g \cdot F_{sw} \cdot V_{CC}$$

⇒ 选择门电荷 gate charge selection

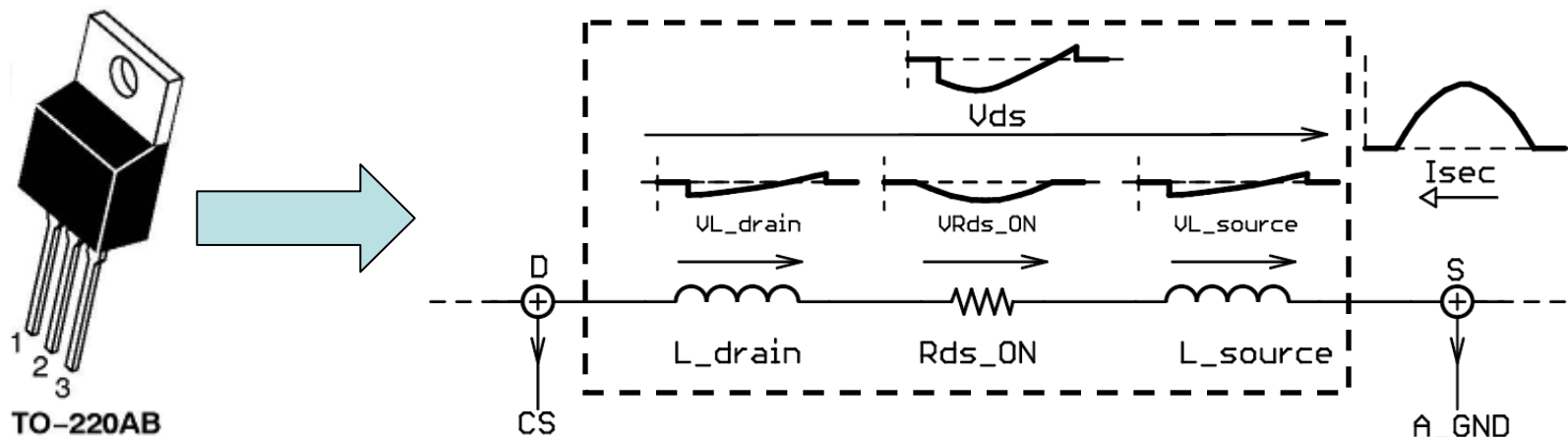
- 体二极管损耗 Body diode losses

$$P_{body} = \frac{I_{out}}{2} \cdot V_f + \left(I_{out} \cdot \frac{\pi}{4} \right)^2 \cdot R_{dyn}$$

⇒ 受二极管正向电压、动态电阻和寄生电感影响，要使用外部肖特基二极管 Affected by diode V_f , dynamic resistance and parasitic inductance, external Schottky to be used

同步整流-封装寄生电感 SR – package parasitic inductance

- 因成本及焊接工艺简单缘故，TO220封装最常用 TO220 package is mostly used due to cost and also simple soldering process



- 寄生电感 L_{drain} 及 L_{source} 产生正比于次级电流 $I_{sec(t)}$ 导数的压降 Parasitic inductances L_{drain} and L_{source} create voltage drop that is proportional to the secondary current $I_{sec(t)}$ derivative.
- V_{ds} 电压比次级电流先达到零电平 The V_{ds} voltage reaches zero level prior secondary current
- 同步整流控制器检测到零电压时次级电流仍有明显电平=>能效降低 SR controller detects zero voltage in the time the secondary current has still significant level => efficiency degradation
- 频率及 $dI_{sec(t)}/dt$ 越高，能效下降得越多 Higher frequency or $dI_{sec(t)}/dt$ is, higher efficiency drop will be

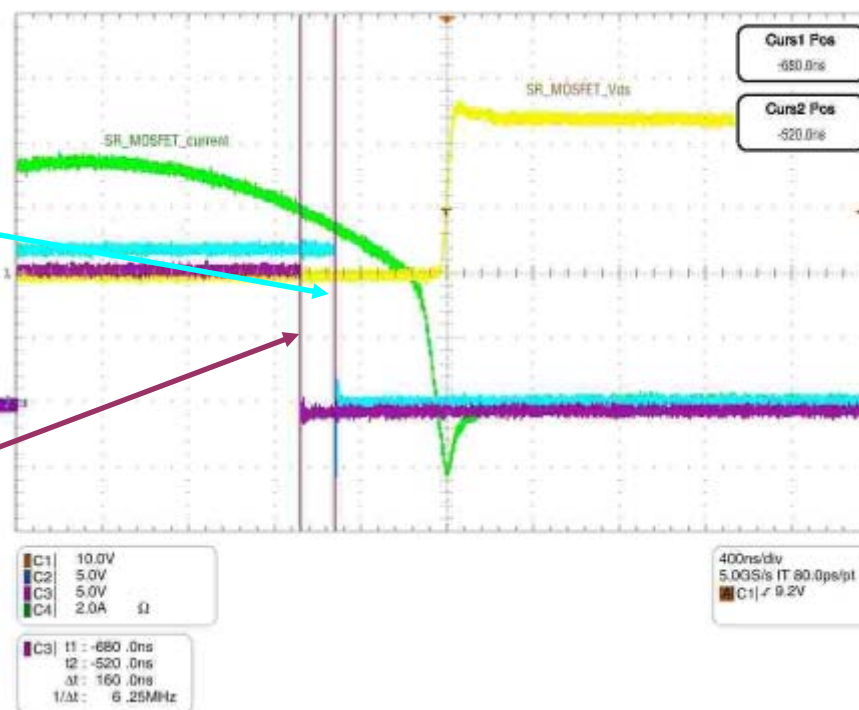
同步整流设计-封装寄生电感

SR design – package parasitic inductance

- 使用了极低导通阻抗的MOSFET时，这个问题变得很严重 This issue becomes really serious when very low R_{ds_on} MOSFET is used

同步整流控制 SR controller
with $V_{th_zcd} = 0\text{ mV}$

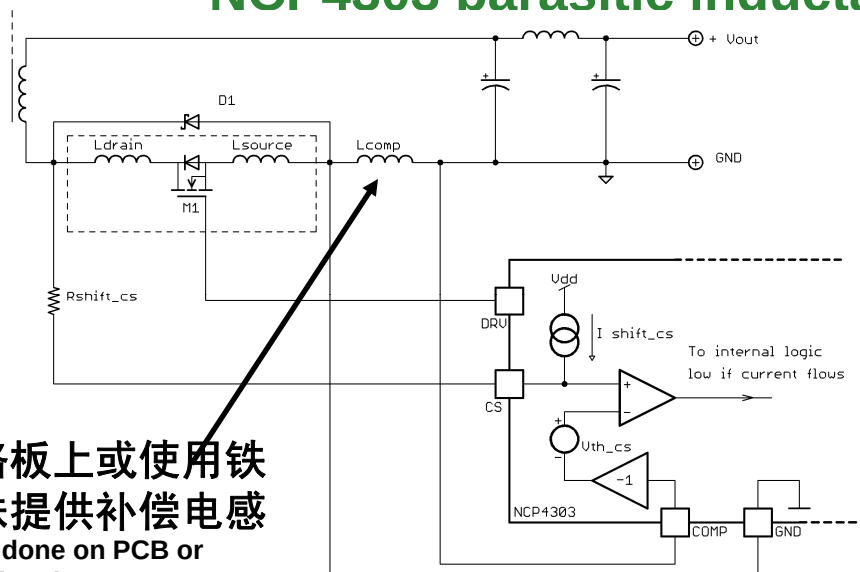
同步整流控制器 SR controller
with $V_{th_zcd} = -5\text{ mV}$



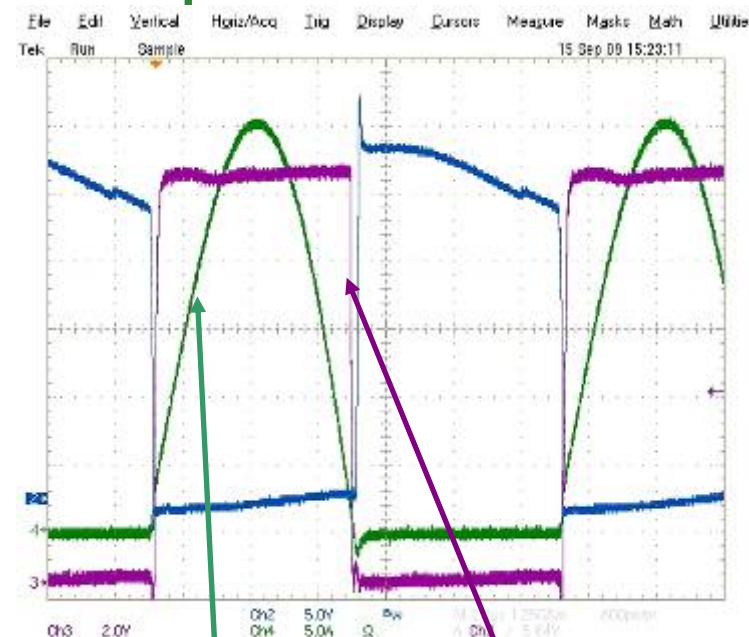
零电流检测(ZCD)阈值为0 V的同步整流控制器提供更长的同步整流MOSFET导电时间 SR controller with 0 mV ZCD threshold provides longer conduction period for SR MOSFET

NCP4303寄生电感补偿

NCP4303 parasitic inductance compensation

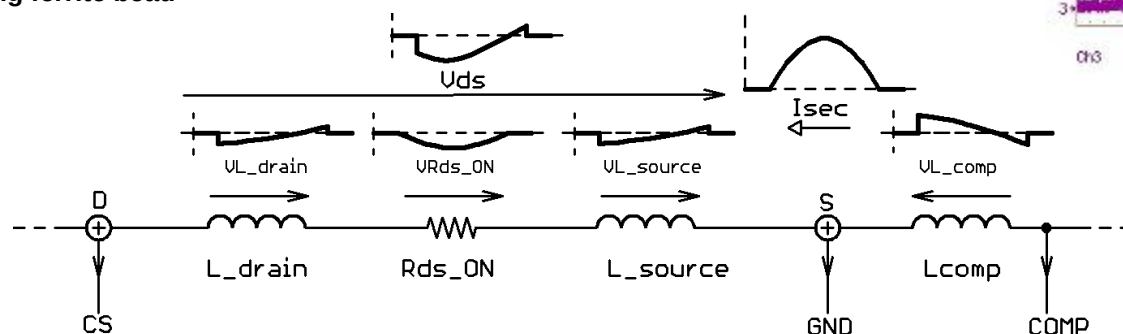


能在电路板上或使用铁氧体磁珠提供补偿电感
 L_{comp} can be done on PCB or using ferrite bead



次级电流
Secondary current

SR MOSFET门电压
SR MOSFET gate voltage



NCP4303应用了补偿电感时，同步整流MOSFET导电周期延至最长
 SR MOSFET conduction period is maximized when NCP4303 implemented with compensation Inductance

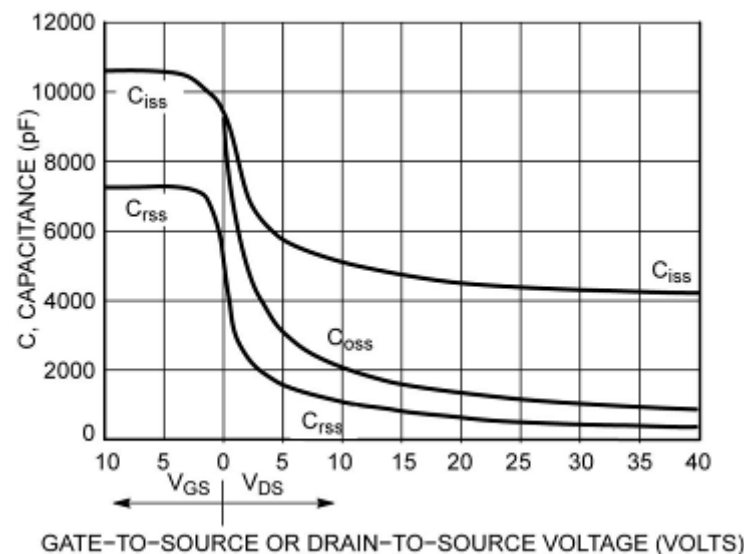
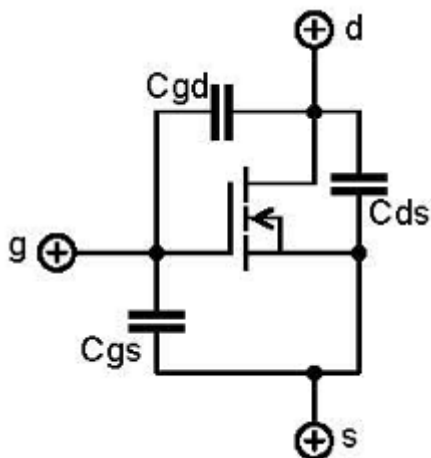
注:专利待批 Note: Patent pending

注: 本电路板版本中未使用寄生电感补偿 Note: Parasitic inductance compensation not used in this PCB version

同步整流(SR)设计-MOSFET选择

SR design – MOSFET selection

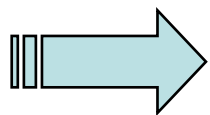
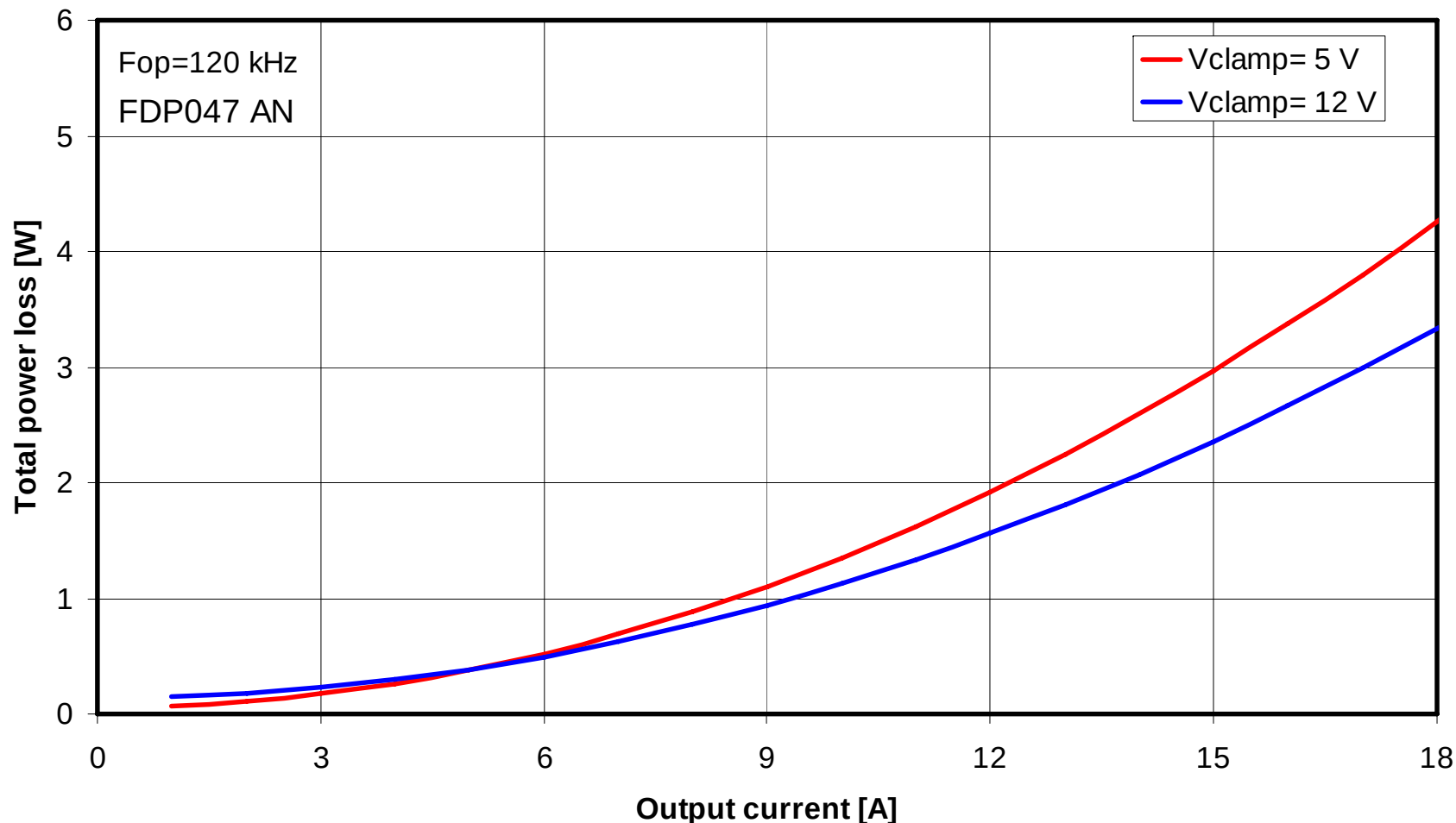
- 同步整流MOSFET工作在零电压开关条件 SR MOSFET works under ZVS conditions
=> 门电荷由Ciss电容($C_{gs}+C_{gd}$)和门电压决定 Gate charge is given by Ciss capacitance ($C_{gs}+C_{gd}$) and gate voltage



MOSFET 类型 type	Qg @ 5 V [nC]	Qg @ 12 V [nC]	Rds_on @ 5V [mW]	Rds_on @ 12V [mW]
IPP015N04N	101	245	1.9	1.2
FDP047AN	39	96	5.8	4
IRFB3206	55	133	3.3	2.3

同步整流(SR)设计-门电压钳位选择

SR design – gate voltage clamp selection

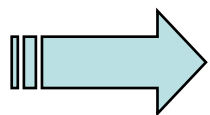
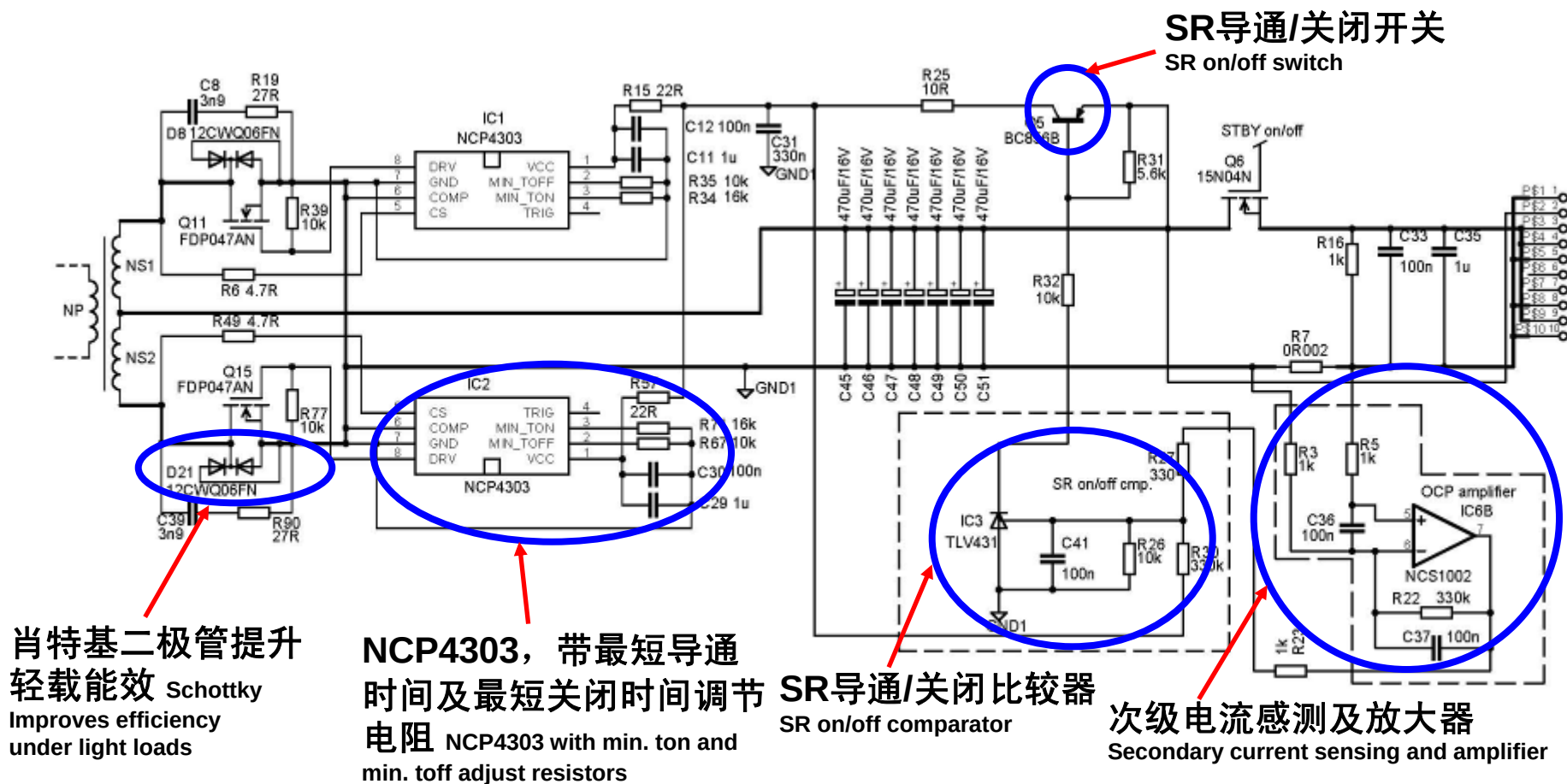


将使用带12 V门电压的NCP4303

NCP4303 with 12 V gate voltage clamp to be used

同步整流(SR)最终电路图, 带SR导通/关闭功能

SR final schematic with SR turn on/off



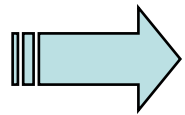
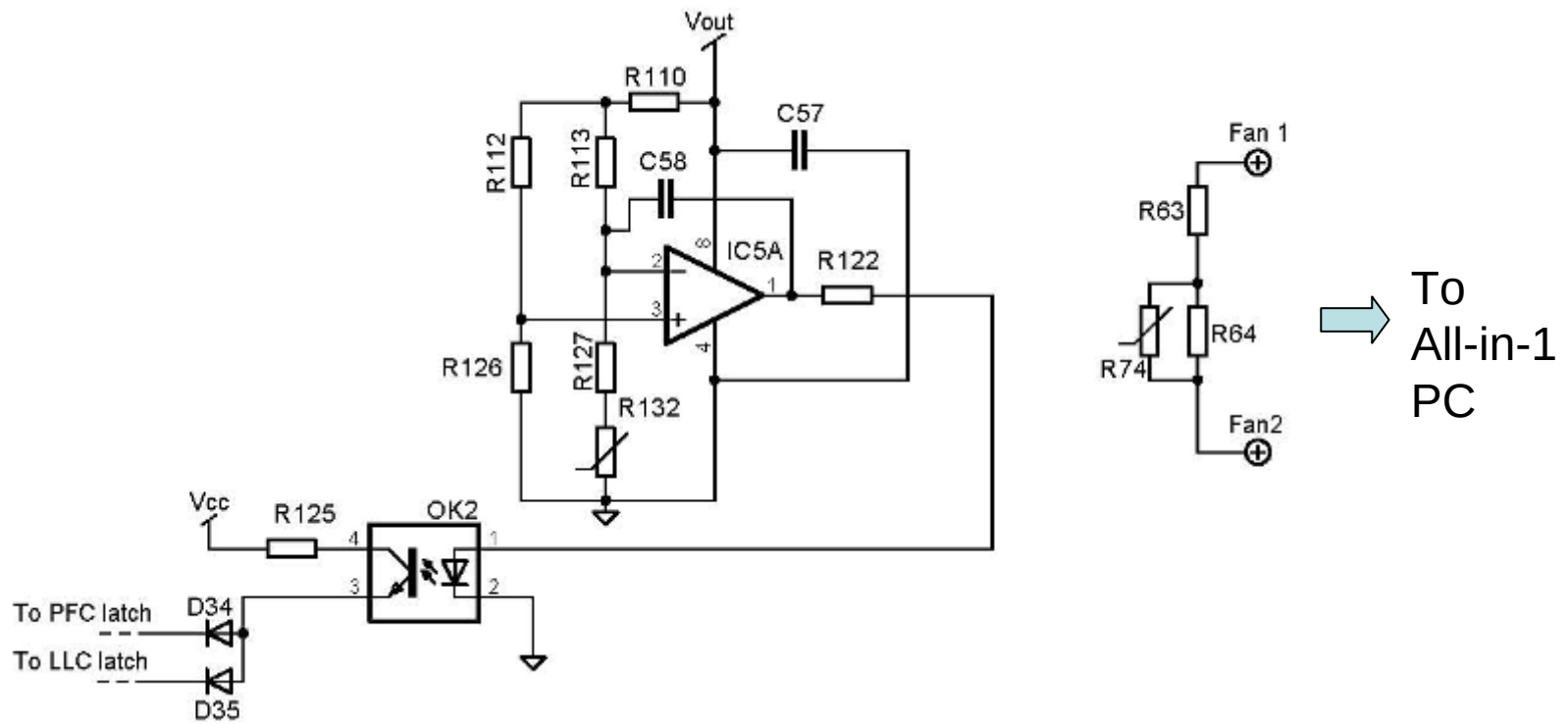
简单、高性价比地应用同步整流

Simple and cost effective SR implementation

议程 Agenda

- EPA能效要求 EPA efficiency requirements
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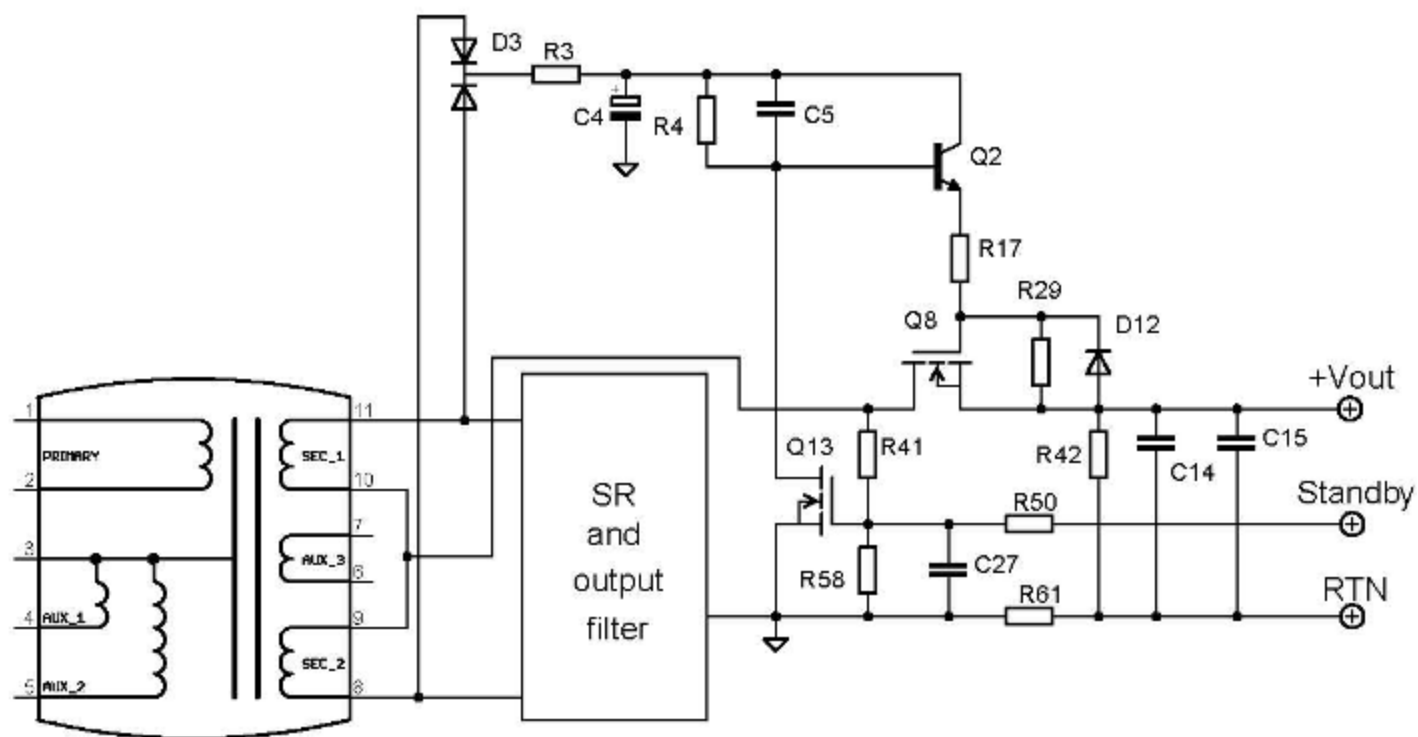
过温保护 OTP



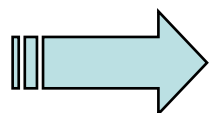
出现温度过高时无论PFC或是LLC都会闩锁关闭
Either PFC or LLC can be latched-off in case of overtemperature

电源端子导通/关闭

Power terminal on/off



连接至
一体式电脑
To All-in-1 PC

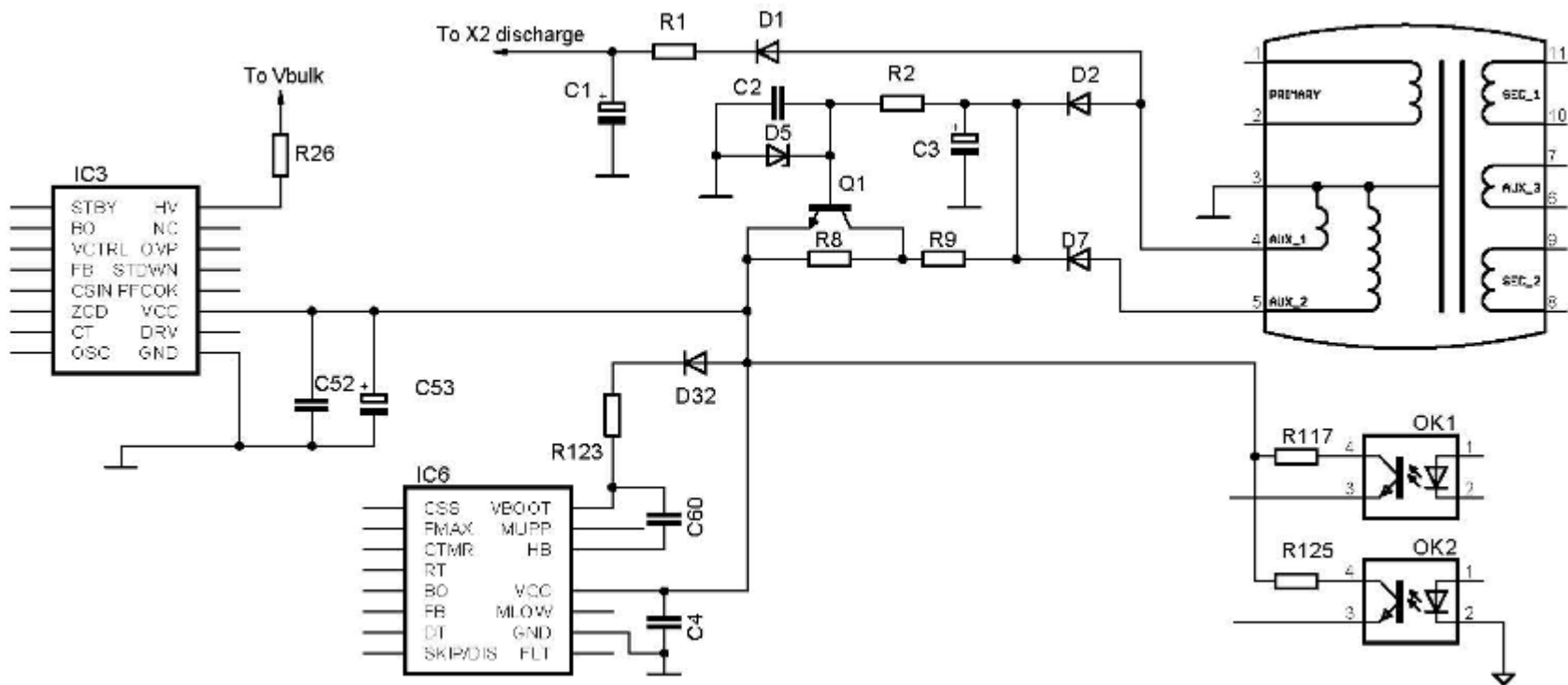


N MOSFET提供低导通阻抗

N MOSFET provides low R_{ds_on}

初级偏置 Primary biasing

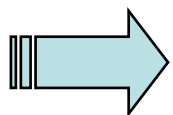
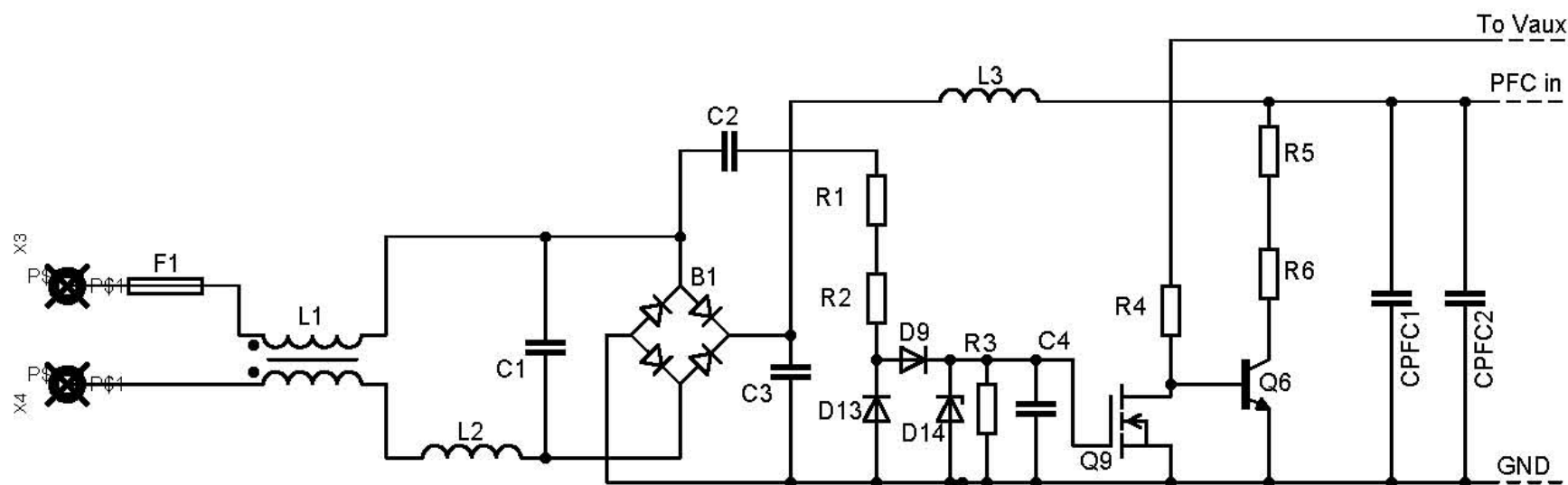
- **一体机应用需要高压启动功能** HV startup is needed for All-in-1 application



NCP1605简化初级偏置

X2电容放电电路 x2 capacitor discharge circuitry

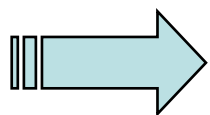
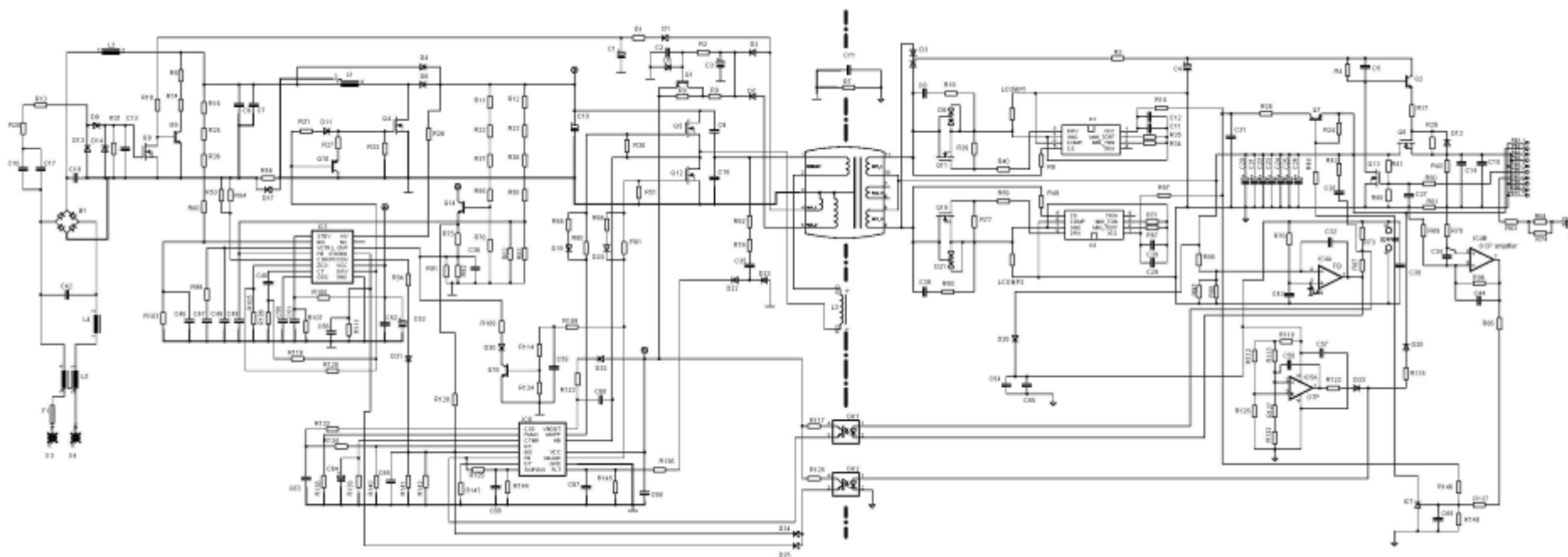
- 强制要求在应用从主电源插座拔出后给X2电容放电 It is mandatory to discharge X2 cap after is application unplugged from mains
- X2放电电阻增加待机能耗 X2 discharge resistor increases standby consumption



电荷泵移除X2电容放电电阻，帮助降低待机输入能耗

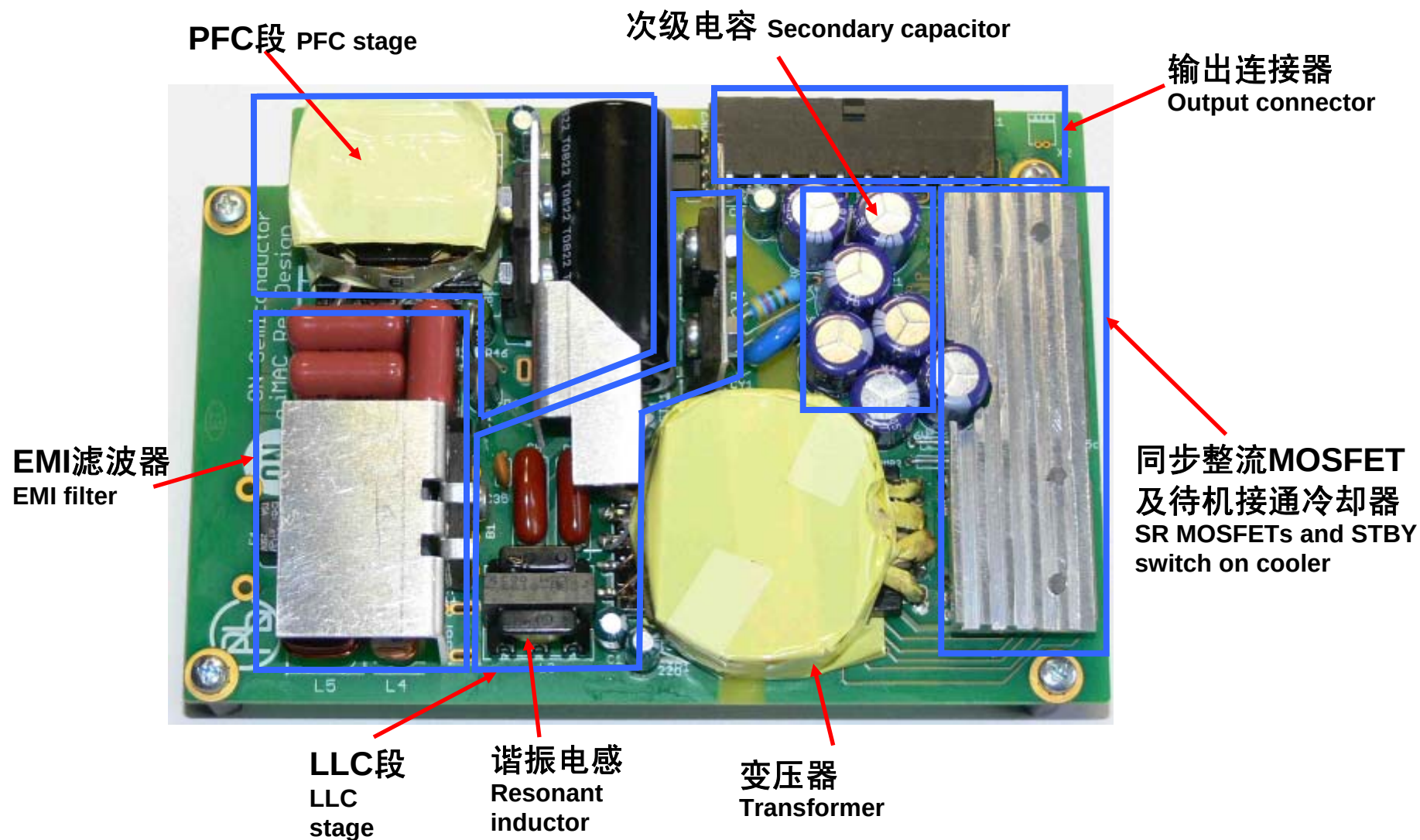
Charge pump helps to decrease standby input power by removing X2 cap. discharge resistor

总电路板电路图 Total board schematic



安森美半导体提供的完整一体机电源方案
Full All-in-1 solution from ON semiconductor

参考设计图片-顶视图 Reference design photo – top side



参考设计图片-底视图

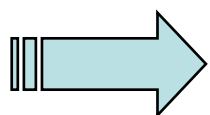
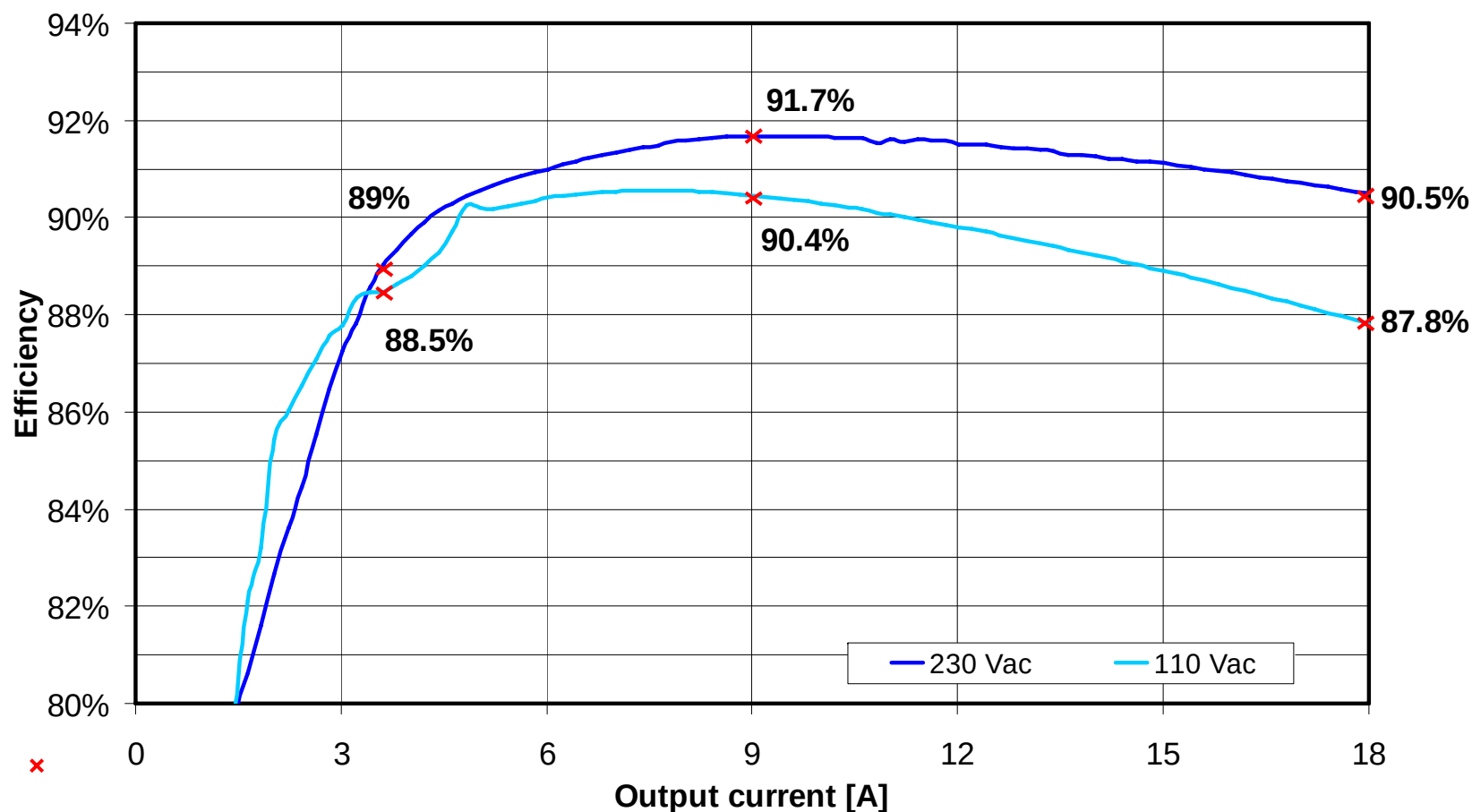
Reference design photo – bottom side



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开关电源能效图 SMPS efficiency charts

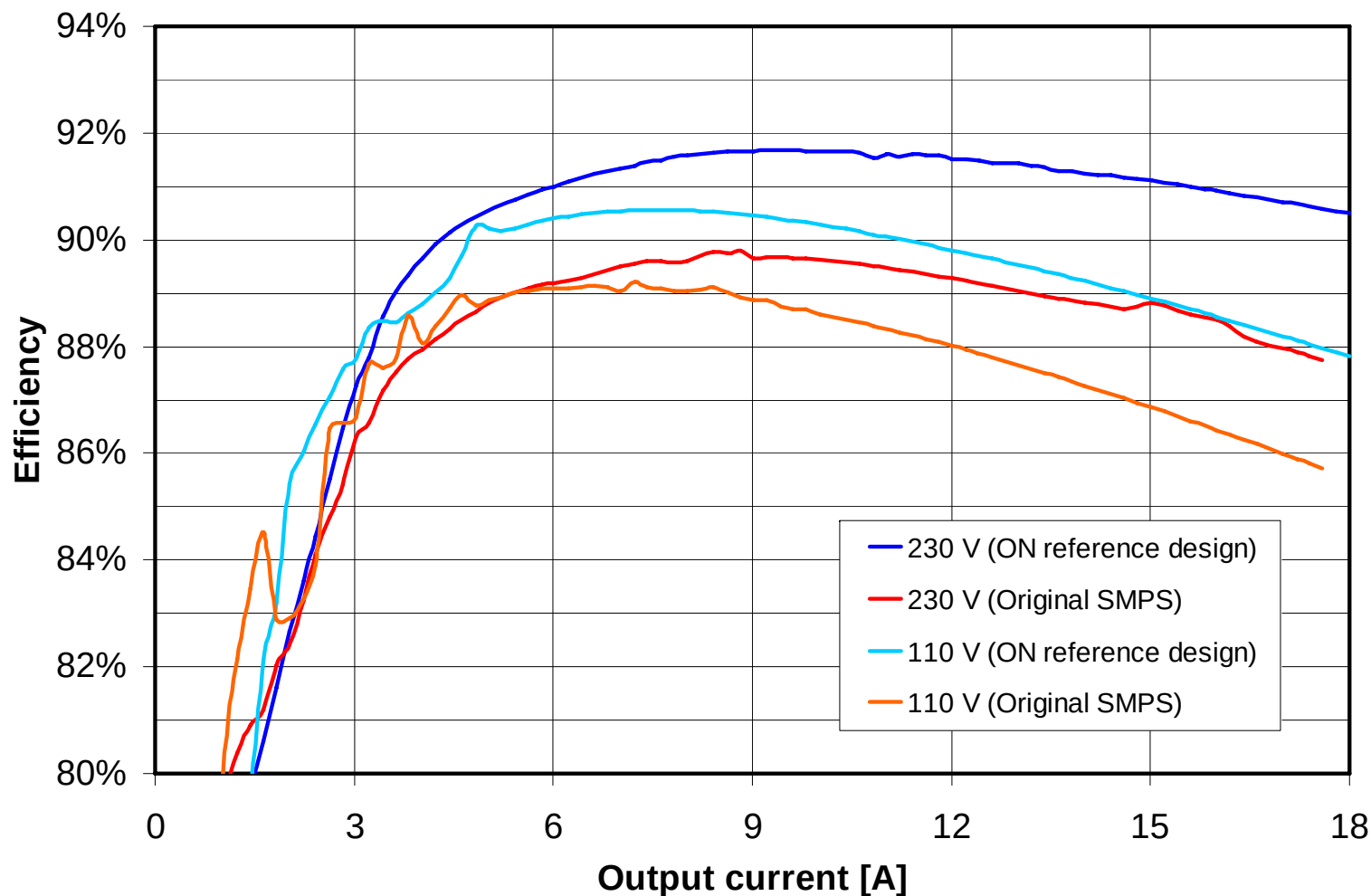


参考设计满足80 PLUS银级能效规范

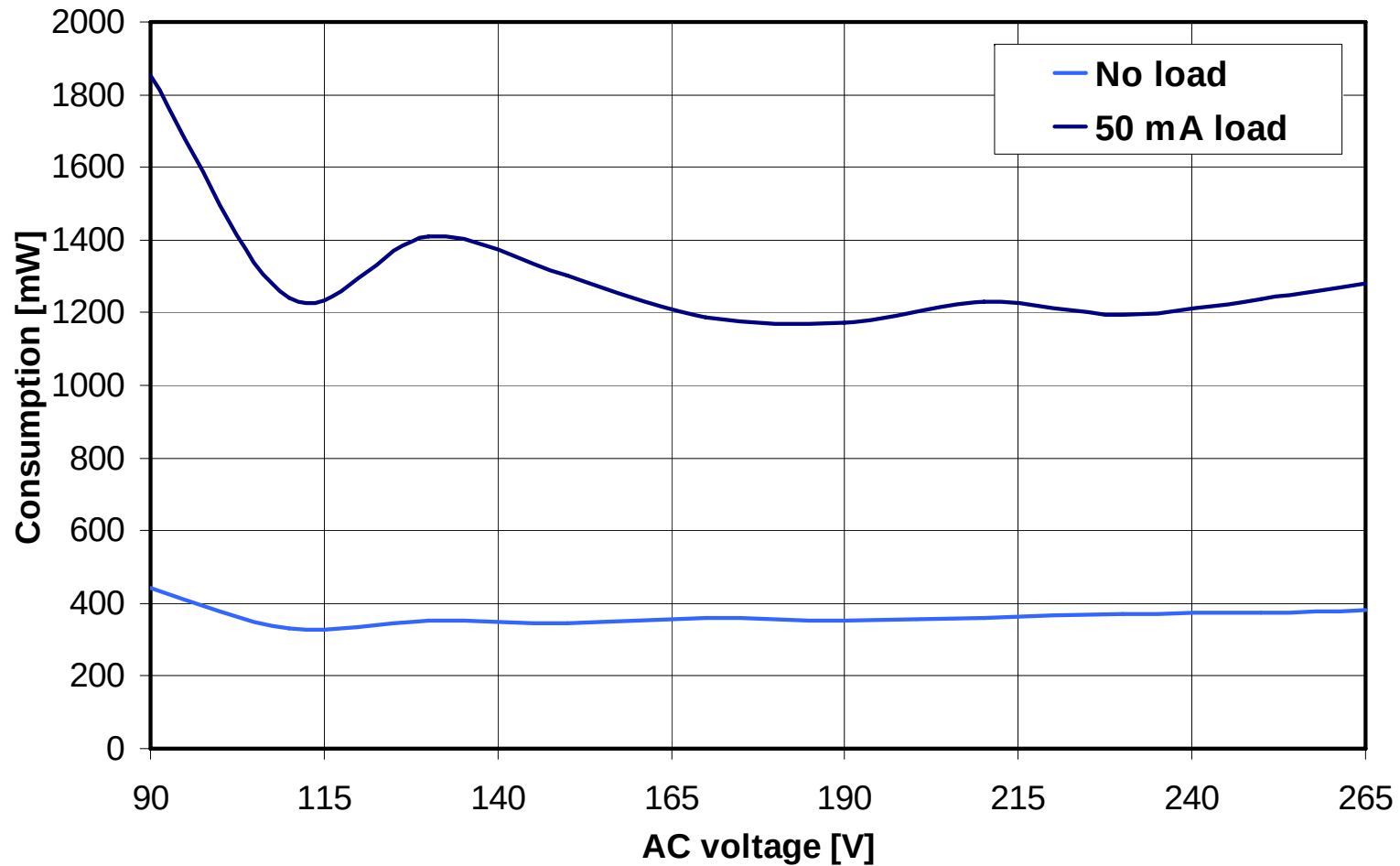
Reference design meets 80+ silver specification

开关电源能效图，与不带同步整流的原方案比较

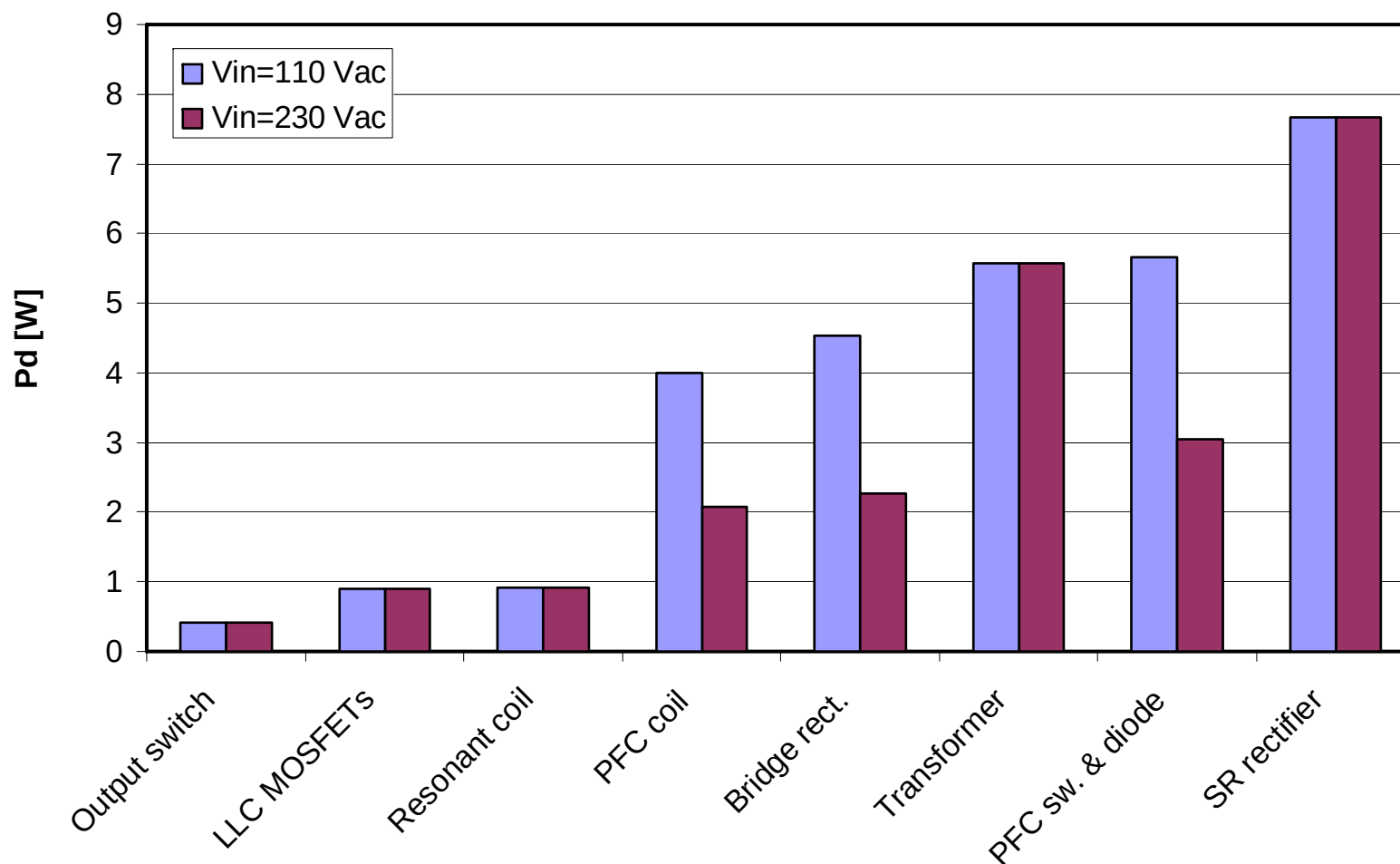
SMPS efficiency charts, comparison with original solution without SR



轻载能效 Light load efficiency



具体损耗来源分布 Detail losses distribution



后续工作 Future work

- 在同步整流段应用寄生电感补偿，从而进一步提升能效
Implement parasitic inductance compensation in SR stage and thus further boost the efficiency.
- 使用不同的同步整流MOSFET及门钳位电压，降低驱动损耗
Use different SR MOSFET(s) and gate clamp voltage to reduce driving losses.
- 进一步优化PFC段能效 Further optimization of the PFC stage efficiency
- 提升能效，满足80 PLUS金级能效规范 Boost efficiency to meet 80+ gold specification ☺

总结 Summary

- 安森美半导体现已提供高能效的80 PLUS银级能效参考设计 High efficient 80+ silver reference design from ON is now available!!
- 由NCP1605驱动的FCCrM PFC段提供极佳的能效结果，并将PFC电感尺寸减至最小。这控制器的“pfcOK”信号及跳周期模式特性简化了一体式计算机开关电源的设计 FCCrM PFC stage driven by NCP1605 provides excellent efficiency results and minimizes PFC inductor size. PFC OK signal and skip mode featured in this controller simplifies design of All-in-1 PC SMPS
- 由NCP1397驱动的LLC电源段提供高能效、跳周期模式能力及低成本的过流保护(OCP)应用 LLC power stage driven by NCP1397 provides high efficiency, skip mode capability and cheap OCP implementation
- 由NCP4303驱动的同步整流器将同步整流MOSFET导电时间延至最长，从而提升能效至最高。这驱动器的电压钳位功能减小驱动损耗 Synchronous Rectifier driven by NCP4303 maximize the SR MOSFET conduction time – thus maximize efficiency. Voltage clamp on the driver reduces driving losses
- 安森美半导体提供这参考设计及所提及IC的完整支援 ON Semiconductor provides full support on this reference design and mentioned ICs

For More Information

- View the extensive portfolio of power management products from ON Semiconductor at www.onsemi.com
- View reference designs, design notes, and other material supporting the design of highly efficient power supplies at www.onsemi.com/powersupplies