

CS2001

1.2 A Switching Regulator, and 5.0 V, 100 mA Linear Regulator with RESET

The CS2001 is a smart power supply ASIC utilized in automotive airbag systems. It contains a current-mode switching regulator with a 1.2 A on-chip switch and a 5.0 V, 100 mA linear regulator. The linear output capacitor must be 3.3 μ F or greater with an ESR in the range of 100 m Ω to 1.0 Ω . If the ESR of the cap is less than 100 m Ω , a series resistor must be used. The switcher can be configured in either a boost or flyback topology. The boost topology produces energy reserve the resistor divider connected to the V_{FB} pin. In the event of fault voltage V_{ER} which is externally adjustable (25 V maximum) through conditions that produce V_{FB} either open or shorted, the switcher is shut down.

Under normal operating conditions ($V_{BAT} > 8.0$ V), the current loading on the linear regulator is directed through V_{BAT} . A low battery or loss of battery condition switches the supply for the linear regulator from V_{BAT} to V_{ER} and shuts down the switcher using the ASIC's internal smart switch. This switchover feature minimizes the power dissipation in both the linear and switcher output devices and saves the cost of using a larger inductor.

The NERD (No Energy Reserve Detected) pin is a dual function output. If V_{OUT} is not in regulation, it provides a Power On Reset function whose time interval is externally adjustable with the capacitor. This interval can be seen on the RESETB pin, which allows for clean power-up and power-down of the microprocessor. Once V_{OUT} is in regulation, the logic level of the NERD output (usually low) indicates to the microprocessor whether or not the V_{ER} pin is connected.

A switched-capacitor voltage tripler accepts input voltage V_{ER} and produces output voltage V_{CHG} (typically $V_{ER} + 8.0$ V). This voltage is used in the system to drive high-side FETs.

This part is capable of withstanding a 50 V peak transient voltage. The linear regulator will not shut down during this event.

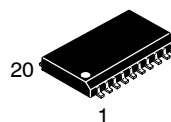
Features

- Linear Regulator 5.0 V $\pm 2\%$ @ 100 mA
- Switching Regulator 1.2 A Peak Internal Switch
- Voltage Tripler
- Smart Functions
 - Smartswitch
 - RESET
 - Energy Reserve Status
- Protection
 - Overtemperature
 - Current Limit
 - 50 V Peak Transient Capability
- Internally Fused Leads in SO-20L Package



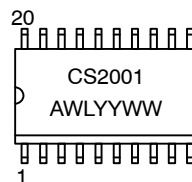
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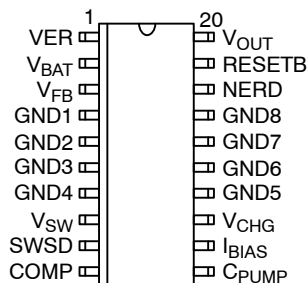
SO-20L
DWF SUFFIX
CASE 751D

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping
CS2001YDWF20	SO-20L	37 Units/Rail
CS2001YDWFR20	SO-20L	1000 Tape & Reel

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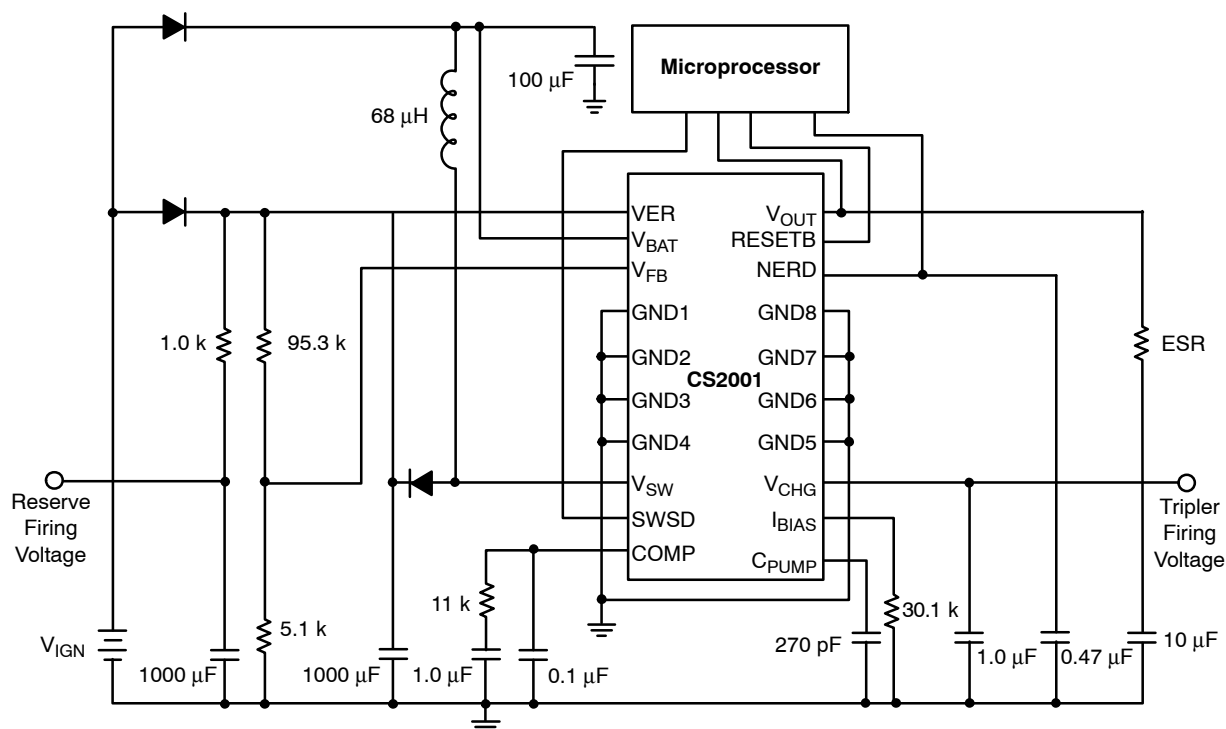


Figure 1. Application Diagram

ABSOLUTE MAXIMUM RATINGS*

Rating	Value	Unit
V _{BAT}	-0.5 to 25	V
VER	-0.5 to 25	V
V _{OUT}	-0.5 to 7.0	V
Digital Input/Output Voltage	-0.5 to 7.0	V
Peak Transient Voltage (36 V Load Dump @ 14 V Battery Voltage)	50	V
Storage Temperature Range	-55 to 150	°C
Junction to Free Air Thermal Impedance	55	°C/W
ESD Susceptibility (Human Body Model)	4.0	kV
Lead Temperature Soldering:	Reflow: (SMD styles only) (Note 1)	230 peak
T _A	-40 to 85	°C
T _J	-40 to 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

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ELECTRICAL CHARACTERISTICS ($8.0\text{ V} \leq V_{\text{BAT}} \leq 16\text{ V}$, $8.0\text{ V} \leq V_{\text{ER}} \leq 25\text{ V}$, $1.0\text{ mA} \leq I_{\text{V(OUT)}} \leq 100\text{ mA}$,
 $T_{\text{TEST}} = -40^{\circ}\text{C}$ to 125°C ; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
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Linear Regulator

Output Voltage	Output Driven from V_{BAT} , $V_{\text{ER}} = 25\text{ V}$ Output Driven from V_{ER} , $V_{\text{BAT}} = 0\text{ V}$	4.9 4.9	– –	5.1 5.1	V V
Regulator Bias Current (from V_{BAT})	$I_{\text{V(BAT)}}$ @ $I_{\text{V(OUT)}} = -100\text{ mA}$, SWSD = 4.0 V , $V_{\text{BAT}} = 16\text{ V}$, $V_{\text{ER}} = 25\text{ V}$ $T = -40^{\circ}\text{C}$ $T = 25^{\circ}\text{C}$ $T = 125^{\circ}\text{C}$	– – –	– – –	8.0 7.0 6.0	mA mA mA
Regulator Bias Current (from V_{ER})	I_{VER} @ $I_{\text{V(OUT)}} = -100\text{ mA}$, SWSD = 4.0 V , $V_{\text{BAT}} = 0\text{ V}$, $V_{\text{ER}} = 25\text{ V}$ $T = -40^{\circ}\text{C}$ $T = 25^{\circ}\text{C}$ $T = 125^{\circ}\text{C}$	– – –	– – –	11 9.0 8.0	mA mA mA
Dropout Voltage $V_{\text{BAT}} - V_{\text{OUT}}$	$V_{\text{ER}} = 25\text{ V}$, $I_{\text{V(OUT)}} = -100\text{ mA}$ (Probe Only)	–	–	1.5	V
Dropout Voltage $V_{\text{ER}} - V_{\text{OUT}}$	$V_{\text{BAT}} = 0\text{ V}$, $I_{\text{V(OUT)}} = -100\text{ mA}$	–	–	1.5	V
Smart Switch Threshold V_{BAT} to V_{ER}	$V_{\text{ER}} = 25\text{ V}$, $I_{\text{V(OUT)}} = -50\text{ mA}$	6.5	–	8.0	V
Smart Switch Threshold Hysteresis	$V_{\text{ER}} = 25\text{ V}$, $I_{\text{V(OUT)}} = -50\text{ mA}$	0.5	–	1.0	V
V_{OUT} Output Noise	$V_{\text{BAT}} = 16\text{ V}$, $V_{\text{ER}} = 25\text{ V}$, $I_{\text{V(OUT)}} = -1.0\text{ mA}$, $C = 10\text{ }\mu\text{F}$, $\text{ESR} = 0.5\text{ }\Omega$	–	–	0.05	V
Line Regulation	–	–	–	0.025	V
Load Regulation	–	–	–	0.025	V
Output Current Limit	–	120	–	–	mA

Switching Regulator

$V_{\text{ER}} = 25\text{ V}$, $I_{\text{V(OUT)}} = -1.0\text{ mA}$

Switching Frequency	$C_{\text{PUMP}} = 270\text{ pF}$, $R_{\text{I(BIAS)}} = 30.1\text{ k}\Omega$	135	150	165	kHz
Pump Drive Current	$\Delta I_{\text{V(BAT)}}$ for $0\text{ A} \leq I_{\text{V(SW)}} \leq 1.2\text{ A}$	–	–	50	mA
Switch Saturation Voltage	$I_{\text{V(SW)}} = 1.2\text{ A}$	–	–	1.6	V
Output Current Limit	–	1.2	–	2.4	A
V_{FB} Regulation	–	1.238	1.27	1.303	V
V_{FB} Input Current	V_{FB} Above Short Low Detection Level	–	–	1.0	μA
V_{FB} Input Shorted Low Detection Level	–	200	250	300	mV
C_{PUMP} Short Detection Threshold	–	200	250	300	mV
Maximum Duty Cycle	–	80	–	95	%
V_{SW} Leakage Current	$I_{\text{V(SW)}}$ @ $V_{\text{SW}} = 50\text{ V}$, SWSD = V_{OUT}	–	–	100	μA

Voltage Tripler

$V_{\text{BAT}} = 16\text{ V}$, $I_{\text{V(OUT)}} = -1.0\text{ mA}$, $C_{\text{CHG}} = 1.5\text{ }\mu\text{F}$

Output Voltage Clamp $V_{\text{CHG}} - V_{\text{ER}}$	$V_{\text{ER}} = 8.0\text{ V}$, $I_{\text{V(CHG)}} = -30\text{ }\mu\text{A}$ $V_{\text{ER}} = 12\text{ V}$, $I_{\text{V(CHG)}} = -90\text{ }\mu\text{A}$	6.25 6.25	8.0 8.0	13 13	V V
Initial Charge Time	$C_{\text{CHG}} = 0.15\text{ }\mu\text{F}$, $V_{\text{ER}} = 8.0\text{ V}$, $V_{\text{CHG}} = 14.25\text{ V}$	–	–	30	ms
Maximum Output Voltage Clamp V_{CHG}	–	25	32.5	40	V
Output Voltage Clamp V_{CHG}	$V_{\text{ER}} = 28\text{ V}$, $I_{\text{V(CHG)}} = 0\text{ }\mu\text{A}$	25	32.5	40	V
Short Circuit Path Current Limit V_{ER} to V_{CHG}	–	–	–	3.0	mA

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ELECTRICAL CHARACTERISTICS (continued) ($8.0\text{ V} \leq V_{\text{BAT}} \leq 16\text{ V}$, $8.0\text{ V} \leq V_{\text{ER}} \leq 25\text{ V}$, $1.0\text{ mA} \leq I_{\text{V(OUT)}} \leq 100\text{ mA}$, $T_{\text{TEST}} = -40^{\circ}\text{C}$ to 125°C ; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
RESETB OUTPUT $V_{\text{BAT}} = 0\text{ V}$					
High Threshold	V_{OUT} Increasing	4.525	4.75	4.85	V
Low Threshold	V_{OUT} Decreasing	4.5	4.65	4.825	V
Hysteresis	–	25	100	200	mV
Output Low Voltage	$V_{\text{OUT}} = 1.0\text{ V}$, $I_{\text{RESETB}} = 100\text{ }\mu\text{A}$ $I_{\text{RESETB}} = 1.0\text{ mA}$, $V_{\text{OUT}} = 4.5\text{ V}$	–	–	0.5	V
Pull-Up Resistor	RESETB = 1.0 V	25	50	100	k Ω
SWSD Input $V_{\text{BAT}} = 16\text{ V}$, $V_{\text{ER}} = 25\text{ V}$, $I_{\text{V(OUT)}} = -1.0\text{ mA}$					
High Threshold	–	–	–	$0.7 \times V_{\text{OUT}}$	V
Low Threshold	–	$0.3 \times V_{\text{OUT}}$	–	–	V
Input Impedance	Referenced to Ground	10	20	40	k Ω
NERD OUTPUT $V_{\text{BAT}} = 16\text{ V}$, $I_{\text{V(OUT)}} = -1.0\text{ mA}$, $C_{\text{NERD}} = 0.47\text{ }\mu\text{F}$					
VER Detection Voltage	–	1.5	–	6.5	V
Output Low Voltage	$I_{\text{NERD}} = 1.0\text{ mA}$, $V_{\text{OUT}} = 4.5\text{ V}$	–	–	0.5	V
Pull-Up Current	NERD = 0.5 V	30	40	50	μA
Power On Delay	–	6.25	8.5	11	ms
Clamping Voltage (Low)	VER Present	1.0	1.25	1.5	V
Clamping Voltage (High)	VER Not Present	3.5	3.75	4.0	V
General					
VER Load Current	$V_{\text{ER}} = 25\text{ V}$, $V_{\text{BAT}} = 16\text{ V}$, $I_{\text{V(OUT)}} = -100\text{ mA}$ $T = -40^{\circ}\text{C}$ $T = 25^{\circ}\text{C}$ $T = 125^{\circ}\text{C}$	– – –	– – –	5.0 5.0 4.0	mA mA mA
Thermal Shutdown	(Guaranteed by Design)	160	–	210	$^{\circ}\text{C}$

PACKAGE PIN DESCRIPTION

PACKAGE PIN #	PIN SYMBOL	FUNCTION
SO-20L		
1	VER	Energy reserve input.
2	V_{BAT}	Battery input.
3	V_{FB}	Charge PUMP control voltage input.
4	GND1	Ground.
5	GND2	Ground.
6	GND3	Ground.
7	GND4	Ground.
8	V_{SW}	Charge PUMP switch collector.
9	SWSD	Charge PUMP shutdown input.
10	COMP	Charge PUMP compensation pin.
11	C_{PUMP}	Charge PUMP timing cap input.
12	I_{BIAS}	Reference current resistor pin.

PACKAGE PIN DESCRIPTION (continued)

PACKAGE PIN #		
SO-20L	PIN SYMBOL	FUNCTION
13	V _{CHG}	Switched cap voltage tripler output.
14	GND5	Ground.
15	GND6	Ground.
16	GND7	Ground.
17	GND8	Ground.
18	NERD	No energy reserve detected output.
19	RESETB	Reset output.
20	V _{OUT}	Linear regulator output.

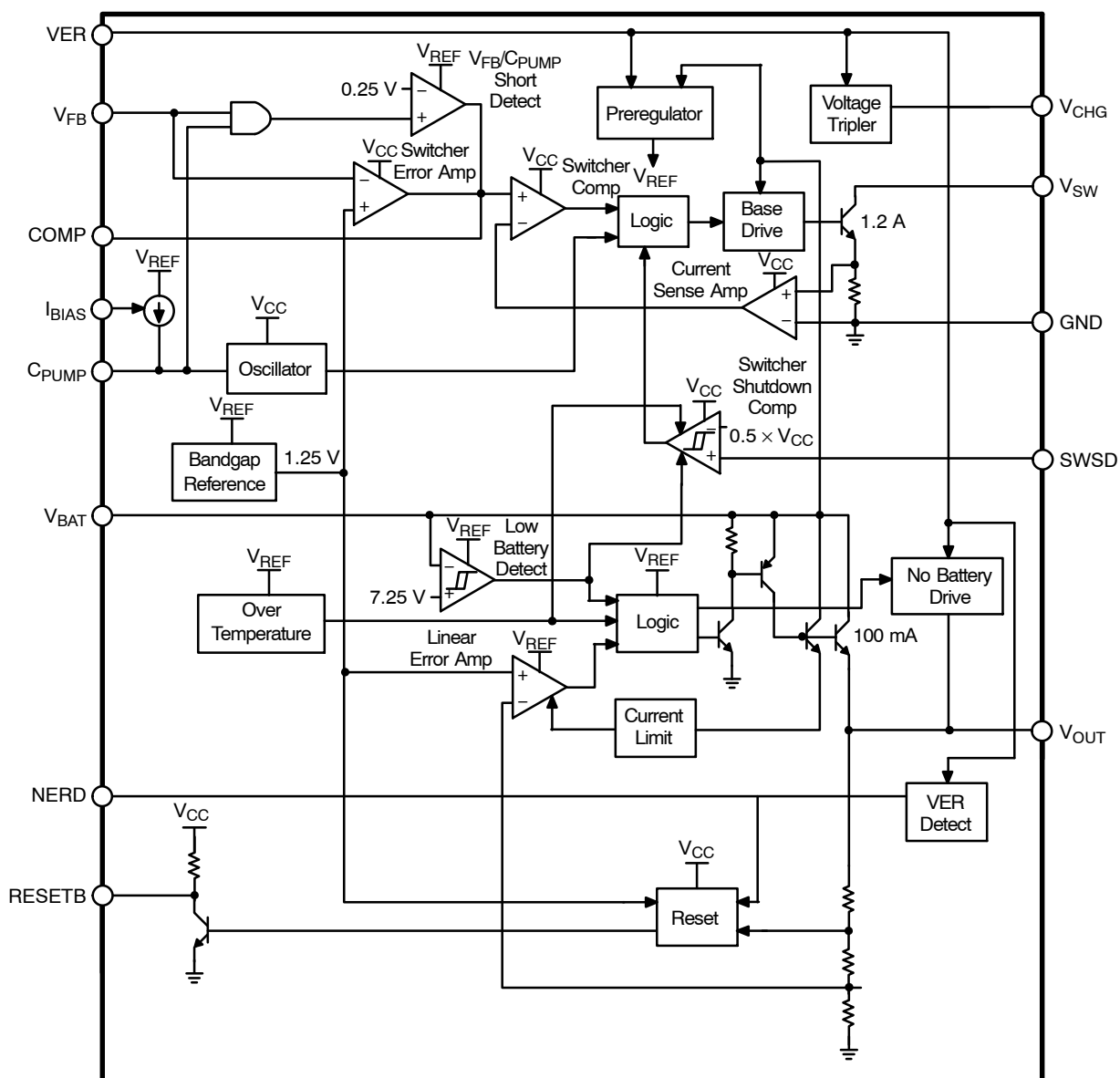


Figure 2. Block Diagram

CIRCUIT DESCRIPTION

Figure 3 is an oscilloscope waveform showing the charge pump collector voltage, collector current and the charge pump timing capacitor during normal operation with $I_{VER} = 30\text{mA}$.

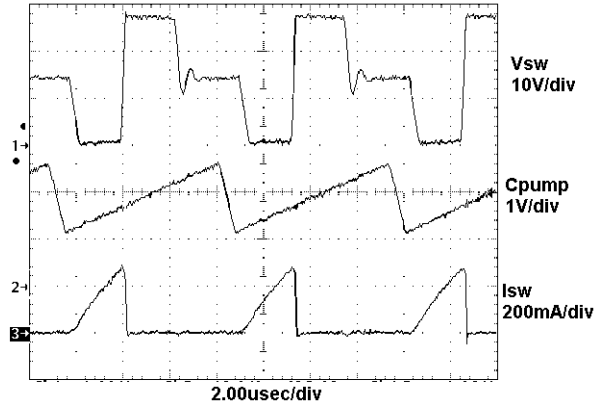


Figure 3. Typical Operation with $I_{VER} = 30\text{ mA}$

Figure 4 is an oscilloscope waveform showing the voltage tripler output and the energy reserve input during power up.

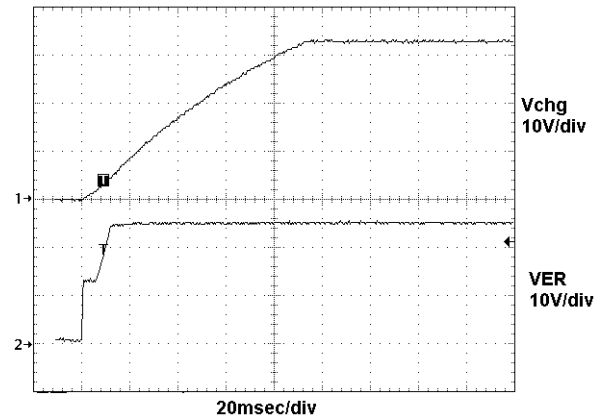
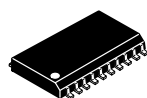


Figure 4. Startup with $R_{V(CHG)} = 510\text{ k}$

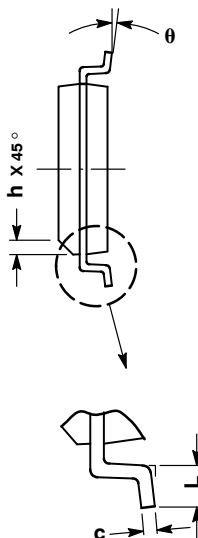
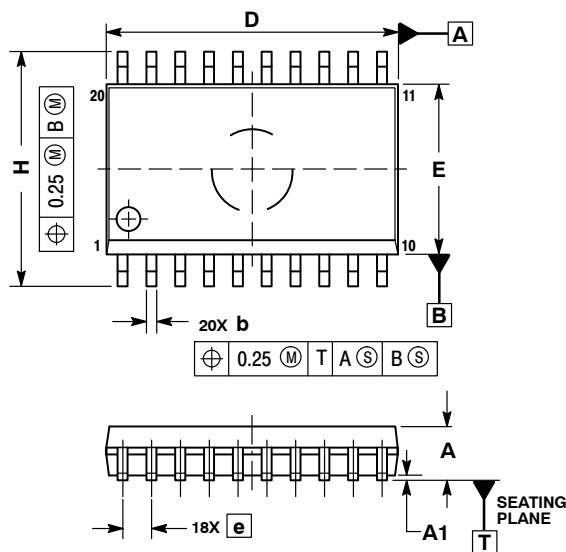
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015

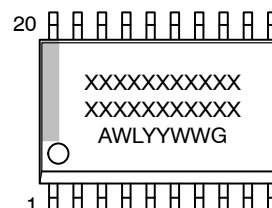


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

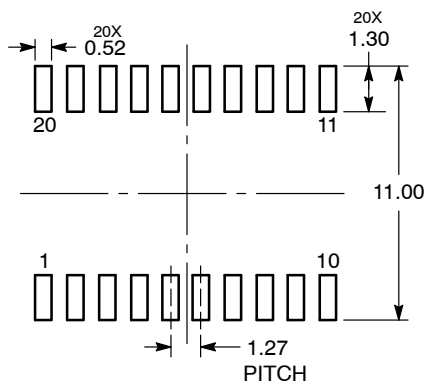
DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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