

# Single Channel Operational Amplifier

## LM321

LM321 is a general purpose, single channel op amp with internal compensation and a true differential input stage. This op amp features a wide supply voltage ranging from 3 V to 32 V for single supplies and  $\pm 1.5$  to  $\pm 16$  V for split supplies, suiting a variety of applications. LM321 is unity gain stable even with large capacitive loads up to 1.5 nF. LM321 is available in a space-saving TSOP-5/SOT23-5 package.

### Features

- Wide Supply Voltage Range: 3 V to 32 V
- Short Circuit Protected Outputs
- True Differential Input Stage
- Low Input Bias Currents
- Internally Compensated
- Single and Split Supply Operation
- Unity Gain Stable with 1.5 nF Capacitive Load
- This Device is Pb-Free, Halogen Free/BFR Free and is RoHS Compliant

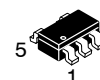
### Typical Applications

- Gain Stage
- Active Filter
- Signal Processing



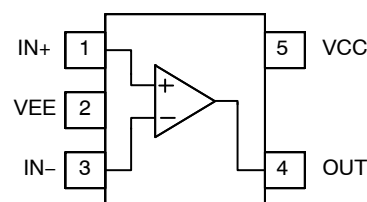
**ON Semiconductor®**

[www.onsemi.com](http://www.onsemi.com)

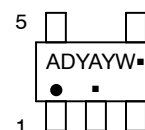


**TSOP-5  
CASE 483**

### PIN CONNECTION



### MARKING DIAGRAM



ADY = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

| Device      | Package             | Shipping <sup>†</sup> |
|-------------|---------------------|-----------------------|
| LM321SN3T1G | TSOP-5<br>(Pb-Free) | 3000 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# LM321

**Table 1. ABSOLUTE MAXIMUM RATINGS** (Over operating free-air temperature, unless otherwise stated)

| Parameter      | Rating | Unit |
|----------------|--------|------|
| Supply Voltage | 36     | V    |

## INPUT AND OUTPUT PINS

|                                        |                      |    |
|----------------------------------------|----------------------|----|
| Input Voltage                          | $V_{EE} - 0.3$ to 32 | V  |
| Input Current                          | $\pm 10$             | mA |
| Output Short Circuit Duration (Note 1) | Continuous           |    |

## TEMPERATURE

|                       |             |    |
|-----------------------|-------------|----|
| Operating Temperature | -40 to +125 | °C |
| Storage Temperature   | -65 to +150 | °C |
| Junction Temperature  | -65 to +150 | °C |

## ESD RATINGS (Note 2)

|                            |     |   |
|----------------------------|-----|---|
| Human Body Model (HBM)     | 200 | V |
| Charged Device Model (CDM) | 800 | V |
| Machine Model (MM)         | 100 | V |

## OTHER RATINGS

|                           |         |    |
|---------------------------|---------|----|
| Latch-Up Current (Note 3) | 100     | mA |
| MSL                       | Level 1 |    |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Short circuits can cause excessive heating and eventual destruction.
- This device series incorporates ESD protection and is tested by the following methods:  
ESD Human Body Model tested per JEDEC standard: JESD22-A114  
ESD Machine Model tested per JEDEC standard: JESD22-A115
- Latch-up Current tested per JEDEC standard: JESD78

**Table 2. THERMAL INFORMATION** (Note 4)

| Parameter           | Symbol        | Package        | Value | Unit |
|---------------------|---------------|----------------|-------|------|
| Junction to Ambient | $\theta_{JA}$ | TSOP-5/SOT23-5 | 235   | °C/W |

- As mounted on an 80 × 80 × 1.5 mm FR4 PCB with 650 mm<sup>2</sup> and 2 oz (0.034 mm) thick copper heat spreader. Following JEDEC JESD/EIA 51.1, 51.2, 51.3 test guidelines.

**Table 3. RECOMMENDED OPERATING CONDITIONS**

| Parameter                            | Symbol   | Range                      | Unit |
|--------------------------------------|----------|----------------------------|------|
| Supply Voltage ( $V_{CC} - V_{EE}$ ) | $V_S$    | 3 to 32                    | V    |
| Specified Operating Range            | $T_A$    | -40 to 85                  | °C   |
| Common Mode Input Voltage Range      | $V_{CM}$ | $V_{EE}$ to $V_{CC} - 1.7$ | V    |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# LM321

**Table 4. ELECTRICAL CHARACTERISTICS –  $V_S = 5\text{ V}$**

(At  $T_A = +25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to mid-supply,  $V_{CM} = V_{OUT} = \text{mid-supply}$ , unless otherwise noted.)

**Boldface** limits apply over the specified temperature range,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ , guaranteed by characterization and/or design.)

| Parameter                     | Symbol                   | Conditions                                                                                                                                       | Min                                                              | Typ                          | Max                            | Unit                         |
|-------------------------------|--------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------|------------------------------|--------------------------------|------------------------------|
| <b>INPUT CHARACTERISTICS</b>  |                          |                                                                                                                                                  |                                                                  |                              |                                |                              |
| Offset Voltage                | $V_{OS}$                 | $V_S = 5\text{ V}$ , $V_{CM} = V_{EE}$ to $V_{CC} - 1.7\text{ V}$<br>$T_A = 25^\circ\text{C}$<br>$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ | –<br>–                                                           | 0.3<br>–                     | 7<br><b>9</b>                  | mV                           |
| Offset Voltage Drift vs Temp  | $\Delta V_{OS}/\Delta T$ | $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$                                                                                                  | –                                                                | <b>7</b>                     | –                              | $\mu\text{V}/^\circ\text{C}$ |
| Input Bias Current            | $I_{IB}$                 | $T_A = 25^\circ\text{C}$<br>$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$                                                                      | –<br>–                                                           | –10<br>–                     | –<br><b>–500</b>               | nA                           |
| Input Offset Current          | $I_{OS}$                 | $T_A = 25^\circ\text{C}$<br>$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$                                                                      | –<br>–                                                           | 1<br>–                       | –<br><b>150</b>                | nA                           |
| Common Mode Rejection Ratio   | CMRR                     | $V_{CM} = V_{EE}$ to $V_{CC} - 1.7\text{ V}$                                                                                                     | 65                                                               | 85                           | –                              | dB                           |
| Input Resistance              | $R_{IN}$                 | Differential<br>Common Mode                                                                                                                      | –<br>–                                                           | 85<br>300                    | –<br>–                         | G $\Omega$                   |
| Input Capacitance             | $C_{IN}$                 | Differential<br>Common Mode                                                                                                                      | –<br>–                                                           | 0.6<br>1.6                   | –<br>–                         | pF                           |
| <b>OUTPUT CHARACTERISTICS</b> |                          |                                                                                                                                                  |                                                                  |                              |                                |                              |
| Open Loop Voltage Gain        | $A_{VOL}$                |                                                                                                                                                  | –                                                                | 100                          | –                              | dB                           |
| Open Loop Output Impedance    | $Z_{OUT\_OL}$            | $f = \text{UGBW}$ , $I_O = 0\text{ mA}$                                                                                                          | –                                                                | 1,200                        | –                              | $\Omega$                     |
| Output Voltage High           | $V_{OH}$                 | $R_L = 2\text{ k}\Omega$ to $V_{EE}$<br>$R_L = 10\text{ k}\Omega$ to $V_{EE}$                                                                    | <b><math>V_{CC}-1.8</math></b><br><b><math>V_{CC}-1.8</math></b> | $V_{CC}-1.4$<br>$V_{CC}-1.4$ | –<br>–                         | V                            |
| Output Voltage Low            | $V_{OL}$                 | $R_L = 10\text{ k}\Omega$ to $V_{CC}$                                                                                                            | –                                                                | $V_{EE}+0.8$                 | <b><math>V_{EE}+1.0</math></b> | V                            |
| Output Current Capability     | $I_O$                    | Sinking Current<br>$V_S = 5\text{ V}$<br>$V_S = 15\text{ V}$                                                                                     | <b>10</b><br><b>10</b>                                           | 20<br>20                     | –<br>–                         | mA                           |
| Output Current Capability     | $I_O$                    | Sourcing Current<br>$V_S = 5\text{ V}$<br>$V_S = 15\text{ V}$                                                                                    | <b>20</b><br><b>20</b>                                           | 40<br>40                     | –<br>–                         | mA                           |
| Capacitive Load Drive         | $C_L$                    | Phase Margin = $15^\circ$                                                                                                                        | –                                                                | 1,500                        | –                              | pF                           |
| <b>NOISE PERFORMANCE</b>      |                          |                                                                                                                                                  |                                                                  |                              |                                |                              |
| Voltage Noise Density         | $e_N$                    | $f_{IN} = 1\text{ kHz}$                                                                                                                          | –                                                                | 40                           | –                              | nV/ $\sqrt{\text{Hz}}$       |
| <b>DYNAMIC PERFORMANCE</b>    |                          |                                                                                                                                                  |                                                                  |                              |                                |                              |
| Gain Bandwidth Product        | GBWP                     | $C_L = 25\text{ pF}$ , $R_L$ to $V_{CC}$                                                                                                         | –                                                                | 750                          | –                              | kHz                          |
| Gain Margin                   | $A_M$                    | $C_L = 25\text{ pF}$ , $R_L$ to $V_{CC}$                                                                                                         | –                                                                | 14                           | –                              | dB                           |
| Phase Margin                  | $\alpha_M$               | $C_L = 25\text{ pF}$ , $R_L$ to $V_{CC}$                                                                                                         | –                                                                | 60                           | –                              | $^\circ$                     |
| Slew Rate                     | SR                       | $C_L = 25\text{ pF}$ , $R_L = \infty$                                                                                                            | –                                                                | 0.3                          | –                              | V/ $\mu\text{s}$             |
| <b>POWER SUPPLY</b>           |                          |                                                                                                                                                  |                                                                  |                              |                                |                              |
| Power Supply Rejection Ratio  | PSRR                     | $V_S = 5\text{ V}$ to $32\text{ V}$                                                                                                              | <b>62</b>                                                        | 100                          | –                              | dB                           |
| Quiescent Current             | $I_Q$                    | No Load                                                                                                                                          | –                                                                | 0.25                         | <b>0.5</b>                     | mA                           |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# LM321

**Table 5. ELECTRICAL CHARACTERISTICS –  $V_S = 32\text{ V}$**

(At  $T_A = +25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to mid-supply,  $V_{CM} = V_{OUT} = \text{mid-supply}$ , unless otherwise noted.)

**Boldface** limits apply over the specified temperature range,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ , guaranteed by characterization and/or design.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-----------|--------|------------|-----|-----|-----|------|
|-----------|--------|------------|-----|-----|-----|------|

## INPUT CHARACTERISTICS

|                              |                          |                                                                                                                                                   |        |          |                      |                              |
|------------------------------|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|--------|----------|----------------------|------------------------------|
| Offset Voltage               | $V_{OS}$                 | $V_S = 32\text{ V}$ , $V_{CM} = V_{EE}$ to $V_{CC} - 1.7\text{ V}$<br>$T_A = 25^\circ\text{C}$<br>$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ | –<br>– | 0.3<br>– | <b>7</b><br><b>9</b> | mV                           |
| Offset Voltage Drift vs Temp | $\Delta V_{OS}/\Delta T$ | $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$                                                                                                   | –      | <b>7</b> | –                    | $\mu\text{V}/^\circ\text{C}$ |
| Common Mode Rejection Ratio  | CMRR                     | $V_{CM} = V_{EE}$ to $V_{CC} - 1.7\text{ V}$                                                                                                      | –      | 100      | –                    | dB                           |

## OUTPUT CHARACTERISTICS

|                            |               |                                                                               |                                                                  |                              |                                |          |
|----------------------------|---------------|-------------------------------------------------------------------------------|------------------------------------------------------------------|------------------------------|--------------------------------|----------|
| Open Loop Voltage Gain     | $A_{VOL}$     | $T_A = 25^\circ\text{C}$<br>$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$   | –<br><b>84</b>                                                   | 100<br>–                     | –<br>–                         | dB       |
| Open Loop Output Impedance | $Z_{OUT\_OL}$ | $f = \text{UGBW}$ , $I_O = 0\text{ mA}$                                       | –                                                                | 2,000                        | –                              | $\Omega$ |
| Output Voltage High        | $V_{OH}$      | $R_L = 2\text{ k}\Omega$ to $V_{EE}$<br>$R_L = 10\text{ k}\Omega$ to $V_{EE}$ | <b><math>V_{CC}-2.5</math></b><br><b><math>V_{CC}-2.5</math></b> | $V_{CC}-2.0$<br>$V_{CC}-1.5$ | –<br>–                         | V        |
| Output Voltage Low         | $V_{OL}$      | $R_L = 10\text{ k}\Omega$ to $V_{CC}$                                         | –                                                                | $V_{EE}+1.0$                 | <b><math>V_{EE}+1.5</math></b> | V        |
| Capacitive Load Drive      | $C_L$         | Phase Margin = $15^\circ$                                                     | –                                                                | 1,500                        | –                              | pF       |

## NOISE PERFORMANCE

|                                   |       |                                                                   |   |      |   |                        |
|-----------------------------------|-------|-------------------------------------------------------------------|---|------|---|------------------------|
| Voltage Noise Density             | $e_N$ | $f_{IN} = 1\text{ kHz}$                                           | – | 40   | – | nV/ $\sqrt{\text{Hz}}$ |
| Total Harmonic Distortion + Noise | THD+N | $V_S = 30\text{ V}$ , $f_{IN} = 1\text{ kHz}$ , $R_L$ to $V_{CC}$ | – | 0.02 | – | %                      |

## DYNAMIC PERFORMANCE

|                        |            |                                          |   |     |   |                  |
|------------------------|------------|------------------------------------------|---|-----|---|------------------|
| Gain Bandwidth Product | GBWP       | $C_L = 25\text{ pF}$ , $R_L$ to $V_{CC}$ | – | 900 | – | kHz              |
| Gain Margin            | $A_M$      | $C_L = 25\text{ pF}$ , $R_L$ to $V_{CC}$ | – | 18  | – | dB               |
| Phase Margin           | $\alpha_M$ | $C_L = 25\text{ pF}$ , $R_L$ to $V_{CC}$ | – | 66  | – | $^\circ$         |
| Slew Rate              | SR         | $C_L = 25\text{ pF}$ , $R_L = \infty$    | – | 0.4 | – | V/ $\mu\text{s}$ |

## POWER SUPPLY

|                              |       |                                     |           |     |            |    |
|------------------------------|-------|-------------------------------------|-----------|-----|------------|----|
| Power Supply Rejection Ratio | PSRR  | $V_S = 5\text{ V}$ to $32\text{ V}$ | <b>62</b> | 100 | –          | dB |
| Quiescent Current            | $I_Q$ | No Load, $V_S = 32\text{ V}$        | –         | 0.3 | <b>1.2</b> | mA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## TYPICAL CHARACTERISTICS

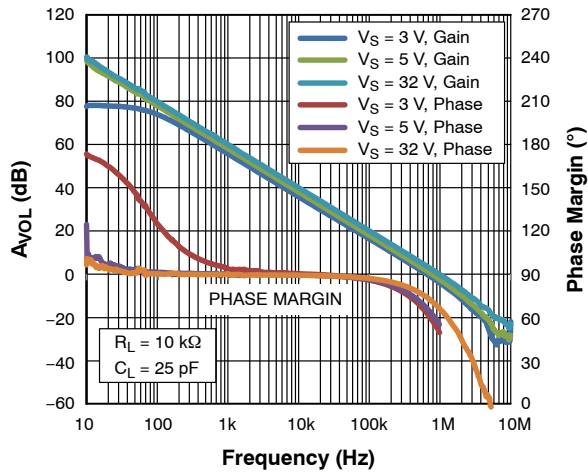


Figure 1. Open Loop Gain and Phase Margin vs. Frequency

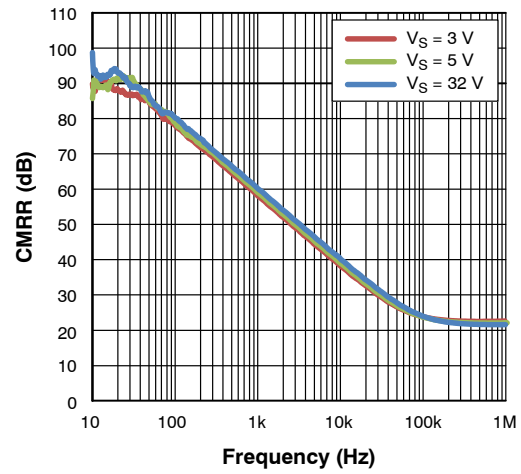


Figure 2. CMRR vs. Frequency

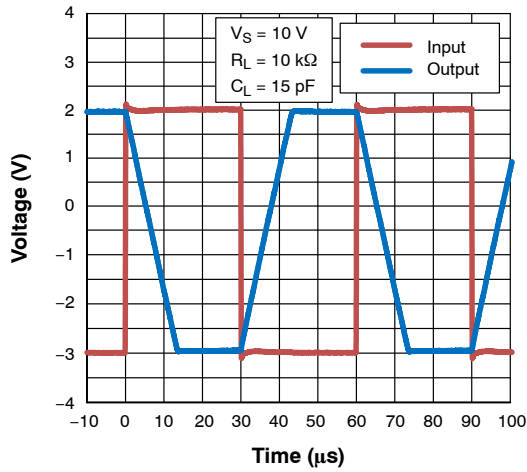


Figure 3. Inverting Large Signal Step Response

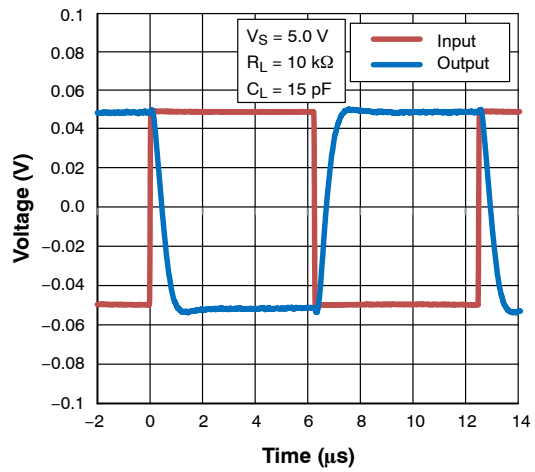


Figure 4. Inverting Small Signal Step Response

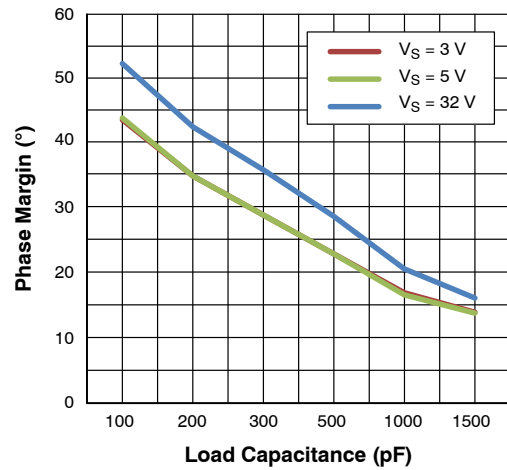


Figure 5. Phase Margin vs. Load Capacitance

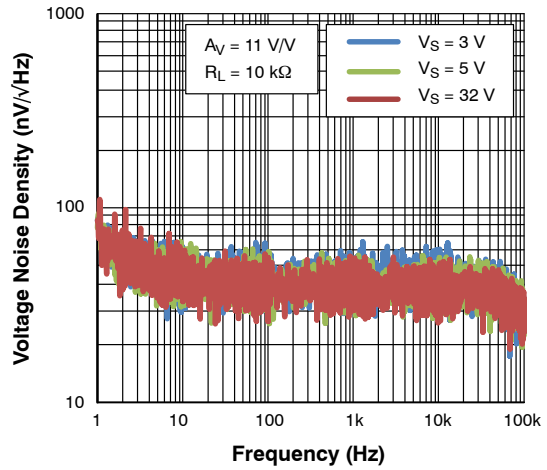


Figure 6. Voltage Noise Density vs. Frequency

## TYPICAL CHARACTERISTICS

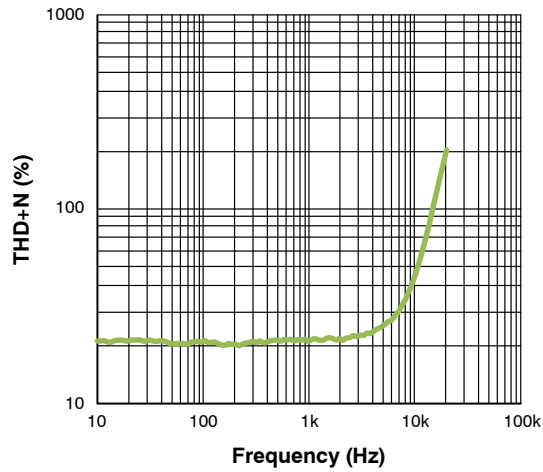


Figure 7. THD+N vs. Frequency

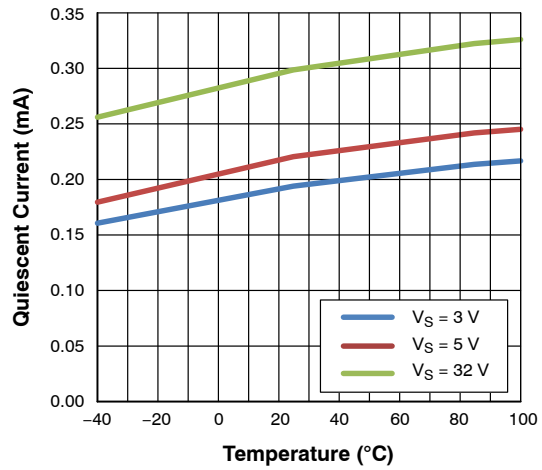


Figure 8. Quiescent Current vs. Temperature

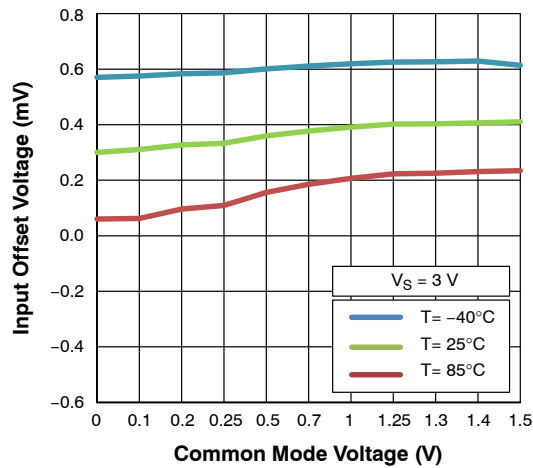


Figure 9. Input Offset Voltage vs. Common Mode Voltage at 3 V Supply

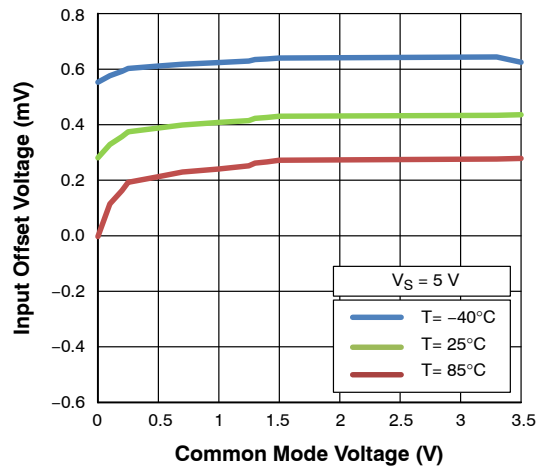


Figure 10. Input Offset Voltage vs. Common Mode Voltage at 5 V Supply

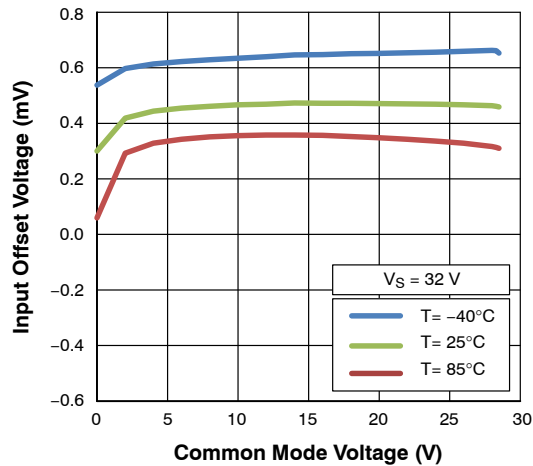


Figure 11. Input Offset Voltage vs. Common Mode Voltage at 32 V Supply

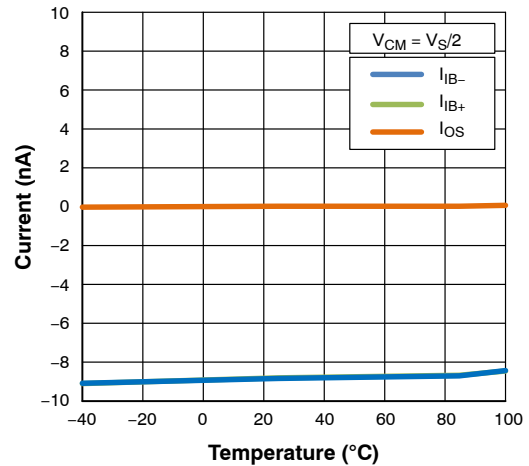


Figure 12. Input Bias and Offset Current vs. Temperature

## TYPICAL CHARACTERISTICS

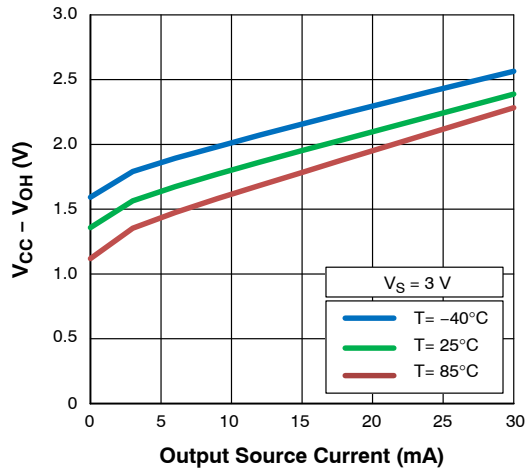


Figure 13. High Level Output Voltage Swing vs. Output Current at 3 V Supply

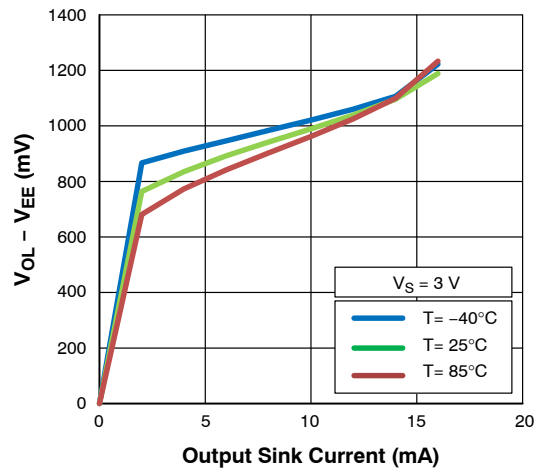


Figure 14. Low Level Output Voltage Swing vs. Output Current at 3 V Supply

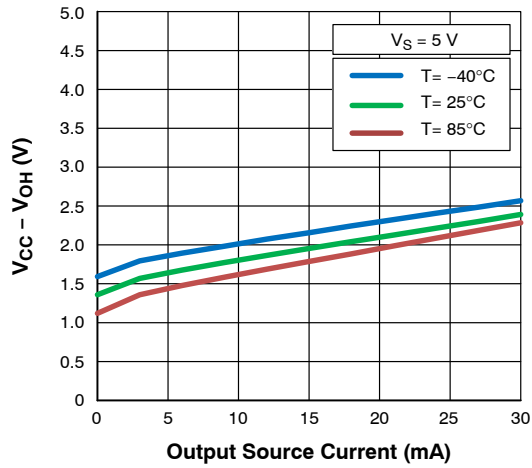


Figure 15. High Level Output Voltage Swing vs. Output Current at 5 V Supply

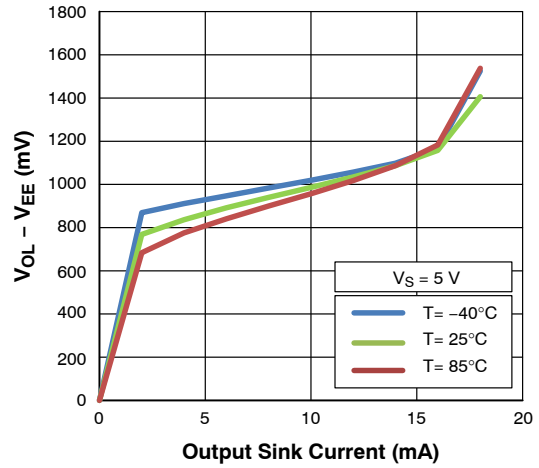


Figure 16. Low Level Output Voltage Swing vs. Output Current at 5 V Supply

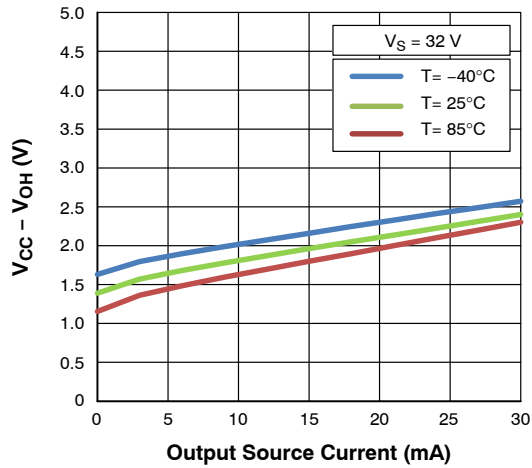


Figure 17. High Level Output Voltage Swing vs. Output Current at 32 V Supply

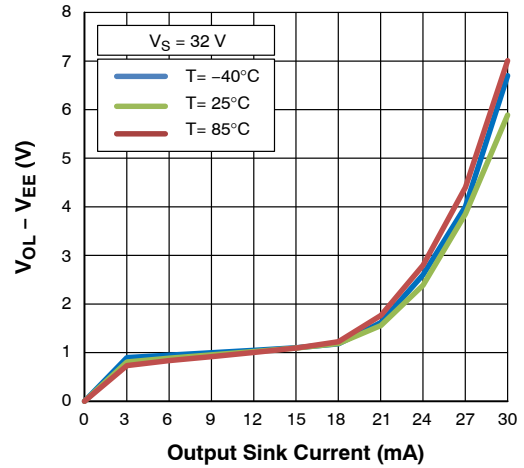


Figure 18. Low Level Output Voltage Swing vs. Output Current at 32 V Supply

## APPLICATION INFORMATION

## CIRCUIT DESCRIPTION

The LM321 is made using two internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance, a smaller compensation capacitor (only 5.0 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by

splitting the collectors of Q20 and Q18. Another feature of this input stage is that the input common mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

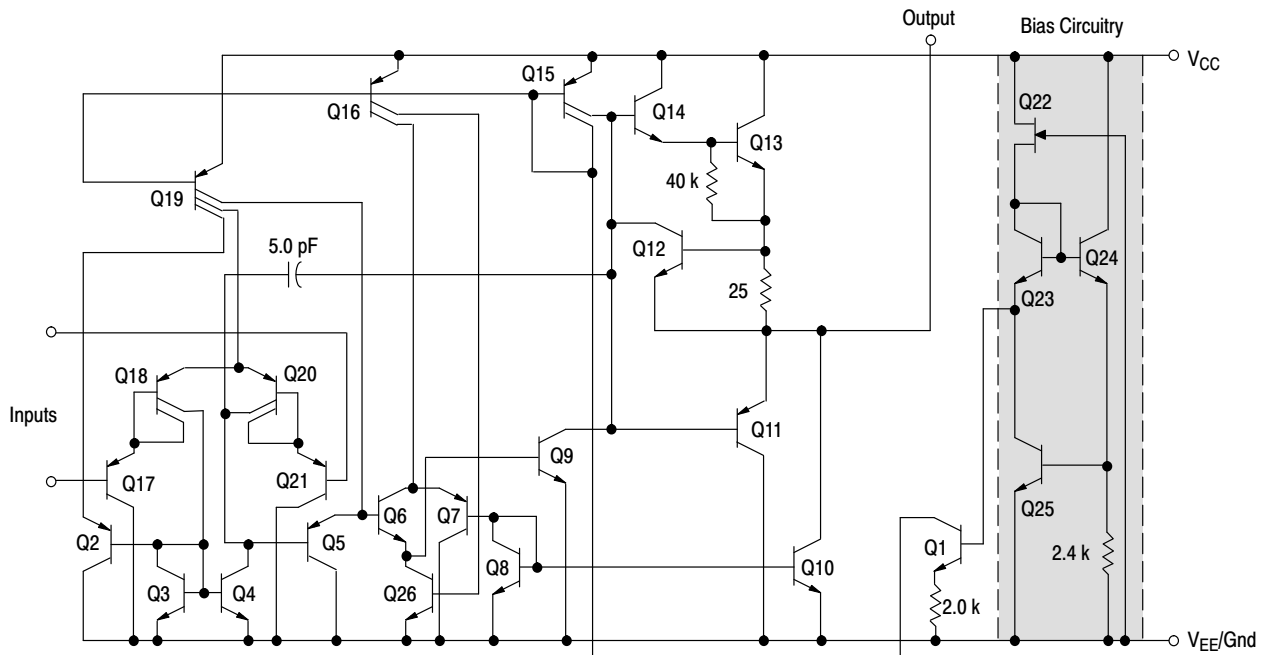


Figure 19. LM321 Representative Schematic Diagram



## LM321

LM321 has a class B output stage, which is comprised of push-pull transistors. This type of output is inherently subject to crossover distortion near mid-rail where neither push or pull transistors are conducting. Several techniques can be used to minimize crossover distortion. Connecting the output load to either the positive or negative supply rail instead of mid-rail can reduce the crossover distortion. Additionally, increasing the load resistance relatively decreases the amount of crossover distortion.

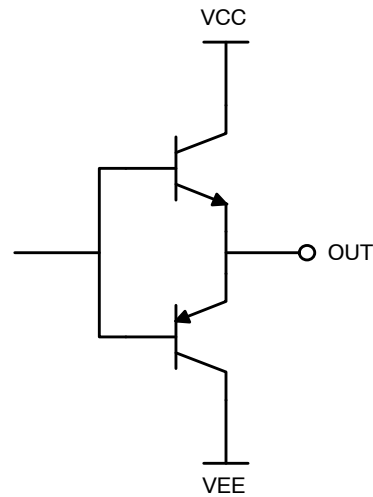


Figure 20. Simplified Class B Output

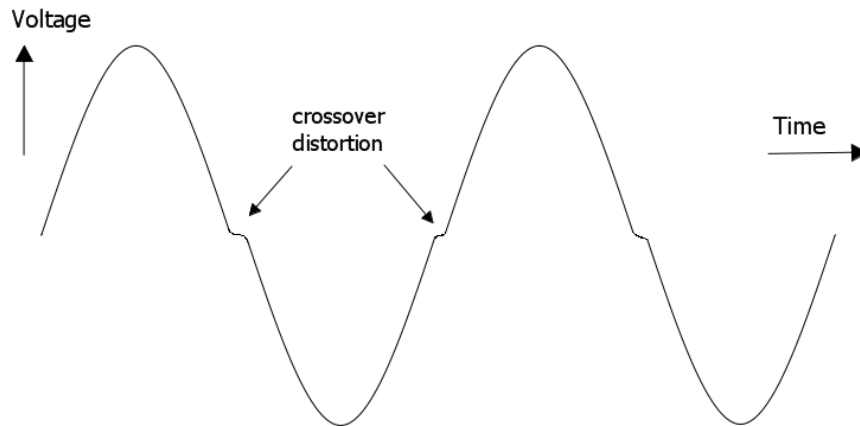
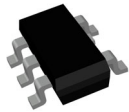


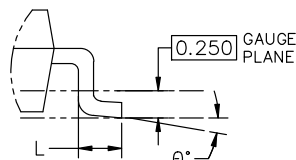
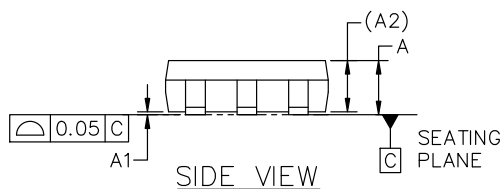
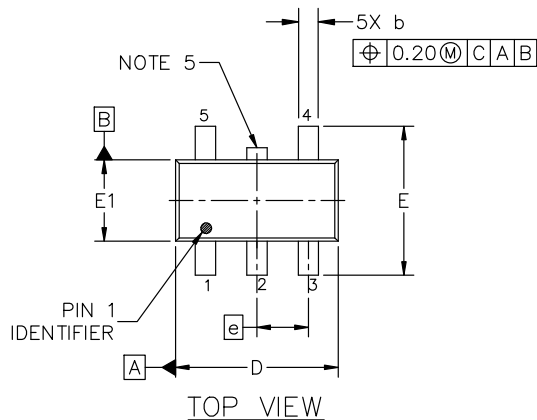
Figure 21. Sine wave with crossover distortion

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

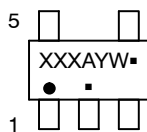


## TSOP-5 3.00x1.50x0.95, 0.95P CASE 483 ISSUE P

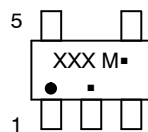
DATE 01 APR 2024



### GENERIC MARKING DIAGRAM\*



Analog



Discrete/Logic

XXX = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

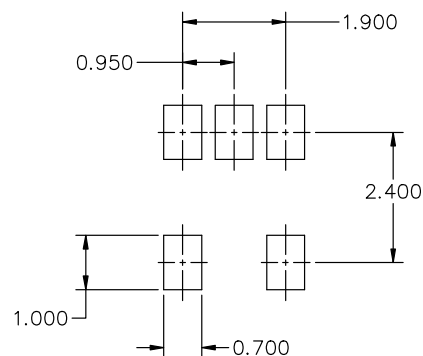
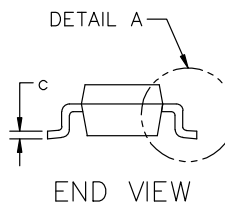
(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

### NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

| DIM | MILLIMETERS |       |       |
|-----|-------------|-------|-------|
|     | MIN.        | NOM.  | MAX.  |
| A   | 0.900       | 1.000 | 1.100 |
| A1  | 0.010       | 0.055 | 0.100 |
| A2  | 0.950 REF.  |       |       |
| b   | 0.250       | 0.375 | 0.500 |
| c   | 0.100       | 0.180 | 0.260 |
| D   | 2.850       | 3.000 | 3.150 |
| E   | 2.500       | 2.750 | 3.000 |
| E1  | 1.350       | 1.500 | 1.650 |
| e   | 0.950 BSC   |       |       |
| L   | 0.200       | 0.400 | 0.600 |
| θ   | 0°          | 5°    | 10°   |



### RECOMMENDED MOUNTING FOOTPRINT\*

\* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

|                  |                              |                                                                                                                                                                                  |
|------------------|------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DOCUMENT NUMBER: | 98ARB18753C                  | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION:     | TSOP-5 3.00x1.50x0.95, 0.95P | PAGE 1 OF 1                                                                                                                                                                      |

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at  
[www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)