Dual 4-Input Multiplexer with 3-State Outputs

MC74AC253, MC74ACT253

The MC74AC253/74ACT253 is a dual 4−input multiplexer with 3−state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus oriented systems.

- Multifunctional Capability
- Noninverting 3−State Outputs
- Outputs Source/Sink 24 mA
- 'ACT253 Has TTL Compatible Inputs
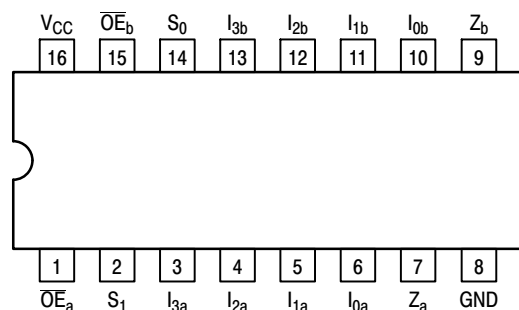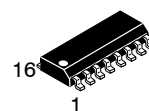- These are Pb−Free Devices

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

Figure 1. Pinout: 16−Lead Packages Conductors
(Top View)

Pin assignments:

Pin	Name
16	V_{CC}
15	$\overline{OE}_b$
14	S_0
13	I_{3b}
12	I_{2b}
11	I_{1b}
10	I_{0b}
9	Z_b
1	$\overline{OE}_a$
2	S_1
3	I_{3a}
4	I_{2a}
5	I_{1a}
6	I_{0a}
7	Z_a
8	GND

PIN NAME

PIN	FUNCTION
$I_{0a}-I_{3a}$	Side A Data Inputs
$I_{0b}-I_{3b}$	Side B Data Inputs
S_0, S_1	Common Select Inputs
$\overline{OE}_a$	Side A Output Enable Input
$\overline{OE}_b$	Side B Output Enable Input
Z_a, Z_b	3−State Outputs

MC74AC253, MC74ACT253

TRUTH TABLE

Select Inputs		Data Inputs				Output Enable	Outputs
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Z
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs S_0 and S_1 are common to both sections.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Figure 2. Logic Symbol

FUNCTIONAL DESCRIPTION

The MC74AC253/74ACT253 contains two identical 4−input multiplexers with 3−state outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4−input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. This device is the logic implementation of a 2−pole, 4−position switch, where the position 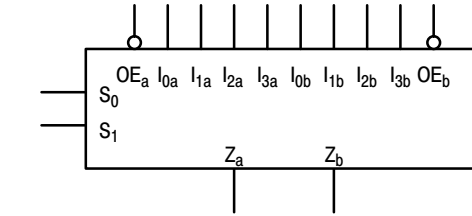of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown:

$$Z_a = \overline{OE}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$
$$Z_b = \overline{OE}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

If the outputs of 3−state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3−state devices whose outputs are tied together are designed so that there is no overlap.
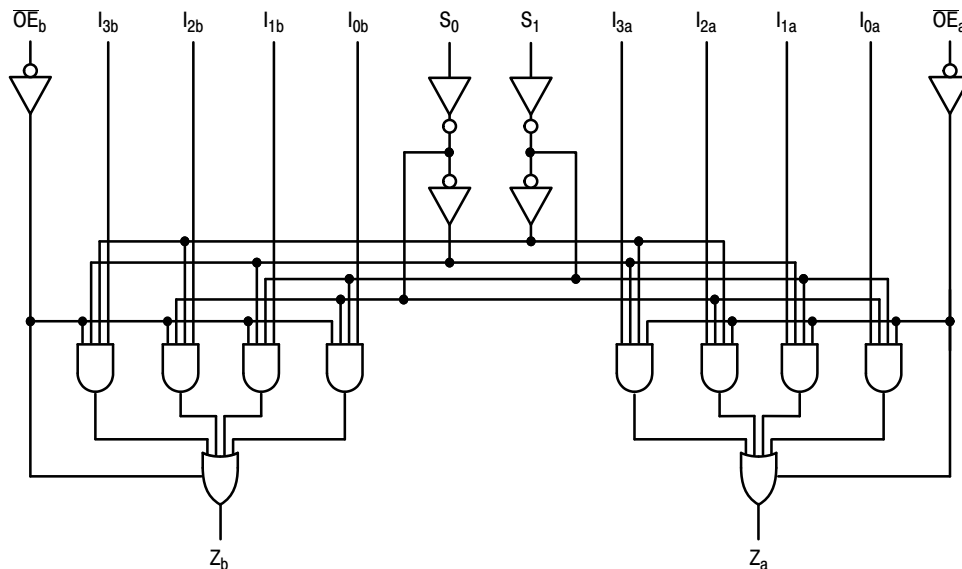
NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_I	DC Input Voltage		$-0.5 \le V_{CC} +0.5$	V
V_O	DC Output Voltage (Note 1)		$-0.5 \le V_{CC} +0.5$	V
I_{IK}	DC Input Diode Current		±20	mA
I_{OK}	DC Output Diode Current		±50	mA
I_O	DC Output Sink/Source Current		±50	mA
I_{CC}	DC Supply Current per Output Pin		±50	mA
I_{GND}	DC Ground Current per Output Pin		±50	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction temperature under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)	SOIC	126	°C/W
P_D	Power Dissipation in Still Air at 25°C (Note 3)	SOIC	995	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% – 35%	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 4) Charged Device Model (Note 5)	> 2000 > 1000	V
$I_{Latch-Up}$	Latch−Up Performance Above V_{CC} and Below GND at 85°C (Note 6)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. I_O absolute maximum rating must be observed.
2.   The package thermal impedance is calculated in accordance with JESD51−7.
3.   500 mW at 65°C; derate to 300 mW by 10 mW/ from 65°C to 85°C.
4.   Tested to EIA/JESD22−A114−A.
5.   Tested to JESD22−C101−A.
6.   Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	'AC	2.0	5.0	6.0	V
		'ACT	4.5	5.0	5.5	
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Ref. to GND)		0	–	V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V_{CC} @ 3.0 V	–	150	–	ns/V
		V_{CC} @ 4.5 V	–	40	–	
		V_{CC} @ 5.5 V	–	25	–	
t_r, t_f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V_{CC} @ 4.5 V	–	10	–	ns/V
		V_{CC} @ 5.5 V	–	8.0	–	
T_A	Operating Ambient Temperature Range		−40	25	85	°C
I_{OH}	Output Current – High		–	–	−24	mA
I_{OL}	Output Current – Low		–	–	24	mA

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
1. V_{IN} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{IN} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V$_{CC}$ (V)	74AC T$_A$ = +25°C Typ	74AC T$_A$ = +25°C Guaranteed Limits	74AC T$_A$ = −40°C to +85°C	Unit	Conditions
V$_{IH}$	Minimum High Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	2.1 3.15 3.85	2.1 3.15 3.85	V	V$_{OUT}$ = 0.1 V or V$_{CC}$ − 0.1 V
V$_{IL}$	Maximum Low Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	0.9 1.35 1.65	0.9 1.35 1.65	V	V$_{OUT}$ = 0.1 V or V$_{CC}$ − 0.1 V
V$_{OH}$	Minimum High Level Output Voltage	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	V	I$_{OUT}$ = −50 μA
		3.0 4.5 5.5	− − −	2.56 3.86 4.86	2.46 3.76 4.76	V	*V$_{IN}$ = V$_{IL}$ or V$_{IH}$ I$_{OH}$ −12 mA −24 mA −24 mA
V$_{OL}$	Maximum Low Level Output Voltage	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V	I$_{OUT}$ = 50 μA
		3.0 4.5 5.5	− − −	0.36 0.36 0.36	0.44 0.44 0.44	V	*V$_{IN}$ = V$_{IL}$ or V$_{IH}$ I$_{OL}$ 12 mA 24 mA 24 mA
I$_{IN}$	Maximum Input Leakage Current	5.5	−	±0.1	±1.0	μA	V$_I$ = V$_{CC}$, GND
I$_{OZ}$	Maximum 3−State Current	5.5	−	±0.5	±5.0	μA	V$_I$ (OE) = V$_{IL}$, V$_{IH}$ V$_I$ = V$_{CC}$, GND V$_O$ = V$_{CC}$, GND
I$_{OLD}$	†Minimum Dynamic Output Current	5.5	−	−	75	mA	V$_{OLD}$ = 1.65 V Max
I$_{OHD}$		5.5	−	−	−75	mA	V$_{OHD}$ = 3.85 V Min
I$_{CC}$	Maximum Quiescent Supply Current	5.5	−	8.0	80	μA	V$_{IN}$ = V$_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I$_{IN}$ and I$_{CC}$ @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V$_{CC}$.

AC CHARACTERISTICS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C C_L = 50 pF			74AC T_A = −40°C to +85°C C_L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay S_n to Z_n	3.3 5.0	2.0 2.0	– –	15.5 11.0	2.0 1.5	17.5 12.5	ns
t_{PHL}	Propagation Delay S_n to Z_n	3.3 5.0	2.5 2.0	– –	16.0 11.5	2.0 1.5	18.0 13.0	ns
t_{PLH}	Propagation Delay I_n to Z_n	3.3 5.0	1.5 1.5	– –	14.5 10.0	1.5 1.5	17.0 11.5	ns
t_{PHL}	Propagation Delay I_n to Z_n	3.3 5.0	2.0 1.5	– –	13.0 9.5	1.5 1.5	15.0 11.0	ns
t_{PZH}	Output Enable Time	3.3 5.0	1.5 1.5	– –	8.0 6.0	1.0 1.0	8.5 6.5	ns
t_{PZL}	Output Enable Time	3.3 5.0	1.5 1.5	– –	8.0 6.0	1.0 1.0	9.0 7.0	ns
t_{PHZ}	Output Disable Time	3.3 5.0	2.0 2.0	– –	9.5 8.0	1.5 1.5	10.0 8.5	ns
t_{PLZ}	Output Disable Time	3.3 5.0	1.5 1.5	– –	8.0 7.0	1.0 1.0	9.0 7.5	ns

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

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DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C	74ACT T_A = −40°C to +85°C	Unit	Conditions
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	4.5 / 5.5	1.5 / 1.5	2.0 / 2.0	2.0 / 2.0	V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
V_{IL}	Maximum Low Level Input Voltage	4.5 / 5.5	1.5 / 1.5	0.8 / 0.8	0.8 / 0.8	V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
V_{OH}	Minimum High Level Output Voltage	4.5 / 5.5	4.49 / 5.49	4.4 / 5.4	4.4 / 5.4	V	I_{OUT} = −50 μA
		4.5 / 5.5	− / −	3.86 / 4.86	3.76 / 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA / −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 / 5.5	0.001 / 0.001	0.1 / 0.1	0.1 / 0.1	V	I_{OUT} = 50 μA
		4.5 / 5.5	− / −	0.36 / 0.36	0.44 / 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA / 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	−	±0.1	±1.0	μA	V_I = V_{CC}, GND
ΔI_{CCT}	Additional Max. I_{CC}/Input	5.5	0.6	−	1.5	mA	V_I = V_{CC} − 2.1 V
I_{OZ}	Maximum 3−State Current	5.5	−	±0.5	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5	−	−	75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5	−	−	−75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	−	8.0	80	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C C_L = 50 pF			74ACT T_A = −40°C to +85°C C_L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay S_n to Z_n	5.0	2.0	–	11.5	2.0	13.0	ns
t_{PHL}	Propagation Delay S_n to Z_n	5.0	3.0	–	13.0	2.5	14.5	ns
t_{PLH}	Propagation Delay I_n to Z_n	5.0	2.5	–	10.0	2.0	11.0	ns
t_{PHL}	Propagation Delay I_n to Z_n	5.0	3.5	–	11.0	3.0	12.5	ns
t_{PZH}	Output Enable Time	5.0	2.0	–	7.5	1.5	8.5	ns
t_{PZL}	Output Enable Time	5.0	2.0	–	8.0	1.5	9.0	ns
t_{PHZ}	Output Disable Time	5.0	3.0	–	9.5	2.5	10.0	ns
t_{PLZ}	Output Disable Time	5.0	2.5	–	7.5	2.0	8.5	ns

* Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	50	pF	V_{CC} = 5.0 V

ORDERING INFORMATION

Device Order Number	Marking	Package	Shipping[†]
MC74AC253DR2G	AC253	SOIC−16 (Pb−Free)	2500 Tape & Reel
MC74ACT253DR2G	ACT253	SOIC−16 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
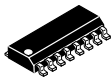
SOIC−16
CASE 751B−05
ISSUE K

SCALE 1:1

DATE 29 DEC 2006
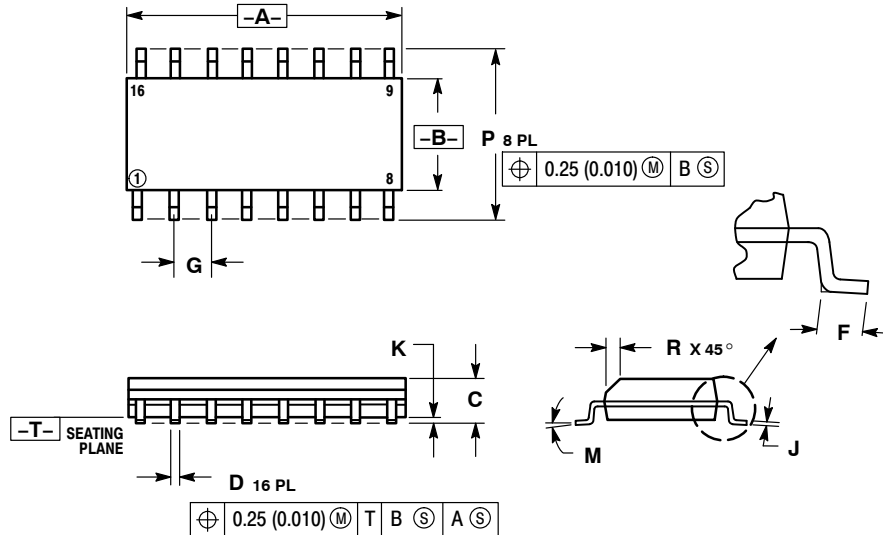
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N−CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P−CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P−CH
9. SOURCE P−CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N−CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N−CH

RECOMMENDED SOLDERING FOOTPRINT*
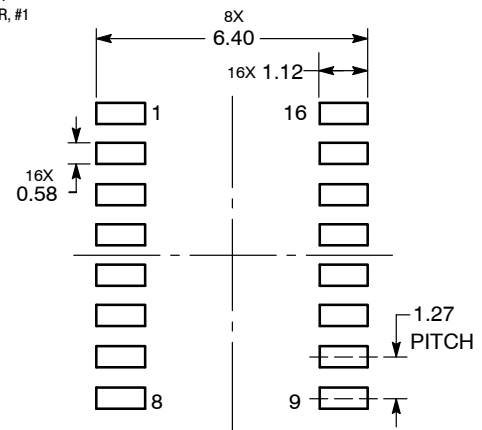
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	SOIC−16		PAGE 1 OF 1

ADDITIONAL INFORMATION

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