NCP5366

Integrated Driver and MOSFET

The NCP5366 integrates a MOSFET driver, high-side MOSFET and low-side MOSFET into a 6mm x 6mm 40-pin QFN package. The driver and MOSFETs have been optimized for high-current DC-DC buck power conversion applications. The NCP5366 integrated solution greatly reduces package parasitics and board space compared to a discrete component solution.

Features

- Capable of Switching Frequencies up to 1 MHz
- Capable of Output Currents up to 40 A
- Integrated Bootstrap Diode
- Output Disable Control turns off both MOSFETs
- Anti Cross-Conduction Protection Circuitry
- Undervoltage Lockout
- Internal Thermal Shutdown for System Protection
- These are Pb-free Devices

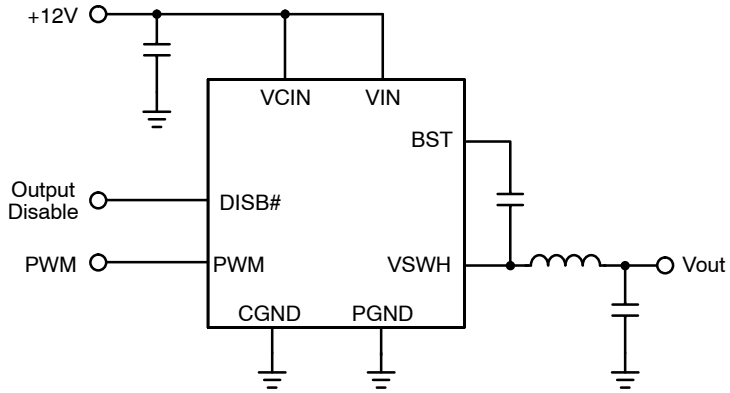

Figure 1. Application Schematic

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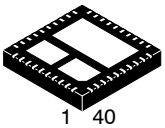
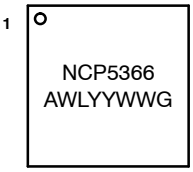


QFN40
MN SUFFIX
CASE 485AZ

MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCP5366MNR2G	QFN40 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

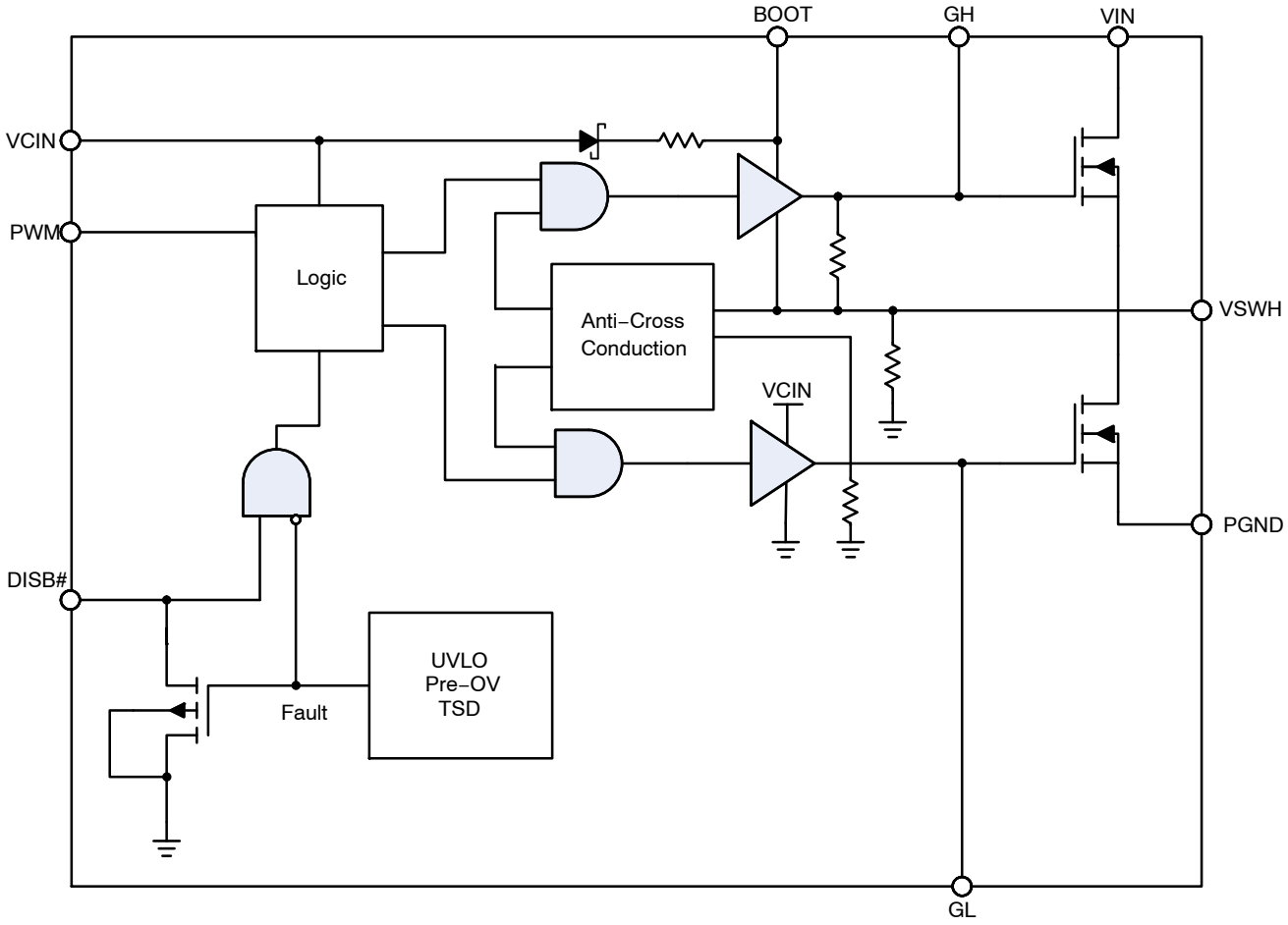


Figure 2. Simplified Block Diagram

PIN CONNECTIONS

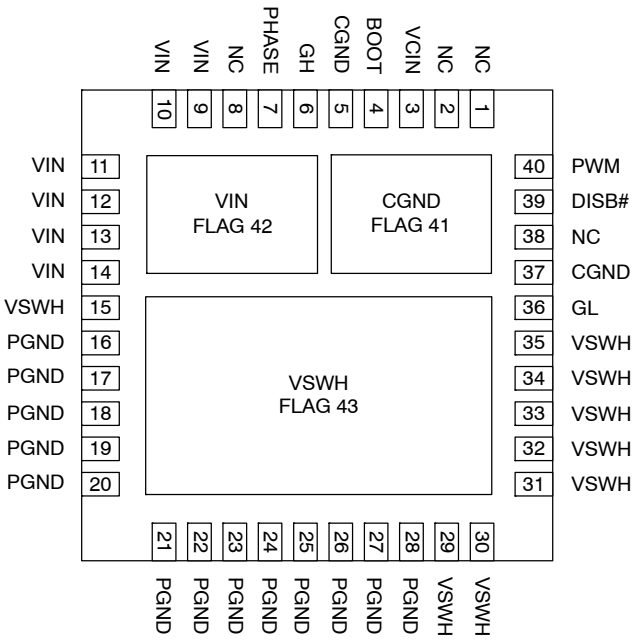


Figure 3. Pin Connections

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1, 2, 8, 38	NC	No Connect
3	VCIN	Control Input Voltage
4	BOOT	Bootstrap Voltage Pin
5, 37, Flag 41	CGND	Control Signal Ground
6	GH	High Side FET Gate Access Pin
7	PHASE	Provides a return path for the high side driver of the internal IC. Place a high frequency ceramic capacitor of 0.1 μF from this pin to BOOT pin.
9−14, Flag 42	VIN	Input Voltage
15, 29−35, Flag 43	VSWH	Switch Node Output
16−28	PGND	Power Ground
36	GL	Low Side FET Gate Access Pin
39	DISB#	Output Disable Pin
40	PWM	PWM Drive Logic

Table 2. ABSOLUTE MAXIMUM RATINGS

Pin Symbol	Pin Name	Min	Max
VCIN	Control Input Voltage	−0.3 V	15 V
VIN	Power Input Voltage	−0.3 V	30 V
BOOT	Bootstrap Voltage	−0.3 V wrt/VSWH	35 V wrt/PGND 40 V < 50 ns wrt/PGND 15 V wrt/VSWH
VSWH	Switch Node Output	−5 V −10 V < 200 ns	30 V
PWM	PWM Drive Logic	−0.3 V	6.5 V
DISB#	Output Disable	−0.3 V	6.5 V
PGND	Ground	0 V	0 V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance, High−Side FET	$R_{\theta JPCB}$	13	°C/W
Thermal Resistance, Low−Side FET	$R_{\theta JPCB}$	5.0	°C/W
Operating Junction Temperature	T_J	0 to 150	°C
Storage Temperature	T_S	−55 to 150	°C
Moisture Sensitivity Level	MSL	3	

1. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.

Table 4. OPERATING RANGES (Note 2)

Rating	Symbol	Min	Typ	Max	Unit
Control Input Voltage	VCIN	4.5	12	13.2	V
Input Voltage	VIN	4.5	12	25	V

2. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.

ELECTRICAL CHARACTERISTICS (Notes 3, 4) (VCIN = 12 V, VIN = 12 V, T_A = −10°C to +100°C, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
SUPPLY CURRENT						
VCIN Current (Normal Mode)	–	DISB# = 5 V, PWM = OSC, Fsw = 400 kHz			50	mA
VCIN Current (Shutdown Mode)	–	DISB# = GND		0.5	1.7	mA
UNDERVOLTAGE LOCKOUT						
UVLO Startup	–		3.8	4.35	4.5	V
UVLO Hysteresis	–		150	200	250	mV
BOOTSTRAP DIODE						
Bootstrap Diode Forward Voltage	–	VCIN = 12 V, Forward Bias Current = 2 mA	0.1	0.4	0.6	V
PWM INPUT						
PWM Input Voltage High	V_{PWM_HI}		3.3			V
PWM Input Voltage Mid−State	V_{PWM_MID}		1.3		2.7	V
PWM Input Voltage Low	V_{PWM_LO}				0.7	V
Tri−State Shutdown Holdoff Time	–			200		ns
OUTPUT DISABLE						
Output Disable Input Voltage High	V_{DISB_HI}		2.0			V
Output Disable Input Voltage Low	V_{DISB_LO}				1.0	V
Output Disable Hysteresis	–			500		mV
Output Disable Propagation Delay				20	40	ns

3. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
4. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

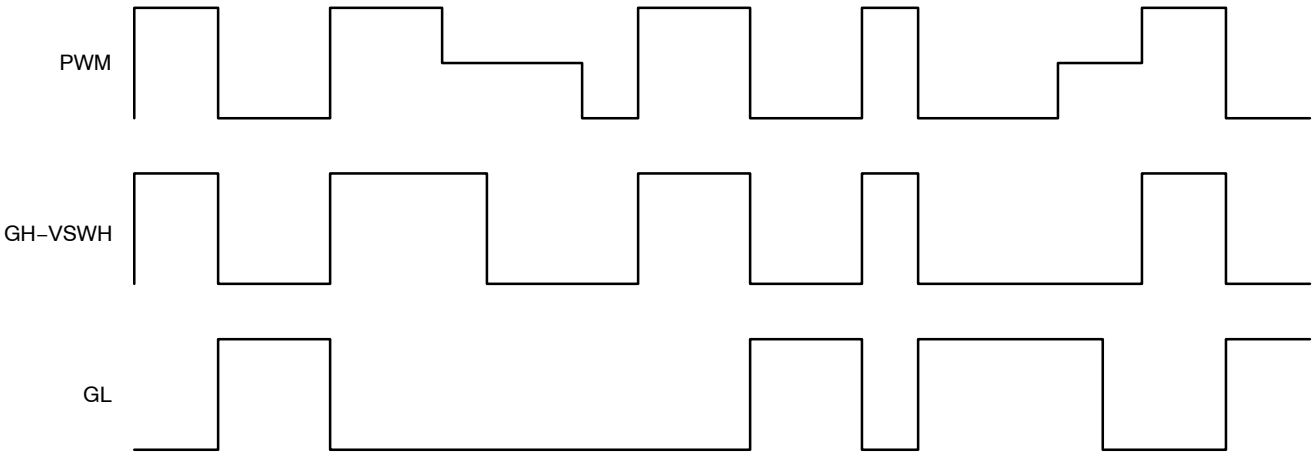


Figure 4. Timing Diagram

APPLICATION INFORMATION

Theory of Operation

The NCP5366 is an integrated driver and MOSFET module designed for use in a synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high−side and low−side MOSFETs.

Undervoltage Lockout

GH and GL are held low until VCIN reaches 4.5 V during startup. The PWM signals will control the gate status when the VCIN threshold is exceeded.

Power-On Reset

Power-On Reset feature is used to protect against an abnormal status during startup. When the initial soft-start voltage is greater than 2.75 V, the switch node pin is monitored. If VSWH is higher than 2.25 V, the low-side FET is turned on to discharge the output capacitors. The fault mode will latch and DISB# will be forced low until the part is recycled. When the input voltage is higher than 4.5 V and DISB# is high, the part will enter normal operation.

Bi-Directional DISB# Signal

Fault modes such as Power-On Reset, Overtemperature and Undervoltage Lockout will assert the DISB# pin. This will pull down the DRON of the controller as well, thus shutting the controller down.

Low−Side Driver

The low−side driver is designed to drive a ground referenced low $R_{DS(on)}$ N−Channel MOSFET. The voltage rail for the low−side driver is internally connected to VCIN and CGND.

High−Side Driver

The high−side driver is designed to drive a floating low $R_{DS(on)}$ N−channel MOSFET. The gate voltage for the high-side driver is developed by a bootstrap circuit referenced to Switch Node (VSWH) pin.

The bootstrap circuit is comprised of the internal bootstrap diode, and an external bootstrap capacitor. When the NCP5366 is starting up, the VSWH pin is at ground, so the bootstrap capacitor will charge up to VCIN through the bootstrap diode. When the PWM input goes high, the high−side driver will begin to turn on the high−side MOSFET using the stored charge of the bootstrap capacitor. As the high−side MOSFET turns on, the VSWH pin will rise. When the high−side MOSFET is fully on, the switch node will be at 12 V, and the BST pin will be at 12 V plus the charge of the bootstrap capacitor (approaching 24 V).

The bootstrap capacitor is recharged when the switch node goes low during the next cycle.

Safety Timer and Overlap Protection Circuit

It is very important that MOSFETs in a synchronous buck regulator do not both conduct at the same time. Excessive shoot−through or cross−conduction can damage the MOSFETs, and even a small amount of cross−conduction will cause a decrease in the power conversion efficiency.

The NCP5366 prevents cross conduction by monitoring the status of the MOSFETs and applying the appropriate amount of “dead−time” or the time between the turn off of one MOSFET and the turn on of the other MOSFET.

When the PWM input pin goes high, the gate of the low-side MOSFET (GL pin) will go low after a propagation delay (tpdlGL). The time it takes for the low−side MOSFET to turn off (tfGL) is dependent on the total charge on the low−side MOSFET gate. The NCP5366 monitors the gate voltage of both MOSFETs and the switchnode voltage to determine the conduction status of the MOSFETs. Once the low−side MOSFET is turned off an internal timer will delay (tpdhGH) the turn on of the high−side MOSFET.

Likewise, when the PWM input pin goes low, the gate of the high-side MOSFET (GH pin) will go low after the propagation delay (tpdlGH). The time to turn off the high−side MOSFET (tfGH) is dependent on the total gate charge of the high−side MOSFET. A timer will be triggered once the high−side MOSFET has stopped conducting, to delay (tpdhGL) the turn on of the low−side MOSFET.

When the PWM input is between V_{PWM_LO} and V_{PWM_HI} for longer than 200 ns, both the high-side and low-side MOSFETs will be turned off. The PWM input will need to exceed V_{PWM_HI} to resume normal switching of the MOSFETs.

Power Supply Decoupling

The NCP5366 can source and sink relatively large currents to the gate pins of the MOSFETs. In order to maintain a constant and stable supply voltage (VCIN) a low ESR capacitor should be placed near the power and ground pins. A 1 μF to 4.7 μF multi layer ceramic capacitor (MLCC) is usually sufficient.

Input Pins

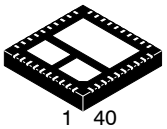
The PWM input and the Output Disable pins of the NCP5366 have internal protection for Electro Static Discharge (ESD), but in normal operation they present a relatively high input impedance. If the PWM controller does not have internal pull−down resistors, they should be added externally to ensure that the driver outputs do not go high before the controller has reached its undervoltage lockout threshold.

Bootstrap Circuit

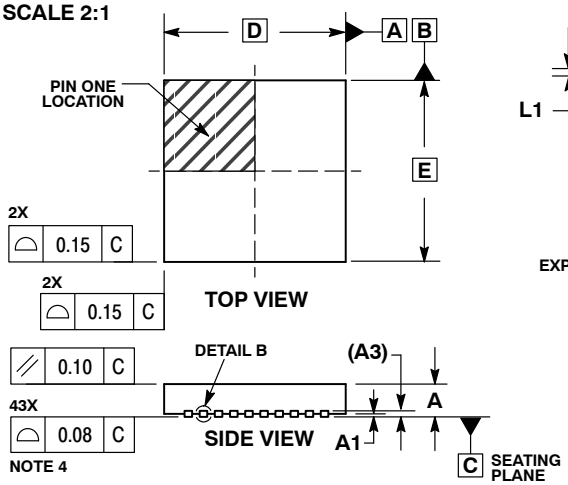
The bootstrap circuit uses a charge storage capacitor (C_{BST}) and the internal diode. The bootstrap capacitor must have a voltage rating that is able to withstand twice the maximum supply voltage. A minimum 50 V rating is recommended. A bootstrap capacitance greater than 100 nF is recommended. A good quality ceramic capacitor should be used.

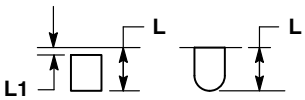
QFN40 6x6, 0.5P
CASE 485AZ
ISSUE O

DATE 09 JAN 2009

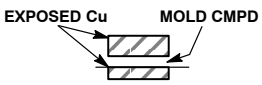


SCALE 2:1

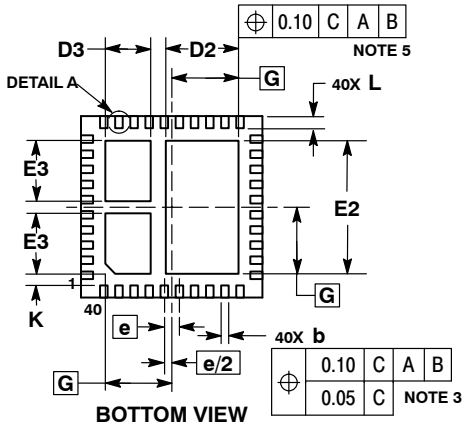




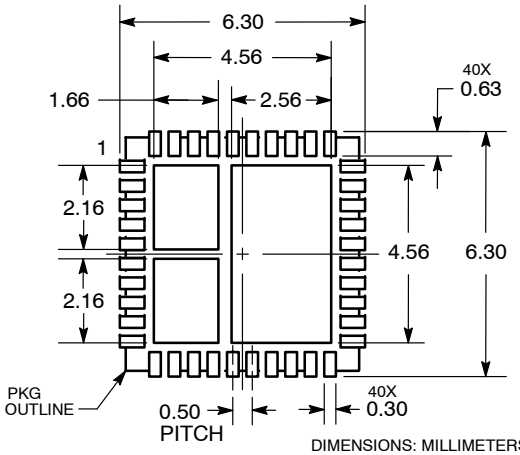
DETAIL A
ALTERNATE CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTION



SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO ALL THREE EXPOSED PADS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	6.00 BSC	
D2	2.30	2.50
D3	1.40	1.60
E	6.00 BSC	
E2	4.30	4.50
E3	1.90	2.10
e	0.50 BSC	
G	2.20 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15

GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**QFN40 6x6, 0.5P**	**PAGE 1 OF 1**

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