

NCV7329

Stand-alone LIN Transceiver

Description

The NCV7329 is a fully featured local interconnect network (LIN) transceiver designed to interface between a LIN protocol controller and the physical bus.

The LIN bus is designed to communicate low rate data from control devices such as door locks, mirrors, car seats, and sunroofs at the lowest possible cost. The bus is designed to eliminate as much wiring as possible and is implemented using a single wire in each node. Each node has a slave MCU–state machine that recognizes and translates the instructions specific to that function.

The main attraction of the LIN bus is that all the functions are not time critical and usually relate to passenger comfort.

Features

- LIN–Bus Transceiver
 - ◆ Compliant to ISO 17987–4 (Backwards Compatible to LIN Specification rev. 2.x, 1.3) and SAE J2602
 - ◆ Bus Voltage ± 42 V
 - ◆ Transmission Rate 1 kbps to 20 kbps
 - ◆ TxD Timeout Function
 - ◆ Integrated Slope Control
- Protection
 - ◆ Thermal Shutdown
 - ◆ Undervoltage Protection
 - ◆ Bus Pins Protected Against Transients in an Automotive Environment
- Modes
 - ◆ Normal Mode: LIN Transceiver Enabled, Communication via the Bus is Possible
 - ◆ Sleep Mode: LIN Transceiver Disabled, the Consumption from V_{BB} is Minimized
 - ◆ Standby Mode: Transition Mode Reached after Wake–up Event on the LIN Bus
- Compatibility
 - ◆ Pin–Compatible Subset with NCV7321
 - ◆ K–line Compatible

Quality

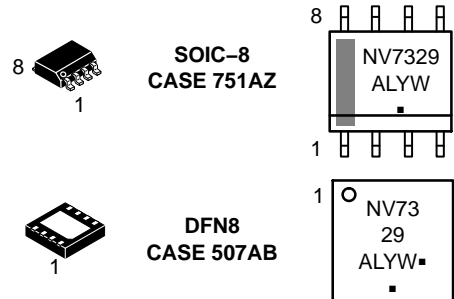
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant



ON Semiconductor®

www.onsemi.com

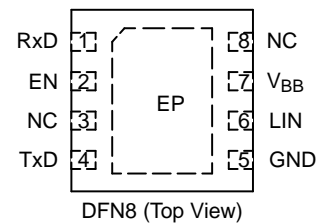
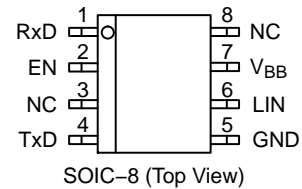
MARKING DIAGRAMS



A = Assembly Location
 L = Wafer Lot
 Y = Year
 W = Work Week
 ■ = Pb–Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

NCV7329

BLOCK DIAGRAM

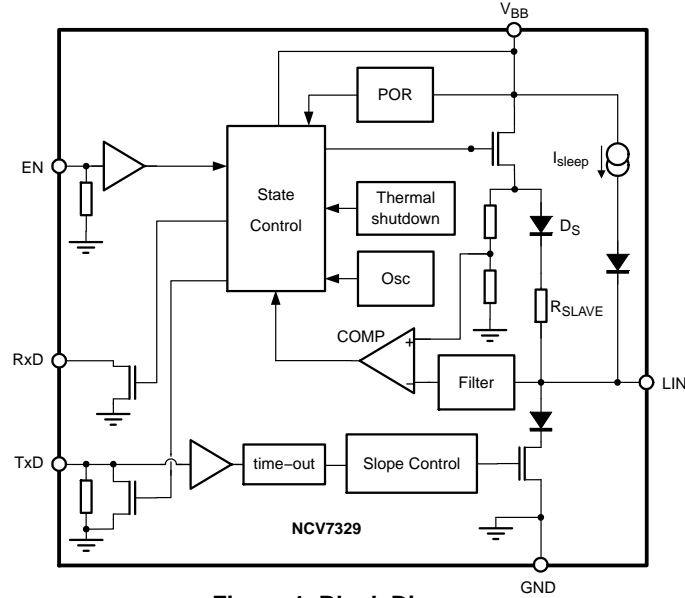


Figure 1. Block Diagram

TYPICAL APPLICATION

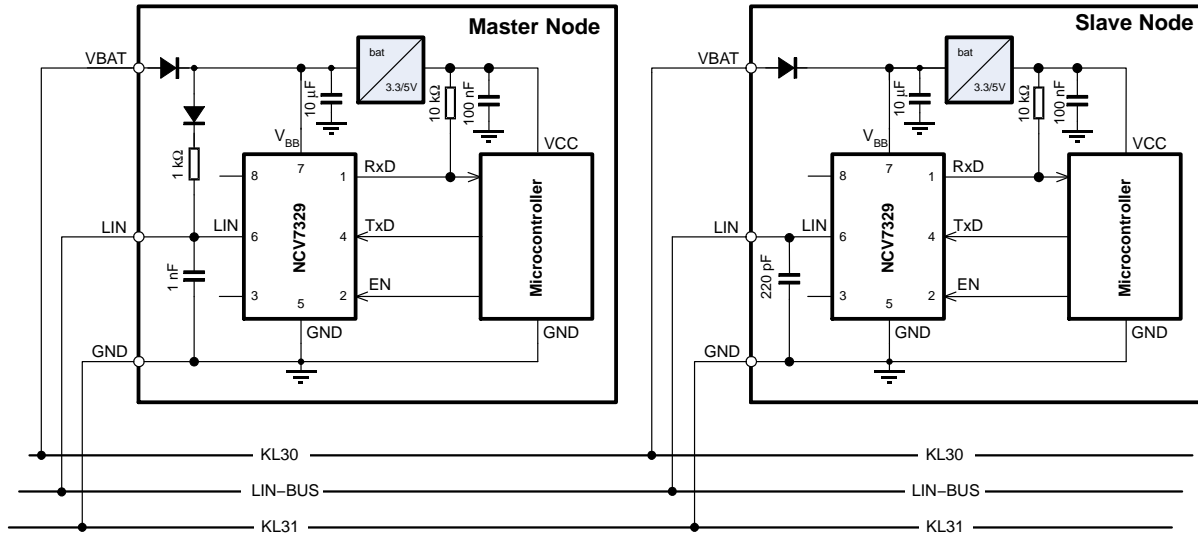


Figure 2. Typical Application Diagram for a Master Node

Table 1. PIN DESCRIPTION

| Pin | Name | Description |
|-----|-----------------|---|
| 1 | RxD | Receive Data Output; Low in Dominant State; Open-Drain Output |
| 2 | EN | Enable Input, Transceiver in Normal Operation Mode when High, Pull-down Resistor to GND |
| 3 | NC | Not Connected |
| 4 | TxD | Transmit Data Input, Low for Dominant State, Pull-down to GND |
| 5 | GND | Ground |
| 6 | LIN | LIN Bus Output/Input |
| 7 | V _{BB} | Battery Supply Input |
| 8 | NC | Not Connected |
| - | EP | Exposed Pad. Recommended to connect to GND or left floating in application (DFN8 package only). |

Table 2. ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Min | Max | Unit |
|---------------------|---|------|------|------|
| V _{BB} | Voltage on Pin V _{BB} | -0.3 | +42 | V |
| V _{LIN} | LIN Bus Voltage with respect to GND | -42 | +42 | V |
| | LIN Bus Voltage with respect to V _{BB} | -42 | +42 | V |
| V _{Dig_IO} | DC Input Voltage on Pins (EN, RxD, TxD) | -0.3 | +7 | V |
| V _{ESD} | Human Body Model (LIN Pin) (Note 1) | -8 | +8 | kV |
| | Human Body Model (All Pins) (Note 1) | -4 | +4 | kV |
| | Charged Device Model (All Pins) (Note 2) | -750 | +750 | V |
| | Machine Model (All Pins) (Note 3) | -200 | +200 | V |
| V _{ESDIEC} | Electrostatic Discharge Voltage (LIN Pin) System Human Body Model (Note 4) Conform to IEC 61000-4-2 | -8 | +8 | kV |
| T _J | Junction Temperature Range | -40 | +150 | °C |
| T _{STG} | Storage Temperature Range | -55 | +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Standardized human body model electrostatic discharge (ESD) pulses in accordance to EIA-JESD22. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
2. Standardized charged device model ESD pulses when tested according to AEC-Q100-011.
3. In accordance to JEDEC JESD22-A115. Equivalent to discharging a 200 pF capacitor through a 10 Ω resistor and 0.75 μH coil.
4. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor. System HBM levels are verified by an external test-house.

Table 3. THERMAL CHARACTERISTICS

| Parameter | Symbol | Value | Unit |
|---|------------------|-------|------|
| Thermal characteristics, SOIC-8 (Note 5) | | | |
| Thermal Resistance Junction-to-Air, Free air, 1S0P PCB (Note 6) | R _{θJA} | 131 | °C/W |
| Thermal Resistance Junction-to-Air, Free air, 2S2P PCB (Note 7) | R _{θJA} | 81 | °C/W |
| Thermal characteristics, DFN8 (Note 5) | | | |
| Thermal Resistance Junction-to-Air, Free air, 1S0P PCB (Note 6) | R _{θJA} | 125 | °C/W |
| Thermal Resistance Junction-to-Air, Free air, 2S2P PCB (Note 7) | R _{θJA} | 58 | °C/W |

5. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
6. Values based on test board according to EIA/JEDEC Standard JESD51-3, signal layer with 10% trace coverage.
7. Values based on test board according to EIA/JEDEC Standard JESD51-7, signal layers with 10% trace coverage.

ELECTRICAL CHARACTERISTICS

Definitions

All voltages are referenced to GND (pin 5) unless otherwise specified. Positive currents flow into the IC. Sinking current means the current is flowing into the pin; sourcing current means the current is flowing out of the pin.

Table 4. DC CHARACTERISTICS ($V_{BB} = 5\text{ V to }18\text{ V}$; $T_J = -40^\circ\text{C to }+150^\circ\text{C}$; Typical values are given at $V_{BB} = 12\text{ V}$ and $T_J = 25^\circ\text{C}$ Bus Load = $500\ \Omega$ (V_{BB} to LIN); unless otherwise specified.)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--|--|--|-------|-------|-------|---------------|
| SUPPLY PIN (V_{BB}) | | | | | | |
| V_{BB} | Battery Supply | | 5 | | 18 | V |
| I_{BB} | Battery Supply Current | Normal Mode; LIN recessive | 0.2 | 0.55 | 1.2 | mA |
| I_{BB} | Battery Supply Current | Normal Mode; TxD = Low, LIN Dominant | 2 | 3.9 | 6.5 | mA |
| I_{BB} | Battery Supply Current | Sleep and Standby Mode; LIN recessive; $V_{LIN} = V_{BB}$; $T_J < 85^\circ\text{C}$ | | 6 | 10 | μA |
| I_{BB} | Battery Supply Current | Sleep and Standby Mode; LIN recessive; $V_{LIN} = V_{BB}$ | | 6 | 15 | μA |
| POR AND V_{BB} MONITOR | | | | | | |
| PORH_ V_{BB} | Power-on Reset; High Level on V_{BB} | V_{BB} Rising | 2.7 | 3.5 | 4.4 | V |
| PORL_ V_{BB} | Power-on Reset; Low Level on V_{BB} | V_{BB} Falling | 1.3 | 2.1 | 2.7 | V |
| MONH_ V_{BB} | Battery Monitoring High Level | V_{BB} Rising | 3.2 | 4.2 | 5.0 | V |
| MONL_ V_{BB} | Battery Monitoring Low Level | V_{BB} Falling | 3.0 | 4.0 | 4.8 | V |
| TRANSMITTER DATA INPUT (PIN TxD) | | | | | | |
| V_{IL_TxD} | Low Level Input Voltage | | -0.3 | | +0.8 | V |
| V_{IH_TxD} | High Level Input Voltage | | 2 | | 7 | V |
| R_{PD_TxD} | Pull-down Resistor on TxD Pin | | 50 | 125 | 325 | k Ω |
| RECEIVER DATA OUTPUT (PIN RxD) | | | | | | |
| I_{OL_RxD} | Low Level Output Current | $V_{RxD} = 0.4\text{ V}$ | 2 | | | mA |
| I_{OH_RxD} | High Level Output Current | | -5 | | +5 | μA |
| ENABLE INPUT (PIN EN) | | | | | | |
| V_{IL_EN} | Low Level Input Voltage | | -0.3 | | +0.8 | V |
| V_{IH_EN} | High Level Input Voltage | | 2 | | 7 | V |
| R_{PD_EN} | Pull-down Resistor to Ground | | 100 | 250 | 650 | k Ω |
| LIN BUS LINE (PIN LIN) | | | | | | |
| V_{BUS_DOM} | Bus Voltage for Dominant State | | | | 0.4 | V_{BB} |
| V_{BUS_REC} | Bus Voltage for Recessive State | | 0.6 | | | V_{BB} |
| V_{REC_DOM} | Receiver Threshold | LIN Bus Recessive – Dominant | 0.4 | | 0.6 | V_{BB} |
| V_{REC_REC} | Receiver Threshold | LIN Bus Dominant – Recessive | 0.4 | | 0.6 | V_{BB} |
| V_{REC_CNT} | Receiver Centre Voltage | $(V_{REC_DOM} + V_{REC_REC}) / 2$ | 0.475 | 0.500 | 0.525 | V_{BB} |
| V_{REC_HYS} | Receiver Hysteresis | $(V_{REC_REC} - V_{REC_DOM})$ | 0.050 | | 0.175 | V_{BB} |
| V_{LIN_DOM} | Dominant Output Voltage | Normal mode; $V_{BB} = 7\text{ V}$ | | | 1.2 | V |
| | | Normal mode; $V_{BB} = 18\text{ V}$ | | | 2.0 | V |
| $I_{BUS_no_GND}$ | Communication not Affected | $V_{BB} = \text{GND} = 12\text{ V}$; $0 < V_{LIN} < 18\text{ V}$ | -1 | | +1 | mA |
| $I_{BUS_no_VBB}$ | LIN Bus Remains Operational | $V_{BB} = \text{GND} = 0\text{ V}$; $0 < V_{LIN} < 18\text{ V}$ | | | 5 | μA |

8. Values based on design and characterization. Not tested in production.

NCV7329

Table 4. DC CHARACTERISTICS ($V_{BB} = 5\text{ V to }18\text{ V}$; $T_J = -40^\circ\text{C to }+150^\circ\text{C}$; Typical values are given at $V_{BB} = 12\text{ V}$ and $T_J = 25^\circ\text{C}$
Bus Load = $500\ \Omega$ (V_{BB} to LIN); unless otherwise specified.)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-------------------------------|---|---|------|------|------|------------------|
| LIN BUS LINE (PIN LIN) | | | | | | |
| I_{BUS_LIM} | Current limitation for Driver | Dominant State; $V_{LIN} = V_{BB_MAX}$ | 40 | | 200 | mA |
| $I_{BUS_PAS_dom}$ | Receiver Leakage current; Driver OFF | TxD = High; $V_{LIN} = 0\text{ V}$; $V_{BB} = 12\text{ V}$ | -1 | | | mA |
| I_{sleep} | Receiver Leakage current; see Figure 1 | Sleep mode; $V_{LIN} = 0\text{ V}$; $V_{BB} = 12\text{ V}$ | -16 | -8 | -3 | μA |
| $I_{BUS_PAS_rec}$ | Receiver Leakage current; Driver OFF; (Note 8) | TxD = High; $8\text{ V} < V_{BB} < 18\text{ V}$; $8\text{ V} < V_{LIN} < 18\text{ V}$; $V_{LIN} \geq V_{BB}$ | | | 20 | μA |
| $V_{SERDiode}$ | Voltage Drop on Serial Diode | Voltage drop on D_S , see Figure 1 | 0.4 | 0.7 | 1 | V |
| R_{SLAVE} | Internal Pull-up Resistance | see Figure 1 | 20 | 30 | 60 | $\text{k}\Omega$ |
| C_{LIN} | Capacitance on Pin LIN, (Note 8) | | | 20 | 30 | pF |

8. Values based on design and characterization. Not tested in production.

NCV7329

Table 5. AC CHARACTERISTICS ($V_{BB} = 5\text{ V to }18\text{ V}$; $T_J = -40^\circ\text{C to }+150^\circ\text{C}$; unless otherwise specified. For the transmitter parameters, the following bus loads are considered: $L1 = 1\text{ k}\Omega / 1\text{ nF}$; $L2 = 660\ \Omega / 6.8\text{ nF}$; $L3 = 500\ \Omega / 10\text{ nF}$)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|------------------------|--|---|-------|------|-------|---------------|
| LIN TRANSCEIVER | | | | | | |
| D1 | Duty Cycle 1 = $t_{BUS_REC(min)} / (2xt_{BIT})$ (See Figure 4) | $TH_{REC(max)} = 0.744 \times V_{BB}$ $TH_{DOM(max)} = 0.581 \times V_{BB}$ $t_{BIT} = 50\ \mu\text{s}$ $V_{BB} = 5\text{ V to }18\text{ V}$ | 0.396 | | 0.500 | |
| D2 | Duty Cycle 2 = $t_{BUS_REC(max)} / (2xt_{BIT})$ (See Figure 4) | $TH_{REC(min)} = 0.422 \times V_{BB}$ $TH_{DOM(min)} = 0.284 \times V_{BB}$ $t_{BIT} = 50\ \mu\text{s}$ $V_{BB} = 5\text{ V to }18\text{ V}$ | 0.500 | | 0.581 | |
| D3 | Duty Cycle 3 = $t_{BUS_REC(min)} / (2xt_{BIT})$ (See Figure 4) | $TH_{REC(max)} = 0.778 \times V_{BB}$ $TH_{DOM(max)} = 0.616 \times V_{BB}$ $t_{BIT} = 96\ \mu\text{s}$ $V_{BB} = 5\text{ V to }18\text{ V}$ | 0.417 | | 0.500 | |
| D4 | Duty Cycle 4 = $t_{BUS_REC(max)} / (2xt_{BIT})$ (See Figure 4) | $TH_{REC(min)} = 0.389 \times V_{BB}$ $TH_{DOM(min)} = 0.251 \times V_{BB}$ $t_{BIT} = 96\ \mu\text{s}$ $V_{BB} = 5\text{ V to }18\text{ V}$ | 0.500 | | 0.590 | |
| $t_{TX_PROP_DOWN}$ | Propagation Delay of TxD to LIN. TxD High to Low (See Figure 7) | | | | 14 | μs |
| $t_{TX_PROP_UP}$ | Propagation Delay of TxD to LIN. TxD Low to High (See Figure 7) | | | | 14 | μs |

LIN RECEIVER

| | | | | | | |
|---------------|---|---|-----|--|----|---------------|
| t_{RX_PD} | Propagation Delay of Receiver, Rising and falling Edge (See Figure 5) | $R_{RXD} = 2.4\text{ k}\Omega$; $C_{RXD} = 20\text{ pF}$ | 0.1 | | 6 | μs |
| t_{RX_SYM} | Propagation Delay Symmetry | $R_{RXD} = 2.4\text{ k}\Omega$; $C_{RXD} = 20\text{ pF}$; Rising edge with respect to falling edge | -2 | | +2 | μs |

MODE TRANSITIONS AND TIMEOUTS

| | | | | | | |
|--------------------|--|------------------------|----|----|-----|---------------|
| t_{LIN_WAKE} | Duration of LIN Dominant for Detection of Wake-up via LIN Bus (See Figure 6) | Sleep Mode | 40 | 70 | 150 | μs |
| $t_{TXD_TIMEOUT}$ | TxD Dominant Timeout | Normal Mode, TxD = Low | 14 | 25 | 46 | ms |
| t_{INIT_NORM} | Time From Rising Edge of EN pin to the moment when the transmitter is able to correctly transmit | | 15 | 30 | 75 | μs |
| t_{ENABLE} | Duration of EN pin in High Level State for transition to Normal Mode | | 11 | 20 | 55 | μs |
| $t_{DISABLE}$ | Duration of EN pin in Low Level State for transition to Sleep Mode | | 11 | 20 | 55 | μs |
| t_{TO_STB} | Delay from LIN Bus Dominant to Recessive Edge to Entering of Standby Mode after Valid LIN Wake-up (See Figure 6) | Sleep Mode | 5 | 10 | 40 | μs |

THERMAL SHUTDOWN

| | | | | | | |
|-------------|-------------------------------|--------------------|-----|-----|-----|------------------|
| $T_{J(sd)}$ | Shutdown Junction Temperature | Temperature Rising | 160 | 180 | 200 | $^\circ\text{C}$ |
|-------------|-------------------------------|--------------------|-----|-----|-----|------------------|

9. Values based on design and characterization. Not tested in production.

FUNCTIONAL DESCRIPTION

Overall Functional Description

LIN is a serial communication protocol that efficiently supports the control of mechatronic nodes in distributed automotive applications.

The NCV7329 contains the LIN transmitter, LIN receiver, power-on-reset (POR) circuits and thermal shutdown (TSD). The LIN transmitter is optimized for a maximum specified transmission speed of 20 kbps.

Table 6. OPERATING MODES

| Pin EN | Mode | Pin RxD | LIN bus |
|--------|-----------|----------------------------------|---------------|
| x | Unpowered | Floating | OFF; Floating |
| Low | Sleep | Floating | OFF; Floating |
| Low | Standby | Low indicates wake-up | OFF; 30 kΩ |
| High | Normal | LOW: dominant HIGH: recessive | ON; 30 kΩ |

Unpowered Mode

As long as V_{BB} remains below its power-on-reset level, the chip is kept in a safe unpowered state. The LIN transmitter is inactive, the LIN pin is left floating and only a weak pull-down is connected on pin TxD. Pin RxD remains floating.

The unpowered state will be entered from any other state when V_{BB} falls below its power-on-reset level (PORL_V_{BB}). When V_{BB} rises above the power-on-reset high threshold (PORH_V_{BB}), the NCV7329 switches to a Sleep mode.

Normal Mode

In the Normal mode, the full functionality of the LIN transceiver is available. The transceiver can transmit and receive data via the LIN bus with speed up to 20 kbps. Data according the state of TxD input are sent to the LIN bus while pin RxD reflects the logical symbol received on the LIN bus – high-impedant for recessive and Low for dominant. A 30 kΩ resistor in series with a reverse-protection diode is internally connected between LIN and V_{BB} pins.

The signal on pin TxD passes through a timer, which releases the bus in case the TxD remains low for longer than t_{TxD_TIMEOUT}. It prevents the LIN bus being permanently driven dominant and thus blocking all subsequent communication due to a failure of the application (e.g. software error). The transmission can continue once the TxD returns to High logical level.

In case the junction temperature increases above the thermal shutdown threshold (T_{J(sd)}), e.g. due to a short of the LIN wiring to the battery, the transmitter is disabled and releases the LIN bus to recessive. Once the junction temperature decreases back below the thermal shutdown level, the transmission can be enabled again. However, to avoid thermal oscillations, first a High logical level on TxD must be encountered before the transmitter is enabled.

As required by SAE J2602, the transceiver must behave safely below its operating range – it shall either continue to transmit correctly (according its specification) or remain silent (transmit a recessive state regardless of the TxD signal). A battery monitoring circuit in NCV7329 deactivates the transmitter in the Normal mode if the V_{BB} level drops below MONL_V_{BB}. Transmission is enabled again when V_{BB} reaches MONH_V_{BB}. The internal logic remains in the normal mode and the reception from the LIN line is still possible even if the battery monitor disables the transmission. Although the specifications of the monitoring and power-on-reset levels are overlapping, it's ensured by the implementation that the monitoring level never falls below the power-on-reset level.

The Normal mode can be entered from either Standby or Sleep mode when EN Pin is High for longer than t_{ENABLE}. When the transition is made from Standby mode, TxD pull-down is set to weak and RxD is put into a high-impedance immediately after EN becomes High (before the expiration of t_{ENABLE} filtering time). This excludes signal conflicts between the Standby mode pin settings and the signals required to control the chip in the Normal mode after a local wake-up vs. High logical level on TxD required to send a recessive symbol to the LIN bus.

Sleep Mode

Sleep mode provides extremely low current consumption. The LIN transceiver is inactive and the battery consumption is minimized.

This mode is entered in one of the following ways:

- After the voltage level at V_{BB} pin rises above its power-on-reset level (PORH_V_{BB}). In this case, RxD Pin remains high-impedant and the pull-down applied on pin TxD remains weak.
- After assigning Low logical level to pin EN for longer than t_{DISABLE} while NCV7329 is in the Normal mode.

Standby Mode

Standby mode is entered from the Sleep mode when a remote wake-up event occurred. The Low level on RxD pin indicates interrupt flag for the microcontroller.

NCV7329

OPERATING STATES

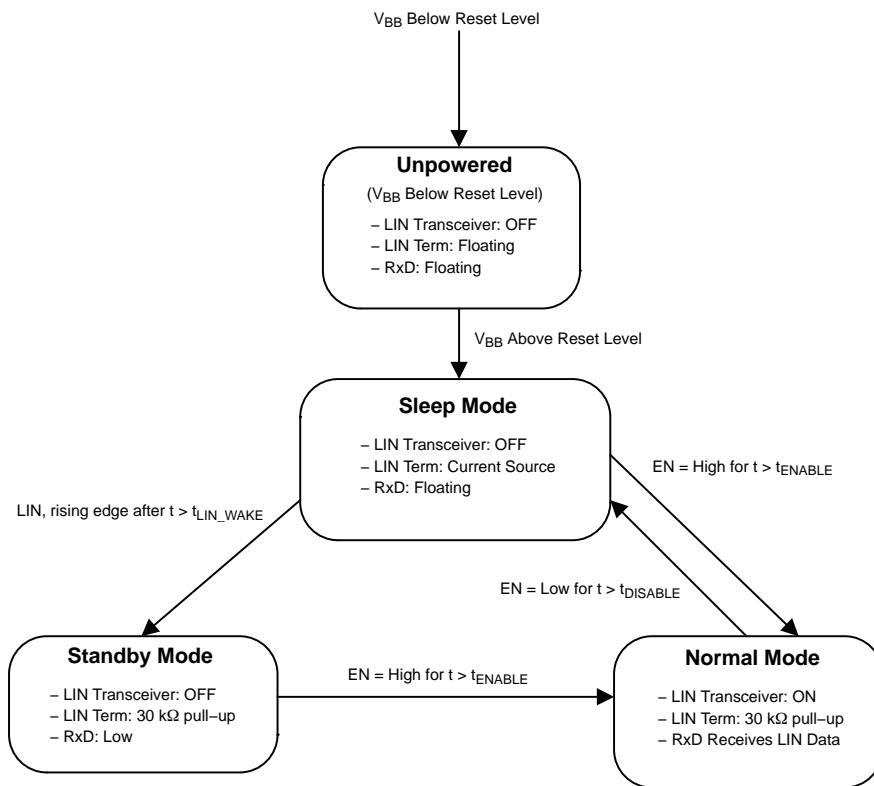


Figure 3. State Diagram

MEASUREMENT SETUPS AND DEFINITIONS

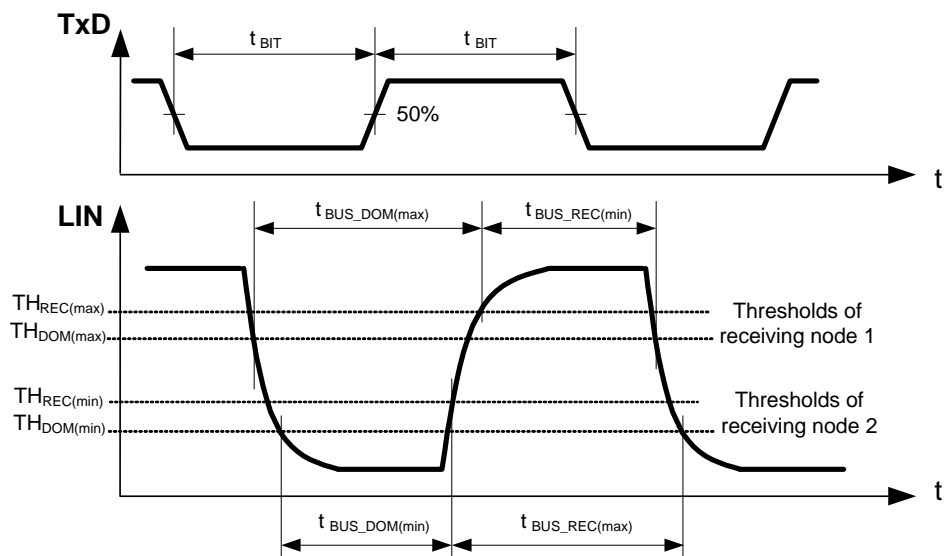


Figure 4. LIN Transmitter Duty Cycle

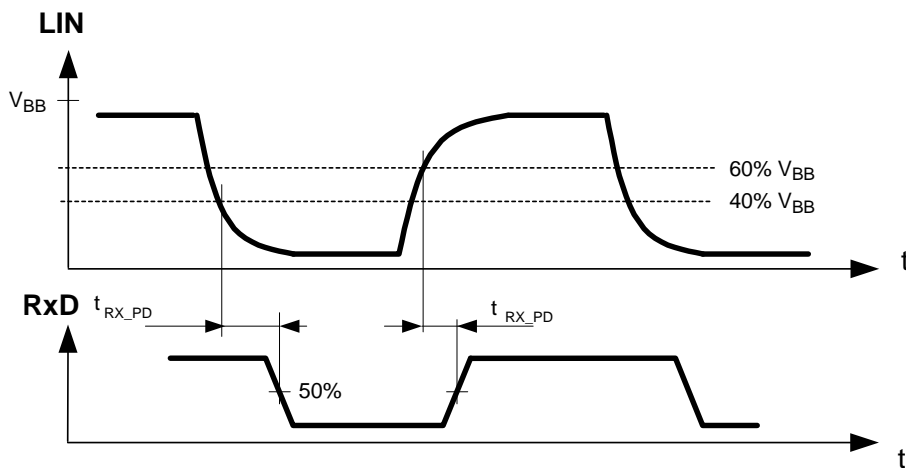


Figure 5. LIN Receiver Timing

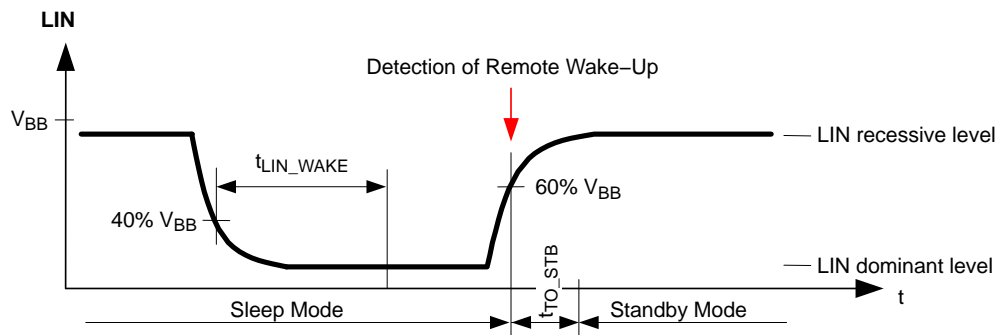


Figure 6. Remote (LIN) Wake-up Detection

NCV7329

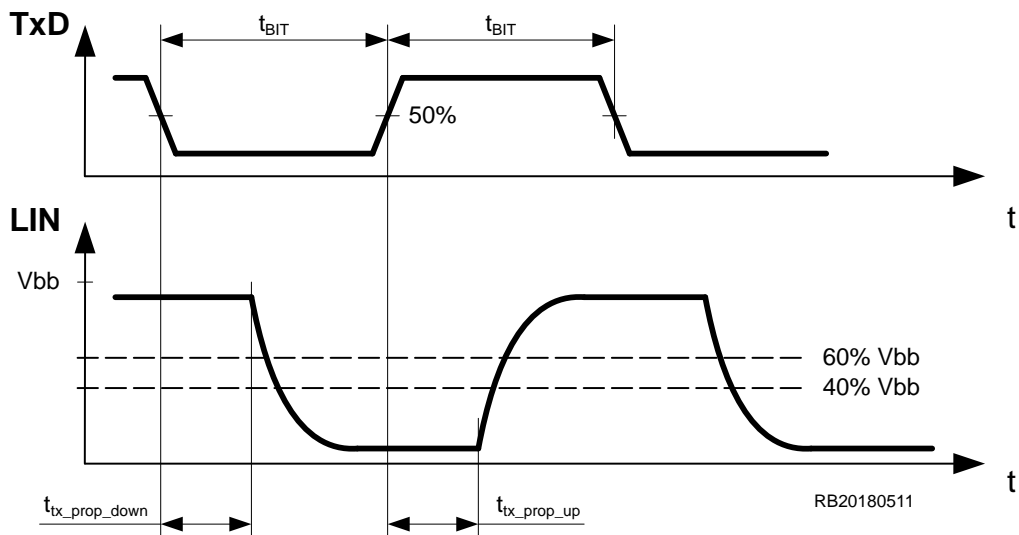


Figure 7. LIN Transmitter Timing

DEVICE ORDERING INFORMATION

| Part Number | Description | Temperature Range | Package | Shipping [†] |
|---------------|-----------------------------|-------------------|---------------------|-----------------------|
| NCV7329D10R2G | Stand-alone LIN Transceiver | -40°C to +125°C | SOIC-8 (Pb-Free) | 3000 / Tape & Reel |
| NCV7329MW0R2G | Stand-alone LIN Transceiver | -40°C to +125°C | DFN8 (Pb-Free) | 3000 / Tape & Reel |

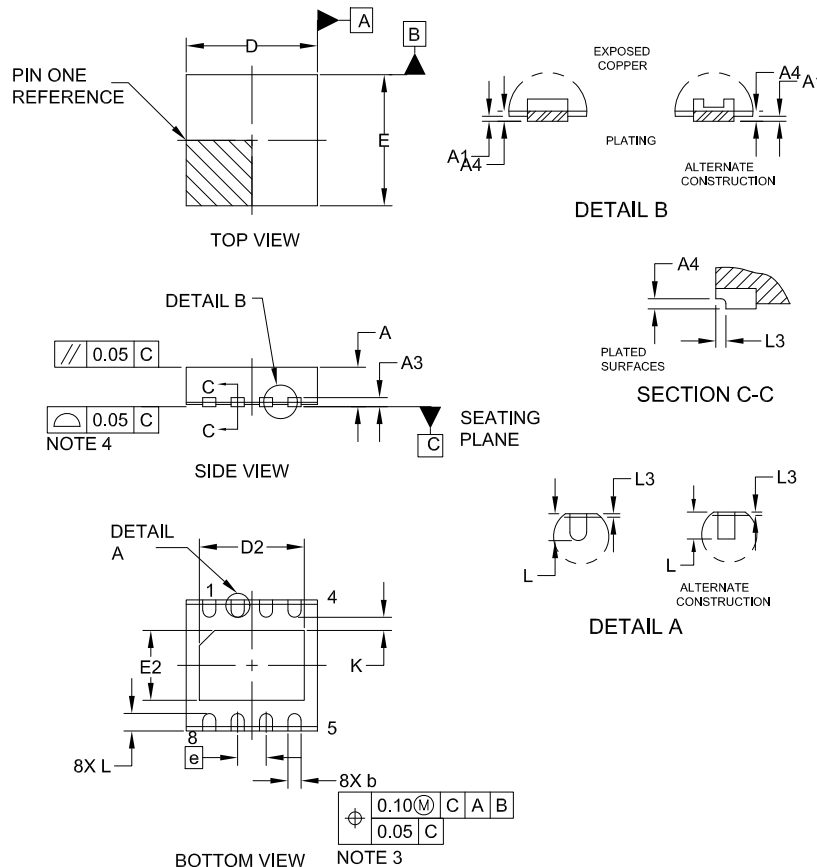
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 2:1

DFNW8 3x3, 0.65P
CASE 507AB
ISSUE E

DATE 02 JUL 2021

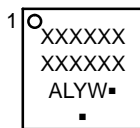


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

| DIM | MILLIMETERS | | |
|-----|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | 0.80 | 0.85 | 0.90 |
| A1 | — | — | 0.05 |
| A3 | 0.20 REF | | |
| A4 | 0.10 | — | — |
| b | 0.25 | 0.30 | 0.35 |
| D | 2.95 | 3.00 | 3.05 |
| D2 | 2.30 | 2.40 | 2.50 |
| E | 2.95 | 3.00 | 3.05 |
| E2 | 1.50 | 1.60 | 1.70 |
| e | 0.65 BSC | | |
| K | 0.30 REF | | |
| L | 0.35 | 0.40 | 0.45 |
| L3 | 0.00 | 0.05 | 0.10 |

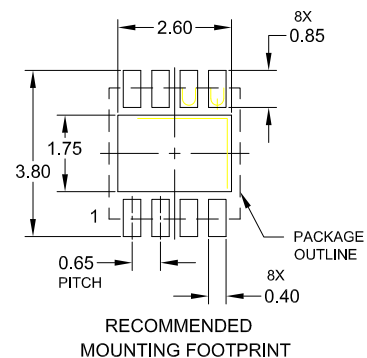
GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



| | | |
|------------------|------------------|--|
| DOCUMENT NUMBER: | 98AON14978G | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | DFNW8 3x3, 0.65P | PAGE 1 OF 1 |

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

| | | |
|------------------|-------------|--|
| DOCUMENT NUMBER: | 98ASB42564B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | SOIC-8 NB | PAGE 1 OF 2 |

onsemi and ONsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|---|--|--|--|
| <p>STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER</p> | <p>STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1</p> | <p>STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1</p> | <p>STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE</p> |
| <p>STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE</p> | <p>STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE</p> | <p>STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd</p> | <p>STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1</p> |
| <p>STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON</p> | <p>STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND</p> | <p>STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1</p> | <p>STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> |
| <p>STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> | <p>STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN</p> | <p>STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON</p> | <p>STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC</p> | <p>STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE</p> | <p>STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1</p> | <p>STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> |
| <p>STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6</p> | <p>STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND</p> | <p>STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT</p> | <p>STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT</p> | <p>STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC</p> | <p>STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN</p> | <p>STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN</p> |
| <p>STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1</p> | <p>STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1</p> | | |

| | | |
|-------------------------|--------------------|---|
| DOCUMENT NUMBER: | 98ASB42564B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | SOIC-8 NB | PAGE 2 OF 2 |

onsemi and **ONSEMI** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales