NCV7342

High Speed Low Power CAN Transceiver

Description

The NCV7342 CAN transceiver is the interface between a controller area network (CAN) protocol controller and the physical bus and may be used in both 12 V and 24 V systems. The transceiver provides differential transmit capability to the bus and differential receive capability to the CAN controller.

The NCV7342 is an addition to the CAN high−speed transceiver family complementing NCV734x CAN stand−alone transceivers and previous generations such as AMIS42665, AMIS3066x, etc.

Due to the wide common−mode voltage range of the receiver inputs and other design features, the NCV7342 is able to reach outstanding levels of electromagnetic susceptibility (EMS). Similarly, extremely low electromagnetic emission (EME) is achieved by the excellent matching of the output signals.

Features

- Compatible with the ISO 11898−2, ISO 11898−5 Standards
- High Speed (up to 1 Mbps)
- V_{IO} Pin on NCV7342−3 Version Allowing Direct Interfacing with 3 V to 5 V Microcontrollers
- V_{SPLIT} Pin on NCV7342−0 Version for Bus Common Mode Stabilization
- Very Low Current Consumption in Standby Mode with Wake−up via the Bus
- Excellent Electromagnetic Susceptibility (EMS) Level Over Full Frequency Range. Very Low Electromagnetic Emissions (EME) Low EME Also Without Common Mode (CM) Choke
- Bus Pins Protected Against >15 kV System ESD Pulses
- Transmit Data (TxD) Dominant Time−out Function
- Bus Dominant Time−out function in Standby Mode
- Under All Supply Condition the Chip Behaves Predictably
- No Disturbance of the Bus Lines with an Unpowered Node
- Thermal Protection
- Bus Pins Protected Against Transients in an Automotive Environment
- Bus Pins Short Circuit Proof to Supply Voltage and Ground
- These are Pb−Free Devices

Quality

- Wettable Flank Package for Enhanced Optical Inspection
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

Typical Applications

- Automotive
- Industrial Networks

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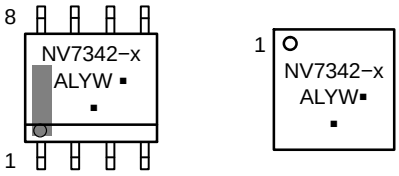
SOIC−8
D SUFFIX
CASE 751AZ

DFN8
MW SUFFIX
CASE 506DG

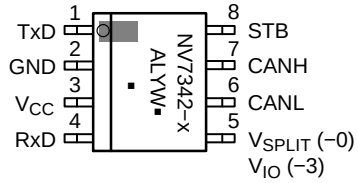
MARKING DIAGRAMS

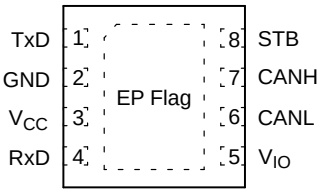


NV7342−x= Specific Device Code
x = 0 or 3
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENTS





(Top Views)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

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Table 1. KEY TECHNICAL CHARACTERISTICS AND OPERATING RANGES

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Power supply voltage		4.5		5.5	V
V_{UVVcc}	Undervoltage detection voltage on pin V_{CC} (NCV7342−3 only)		3.5		4.5	V
I_{CC}	Supply current	Dominant; V_{TxD} = 0 V Recessive; V_{TxD} = V_{IO}			75 10	mA
I_{CCS}	Supply current in standby mode including V_{IO} current	$T_J \leq 100°C$, (Note 1)			15	μA
V_{CANH}	DC voltage at pin CANH	0 < V_{CC} < 5.5 V; no time limit	−50		+50	V
V_{CANL}	DC voltage at pin CANL	0 < V_{CC} < 5.5 V; no time limit	−50		+50	V
$V_{CANH,L}$	DC voltage between CANH and CANL pin	0 < V_{CC} < 5.5 V	−50		+50	V
V_{ESD}	Electrostatic discharge voltage	IEC 61000−4−2 at pins CANH and CANL	−15		15	kV
$V_{O(dif)(bus_dom)}$	Differential bus output voltage in dominant state	45 Ω < R_{LT} < 65 Ω	1.5		3	V
CM−range	Input common−mode range for comparator	Guaranteed differential receiver threshold and leakage current	−35		+35	V
C_{load}	Load capacitance on IC outputs				15	pF
t_{pd_dr}	Propagation delay TxD to RxD dominant to recessive transition See Figure 8	C_i = 100 pF between CANH to CANL, C_{RxD} = 15 pF	50	100	230	ns
t_{pd_rd}	Propagation delay TxD to RxD recessive to dominant transition See Figure 8	C_i = 100 pF between CANH to CANL, C_{RxD} = 15 pF	50	120	230	ns
T_J	Junction temperature		−40		150	°C

1. Not tested in production. Guaranteed by design and prototype evaluation.

BLOCK DIAGRAMS

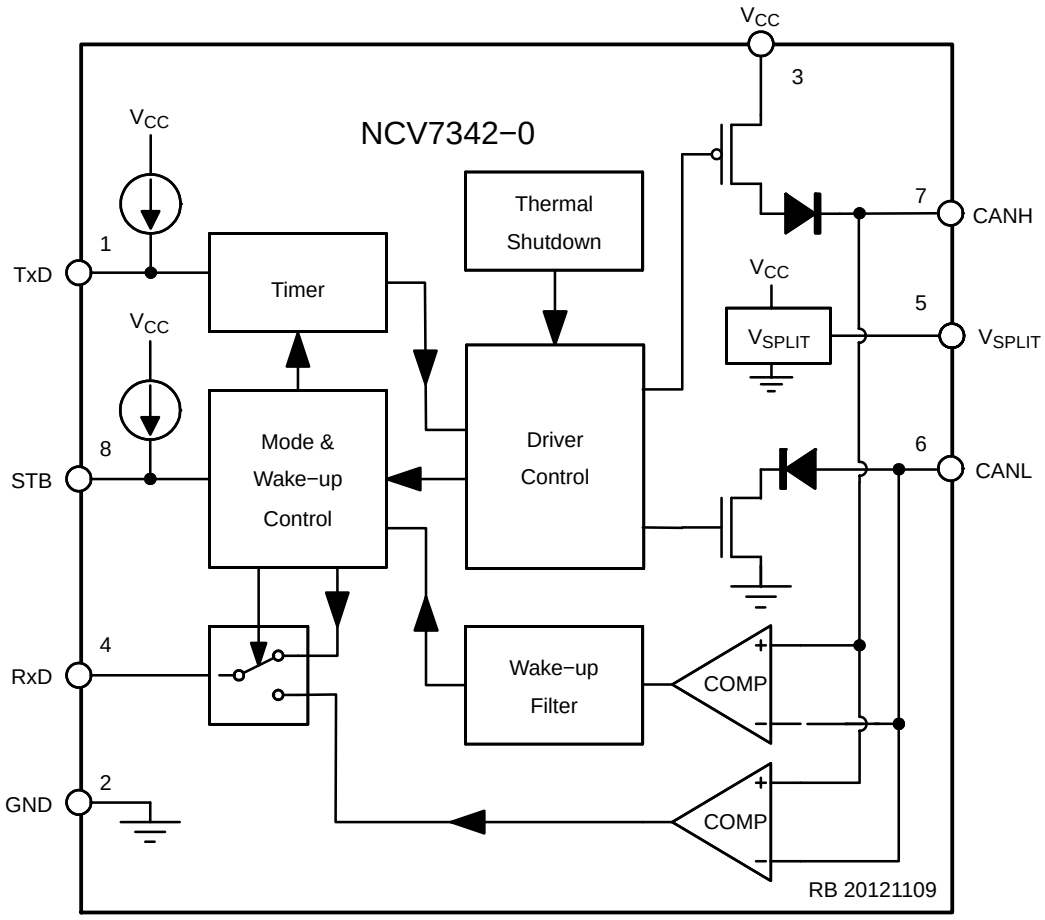


Figure 1. NCV7342−0 Block Diagram

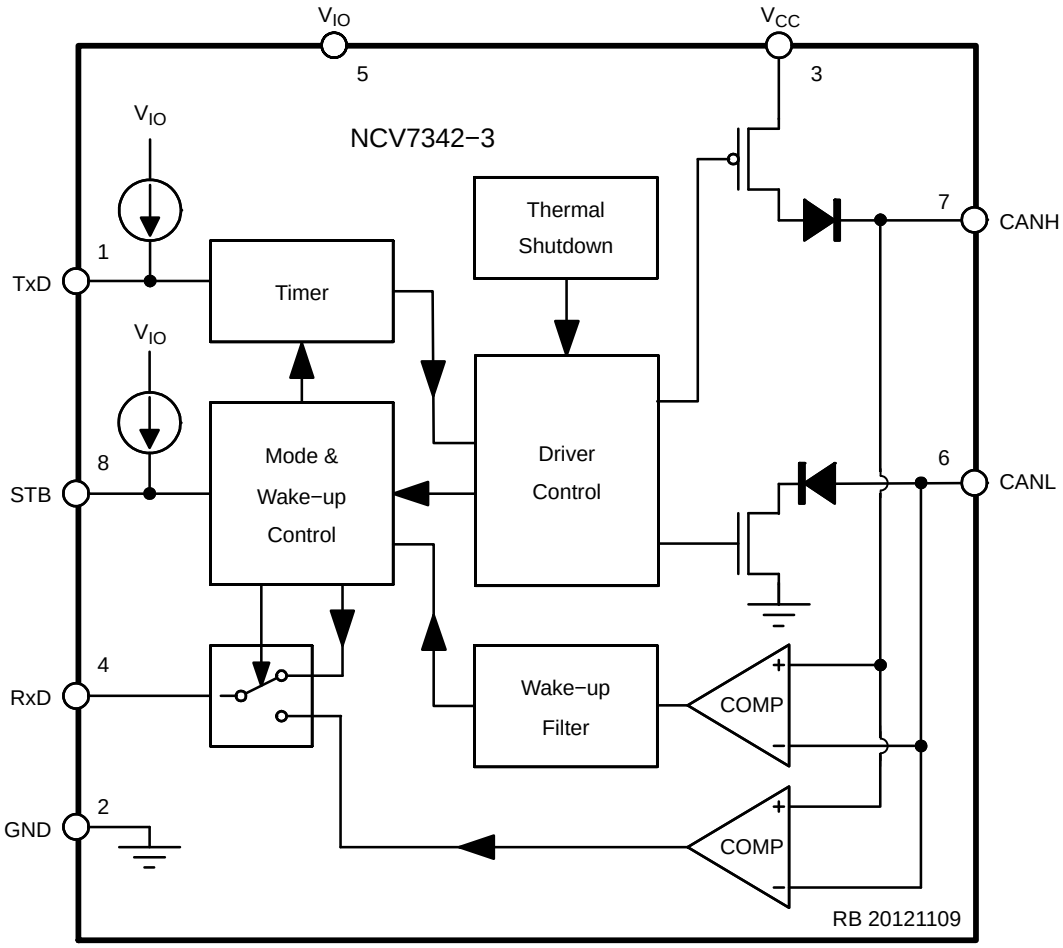


Figure 2. NCV7342−3 Block Diagram

TYPICAL APPLICATION

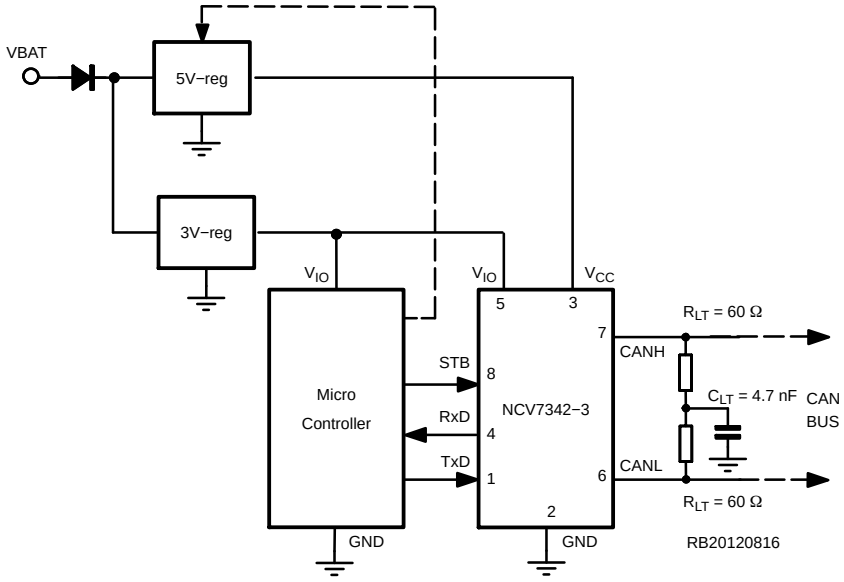


Figure 3. Application Diagram NCV7342−3

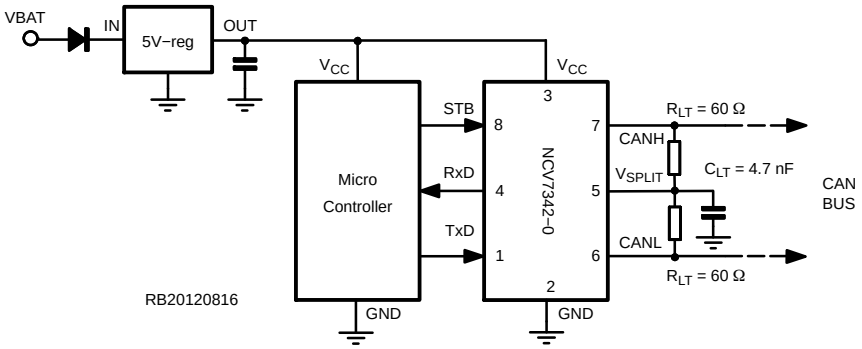


Figure 4. Application Diagram NCV7342−0

Table 2. PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	TxD	Transmit data input; Low input → dominant driver; internal pull−up current
2	GND	Ground
3	V_{CC}	Supply voltage
4	RxD	Receive data output; dominant transmitter → Low output
5 5	V_{IO} V_{SPLIT}	Input/Output pins supply voltage. On NCV7342−3 only Common−mode stabilization output. On NCV7342−0 only
6	CANL	Low−level CAN bus line (Low in dominant mode)
7	CANH	High−level CAN bus line (High in dominant mode)
8	STB	Standby mode control input
EP	Exposed Pad	Connect to GND or left floating

FUNCTIONAL DESCRIPTION

NCV7342 has two versions which differ from each other only by function of pin 5.

NCV7342−0: Pin 5 is common mode stabilization output V_{SPLIT}. (see Figure 4) This version is full replacement of NCV7340.

NCV7342−3: Pin 5 is V_{IO} pin, which is supply pin for transceiver digital inputs/output (supplying pins TxD, RxD, STB) The V_{IO} pin should be connected to microcontroller supply pin. By using V_{IO} supply pin shared with microcontroller, the I/O levels between microcontroller and transceiver are properly adjusted. This adjustment allows communication between 3 V microcontroller and the transceiver. (See Figure 3)

Operating Modes

NCV7342 provides two modes of operation as illustrated in Table 3. These modes are selectable through pin STB.

Table 3. OPERATING MODES

Pin STB	Mode	Pin RxD	
		Low	High
Low	Normal	Bus dominant	Bus recessive
High	Standby	Wake−up request detected	No wake−up request detected

Normal Mode

In normal mode, the transceiver is able to communicate via the bus lines. The signals are transmitted and received to the CAN controller via the pins TxD and RxD. The slopes on the bus lines outputs are optimized to give extremely low EME.

Standby Mode

In standby mode both the transmitter and receiver are disabled and a very low−power differential receiver monitors the bus lines for CAN bus activity. The bus lines are terminated to ground and supply current is reduced to a minimum, typically 10 μA. When a wake−up request is detected by the low−power differential receiver, the signal is first filtered and then verified as a valid wake signal after a time period of $t_{dwakerd}$. The RxD pin is driven Low by the transceiver to inform the controller of the wake−up request.

V_{IO} Supply Pin

The V_{IO} pin (available only on NCV7342−3 version) should be connected to microcontroller supply pin. By using V_{IO} supply pin shared with microcontroller the I/O levels between microcontroller and transceiver are properly adjusted. See Figure 3. Pin V_{IO} also provides the internal supply voltage for low−power differential receiver of the transceiver. This allows detection of wake−up request even when there is no supply voltage on Pin V_{CC}.

Split Circuit

The V_{SPLIT} pin (available on NCV7342−0 version) is operational only in normal mode. In standby mode this pin is floating. The V_{SPLIT} can be connected as shown in Figure 4 or, if it's not used, can be left floating. Its purpose is to provide a stabilized DC voltage of $0.5 \cdot V_{CC}$ to the bus reducing possible steps in the common−mode signal, therefore reducing EME. These unwanted steps could be caused by an unpowered node on the network with excessive leakage current from the bus that shifts the recessive voltage from its nominal $0.5 \cdot V_{CC}$ voltage.

Wake−up

When a valid wake−up (dominant state longer than t_{Wake}) is received during the standby mode, the RxD pin is driven Low after $t_{dwakerd}$. The wake−up detection is not latched: RxD returns to High state after $t_{dwakedr}$ when the bus signal is released back to recessive – see Figure 5.

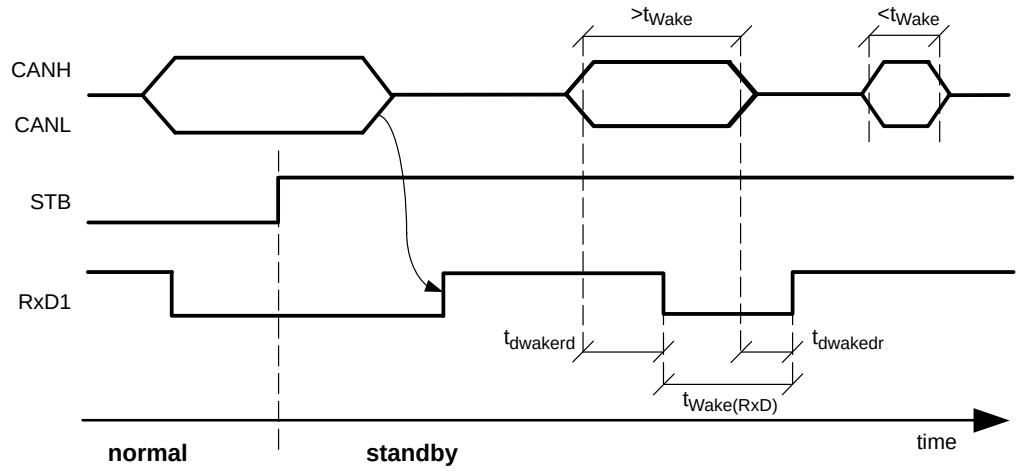


Figure 5. NCV7342 Wake−up behavior

Over−temperature Detection

A thermal protection circuit protects the IC from damage by switching off the transmitter if the junction temperature exceeds a value of approximately 180°C. Because the transmitter dissipates most of the power, the power dissipation and temperature of the IC is reduced. All other IC functions continue to operate. The transmitter off−state resets when the temperature decreases below the shutdown threshold and pin TxD goes High. The thermal protection circuit is particularly needed in case of a bus line failure.

TxD Dominant Time−out Function

A TxD dominant time−out timer circuit prevents the bus lines being driven to a permanent dominant state (blocking all network communication), if pin TxD is forced permanently Low by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TxD. If the duration of the low−level on pin TxD exceeds the internal timer value $t_{dom(TxD)}$, the transmitter is disabled, driving the bus into a recessive state. The timer is reset by a positive edge on pin TxD.

This TxD dominant time−out time ($t_{dom(TxD)}$) limits the minimum possible bit rate to 8 kbps.

Bus Dominant Time−out Function

Bus dominant time−out timer is started in the standby mode when CAN bus changes from recessive to dominant state. If the dominant state on the bus is kept for longer time than $t_{dom(bus)}$, the RxD pin is released to High level. The timer is reset when CAN bus changes from dominant to recessive state. This feature prevents generating permanent wake−up request by the bus clamped to the dominant level.

Fail Safe Features

A current−limiting circuit protects the transmitter output stage from damage caused by an accidental short circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

V_{CC} supply dropping below V_{UVVcc} undervoltage level will force transceiver to switch into the standby mode. The logic level on pin STB will be ignored as long as undervoltage condition is not recovered. (NCV7342−3 version only)

V_{IO} supply dropping below V_{UVDVIO} undervoltage detection level will cause the transceiver to disengage from the bus (no bus loading) until the V_{IO} voltage recovers. (NCV7342−3 version only)

The pins CANH and CANL are protected against automotive electrical transients (according to ISO 7637; see Figure 6). Pins TxD and STB are pulled High internally should the input become disconnected. Pins TxD, STB and RxD will be floating, preventing reverse supply should the V_{CC} supply be removed.

ELECTRICAL CHARACTERISTICS

Definitions

All voltages are referenced to GND (pin 2). Positive currents flow into the IC. Sinking current means the current is flowing into the pin; sourcing current means the current is flowing out of the pin.

Table 4. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{SUP}	Supply voltage V_{CC}, V_{IO}		−0.3	+6	V
V_{CANH}	DC voltage at pin CANH	0 < V_{CC} < 5.5 V; no time limit	−50	+50	V
V_{CANL}	DC voltage at pin CANL	0 < V_{CC} < 5.5 V; no time limit	−50	+50	V
$V_{CANH,Lmax}$	DC voltage at pin CANH and CANL during load dump condition	0 < V_{CC} < 5.5 V; less than one second	−	58	V
V_{SPLIT}	DC voltage at V_{SPLIT} pin (On NCV7342−0 version only)	0 < V_{CC} < 5.5 V; no time limit	−50	+50	V
V_{IO}	DC voltage at pin TxD, RxD, STB		−0.3	+6	V
V_{esd}	Electrostatic discharge voltage at all pins according to EIA−JESD22	(Note 2)	−4	+4	kV
	Standardized charged device model ESD pulses according to ESD−STM5.3.1−1999		−750	+750	V
	Electrostatic discharge voltage at CANH,CANL, V_{SPLIT} pins according to EIA−JESD22	(Note 2)	−8	+8	kV
	Electrostatic discharge voltage at CANH, CANL pins According to IEC 61000−4−2	(Note 3)	−15	+15	kV
V_{schaff}	Transient voltage at CANH, CANL pins, See Figure 6	(Note 4)	−150	+100	V
Latch−up	Static latch−up at all pins	(Note 5)		150	mA
T_{stg}	Storage temperature		−55	+150	°C
T_{amb}	Ambient temperature		−40	+125	°C
T_J	Maximum junction temperature		−40	+170	°C
MSL	Moisture Sensitivity Level SOIC		2		−
MSL	Moisture Sensitivity Level DFN		1		−
T_{SLD}	Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 6)		260		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Standardized human body model electrostatic discharge (ESD) pulses in accordance to EIA−JESD22. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
3. System human body model electrostatic discharge (ESD) pulses. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor referenced to GND. Verified by external test house
4. Pulses 1, 2a,3a and 3b according to ISO 7637 part 3. Verification by external test house.
5. Static latch−up immunity: Static latch−up protection level when tested according to EIA/JESD78.
6. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

Table 5. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, SOIC−8 (Note 7) Thermal Resistance, Junction−to−Air, Free air, 1S0P PCB (Note 8) Thermal Resistance, Junction−to−Air, Free air, 2S2P PCB (Note 9)	 $R_{\theta JA}$ $R_{\theta JA}$	 125 75	 °C/W °C/W
Thermal Characteristics, DFN−8, 3x3 mm (Note 7) Thermal Resistance, Junction−to−Air, Free air, 1S0P PCB (Note 8) Thermal Resistance, Junction−to−Air, Free air, 2S2P PCB (Note 9)	 $R_{\theta JA}$ $R_{\theta JA}$	 140 47	 °C/W °C/W

7. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
8. Values based on test board according to EIA/JEDEC Standard JESD51−3, signal layer with 10% trace coverage.
9. Values based on test board according to EIA/JEDEC Standard JESD51−7, signal layers with 10% trace coverage for the signal layer and 4 thermal vias connected between exposed pad and first inner Cu layer.

Table 6. CHARACTERISTICS
V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8V to 5.5 V (Note 10); T_J = −40 to +150°C; R_{LT} = 60 Ω unless specified otherwise. On chip versions without V_{IO} pin reference voltage for all digital inputs and outputs is V_{CC} instead of V_{IO}.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY (Pin V_{CC})						
I_{CC}	Supply current	Dominant; V_{TxD} = 0 V Recessive; V_{TxD} = V_{IO}		50 6.8	75 10	mA
I_{CCS0}	Supply current in standby mode for NCV7342−0	$T_J \leq$ 100°C (Note 11)		8	15	μA
I_{CCS3}	Supply current in standby mode for NCV7342−3 including current into V_{IO}	$T_J \leq$ 100°C (Note 11)			17	μA
V_{UVVcc}	Undervoltage detection voltage on V_{CC} pin (NCV7342−3 only)		3.5		4.5	V
TRANSMITTER DATA INPUT (Pin TxD)						
V_{IH}	High−level input voltage	Output recessive	2.0		6	V
V_{IL}	Low−level input voltage	Output dominant	−0.3		+0.8	V
I_{IH}	High−level input current	V_{TxD} = V_{IO}	−5	0	+5	μA
I_{IL}	Low−level input current	V_{TxD} = 0V	−385	−200	−45	μA
C_i	Input capacitance	Not tested		5	10	pF
TRANSMITTER MODE SELECT (Pin STB)						
V_{IH}	High−level input voltage	Standby mode	2.0		V_{IO}+0.3 (Note 12)	V
V_{IL}	Low−level input voltage	Normal mode	−0.3		+0.8	V
I_{IH}	High−level input current	V_{STB} = V_{IO}	−5	0	+5	μA
I_{IL}	Low−level input current	V_{STB} = 0 V	−10	−4	−1	μA
C_i	Input capacitance	Not tested		5	10	pF
RECEIVER DATA OUTPUT (Pin RxD)						
I_{OH}	High−level output current	Normal mode V_{RxD} = V_{IO} − 0.4 V	−1.2	−0.4	−0.1	mA
I_{OL}	Low−level output current	V_{RxD} = 0.4 V	1.5	6	12	mA
V_{OH}	High−level output voltage	Standby mode I_{RxD} = −100 μA	V_{IO} − 1.1	V_{IO} −0.7	V_{IO} − 0.4	V
BUS LINES (Pins CANH and CANL)						
$V_{o(reces)\ (norm)}$	Recessive bus voltage on pins CANH and CANL	V_{TxD} = V_{IO}; no load; normal mode	2.0	2.5	3.0	V
$V_{o(reces)\ (stby)}$	Recessive bus voltage on pins CANH and CANL	V_{TxD} = V_{IO}; no load; standby mode	−100	0	+100	mV
$I_{o(reces)\ (CANH)}$	Recessive output current at pin CANH	−30 V < V_{CANH}< 35 V; 0 V < V_{CC} < 5.5 V	−2.5		+2.5	mA
$I_{o(reces)\ (CANL)}$	Recessive output current at pin CANL	−30 V < V_{CANL} < 35 V; 0 V <V_{CC} < 5.5 V	−2.5		+2.5	mA
$I_{LI(CANH)}$	Input leakage current to pin CANH	0Ω < R(V_{CC} to GND) < 1 MΩ 0Ω < R(V_{IO} to GND) < 1 MΩ V_{CANL} = V_{CANH} = 5 V (Note 10)	−10	0	+10	μA
$I_{LI(CANL)}$	Input leakage current to pin CANL		−10	0	+10	μA
$V_{o(dom)\ (CANH)}$	Dominant output voltage at pin CANH	V_{TxD} = 0 V	3.0	3.6	4.25	V

10. Only version NCV7342−3 has V_{IO} supply pin. In NCV7342−0 this supply is provided from V_{CC} pin.
11. Not tested in production. Guaranteed by design and prototype evaluation.
12. In case V_{IO} > V_{CC}, the limit is V_{IO} + 0.3 V

Table 6. CHARACTERISTICS
V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8V to 5.5 V (Note 10); T_J = −40 to +150°C; R_{LT} = 60 Ω unless specified otherwise. On chip versions without V_{IO} pin reference voltage for all digital inputs and outputs is V_{CC} instead of V_{IO}.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BUS LINES (Pins CANH and CANL)						
$V_{o(dom)\ (CANL)}$	Dominant output voltage at pin CANL	V_{TxD} = 0 V	0.5	1.4	1.75	V
$V_{o(dif)\ (bus_dom)}$	Differential bus output voltage ($V_{CANH} - V_{CANL}$)	V_{TxD} = 0 V; dominant; 45 Ω < R_{LT} < 65 Ω	1.5	2.25	3.0	V
$V_{o(dif)\ (bus_rec)}$	Differential bus output voltage ($V_{CANH} - V_{CANL}$)	V_{TxD} = V_{IO}; recessive; no load	−120	0	+50	mV
$V_{o(sym)\ (bus_dom)}$	Bus output voltage symmetry $V_{CANH} + V_{CANL}$	V_{TxD} = 0 V	0.9		1.1	V_{CC}
$I_{o(sc)\ (CANH)}$	Short circuit output current at pin CANH	V_{CANH} = 0 V; V_{TxD} = 0 V	−90	−70	−40	mA
$I_{o(sc)\ (CANL)}$	Short circuit output current at pin CANL	V_{CANL} = 36 V; V_{TxD} = 0 V	40	70	100	mA
$V_{i(dif)\ (th)}$	Differential receiver threshold voltage	−12 V < V_{CANL} < 12 V; −12 V < V_{CANH} < 12 V; V_{CC} = 4.75 V to 5.25 V	0.5	0.7	0.9	V
$V_{ihcm(dif)\ (th)}$	Differential receiver threshold voltage for high common−mode	−30 V < V_{CANL} < 35 V; −30 V < V_{CANH} < 35 V; V_{CC} = 4.75 V to 5.25 V	0.40	0.7	1.0	V
$V_{i(dif)\ (th)_STDBY}$	Differential receiver threshold voltage in standby mode	−12 V < V_{CANL} < 12 V; −12 V < V_{CANH} < 12 V; V_{CC} = 4.5 V to 5.5 V	0.4	0.8	1.15	V
$R_{i(cm)\ (CANH)}$	Common−mode input resistance at pin CANH		15	26	37	kΩ
$R_{i(cm)\ (CANL)}$	Common−mode input resistance at pin CANL		15	26	37	kΩ
$R_{i(cm)\ (m)}$	Matching between pin CANH and pin CANL common mode input resistance	V_{CANH} = V_{CANL}	−0.8	0	+0.8	%
$R_{i(dif)}$	Differential input resistance		25	50	75	kΩ
$C_{i(CANH)}$	Input capacitance at pin CANH	V_{TxD} = V_{IO}; not tested		7.5	20	pF
$C_{i(CANL)}$	Input capacitance at pin CANL	V_{TxD} = V_{IO}; not tested		7.5	20	pF
$C_{i(dif)}$	Differential input capacitance	V_{TxD} = V_{IO} ; not tested		3.75	10	pF
COMMON−MODE STABILIZATION (Pin V_{SPLIT}) Only for NCV7342−0 version						
V_{SPLIT}	Reference output voltage at pin V_{SPLIT}	Normal mode; −500 μA < I_{SPLIT} < 500 μA	0.3		0.7	V_{CC}
V_{SPLITo}	Reference output voltage at pin V_{SPLIT}	$R_{loadVsplit}$ > 1 MΩ	0.45		0.55	V_{CC}
$I_{SPLIT(i)}$	V_{SPLIT} leakage current	Standby mode	−5		+5	μA
$I_{SPLIT(lim)}$	V_{SPLIT} limitation current	Normal mode	1.3		5	mA
V_{IO} SUPPLY VOLTAGE (Pin V_{IO}) Only for NCV7342−3 version						
V_{IO}	Supply voltage on pin V_{IO}		2.8		5.5	V
I_{IOS}	Supply current on pin V_{IO} in standby mode	$T_J \leq$ 100°C (Note 11)			14	μA

10. Only version NCV7342−3 has V_{IO} supply pin. In NCV7342−0 this supply is provided from V_{CC} pin.
11. Not tested in production. Guaranteed by design and prototype evaluation.
12. In case V_{IO} > V_{CC}, the limit is V_{IO} + 0.3 V

Table 6. CHARACTERISTICS
V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8V to 5.5 V (Note 10); T_J = −40 to +150°C; R_{LT} = 60 Ω unless specified otherwise. On chip versions without V_{IO} pin reference voltage for all digital inputs and outputs is V_{CC} instead of V_{IO}.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IO} SUPPLY VOLTAGE (Pin V_{IO}) Only for NCV7342−3 version						
I_{IONM}	Supply current on pin V_{IO}	Normal mode Dominant; V_{TxD} = 0 V Recessive; V_{TxD} = V_{IO}	 0.30 0.29	 0.70 0.44	 1.10 0.68	mA
V_{UVDVIO}	Undervoltage detection voltage on V_{IO} pin		1.3		2.7	V
THERMAL SHUTDOWN						
$T_{J(SD)}$	Shutdown junction temperature	junction temperature rising	160	180	200	°C
TIMING CHARACTERISTICS (See Figure 7 and 8)						
$t_{d(TxD-BUSon)}$	Delay TxD to bus active	C_i = 100 pF between CANH to CANL		60		ns
$t_{d(TxD-BUSoff)}$	Delay TxD to bus inactive	C_i = 100 pF between CANH to CANL		30		ns
$t_{d(BUSon-RxD)}$	Delay bus active to RxD	C_{RxD} = 15 pF		60		ns
$t_{d(BUSoff-RxD)}$	Delay bus inactive to RxD	C_{RxD} = 15 pF		70		ns
t_{pd_dr}	Propagation delay TxD to RxD dominant to recessive transition See Figure 8	C_i = 100 pF between CANH to CANL, C_{RxD} = 15 pF	50	100	230	ns
t_{pd_rd}	Propagation delay TxD to RxD recessive to dominant transition See Figure 8	C_i = 100 pF between CANH to CANL, C_{RxD} = 15 pF	50	120	230	ns
$t_{d(stb-nm)}$	Delay standby mode to normal mode				47	μs
t_{Wake}	Dominant time for wake−up via bus		0.5	2.1	5	μs
$t_{dwakerd}$	Delay to flag wake event (recessive to dominant transitions) See Figure 5	Valid bus wake−up event, C_{RxD} = 15 pF	1	3.5	10	μs
$t_{dwakedr}$	Delay to flag end of wake event (dominant to recessive transition) See Figure 5	Valid bus wake−up event, C_{RxD} = 15 pF	0.5	2.6	6	μs
$t_{Wake(RxD)}$	Minimum pulse width on RxD See Figure 5	5 μs t_{Wake} C_{RxD} = 15 pF	0.5			μs
$t_{dom(TxD)}$	TxD dominant time for time out	V_{TxD} = 0 V	1.3		5	ms
$t_{dom(bus)}$	Bus dominant time out	Standby mode	1.3		5	ms

10. Only version NCV7342−3 has V_{IO} supply pin. In NCV7342−0 this supply is provided from V_{CC} pin.
11. Not tested in production. Guaranteed by design and prototype evaluation.
12. In case V_{IO} > V_{CC}, the limit is V_{IO} + 0.3 V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

MEASUREMENT SET−UPS AND DEFINITIONS

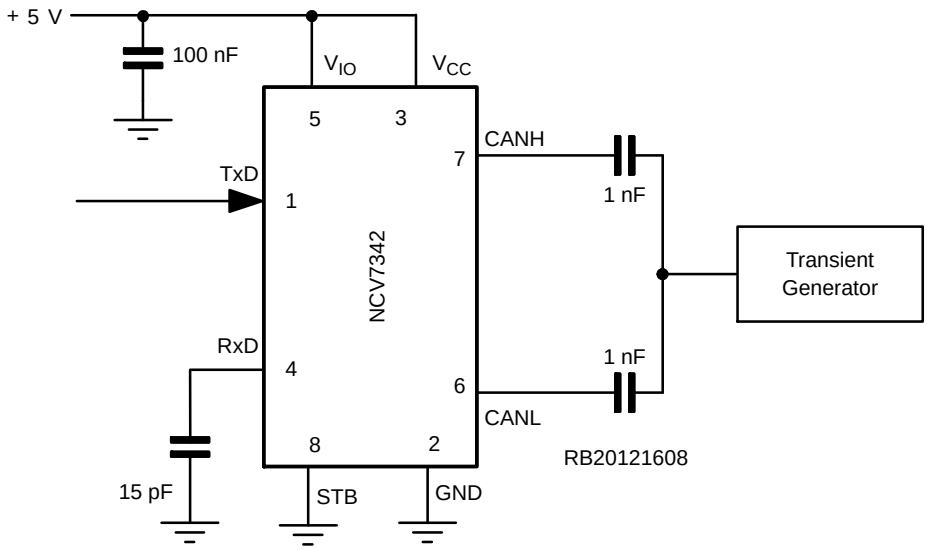


Figure 6. Test Circuit for Automotive Transients

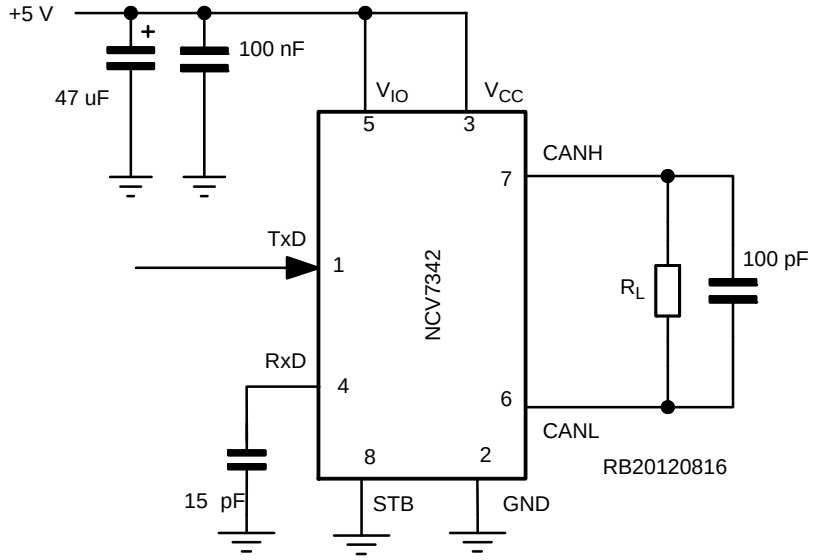


Figure 7. Test Circuit for Timing Characteristics

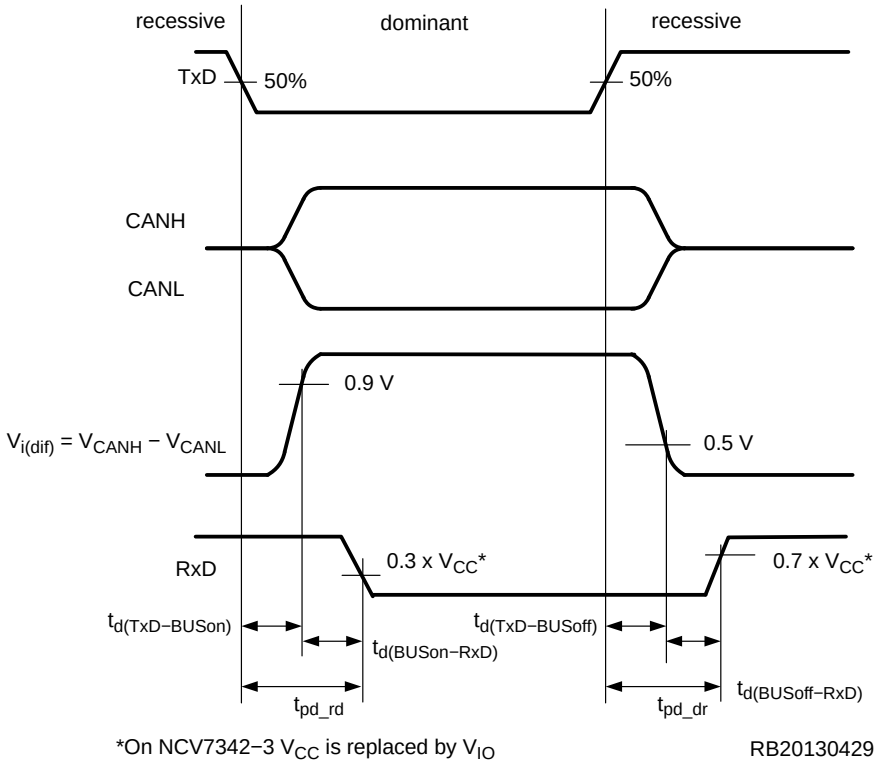


Figure 8. Transceiver Timing Diagram

DEVICE ORDERING INFORMATION

Part Number	Description	Package	Shipping†
NCV7342D10R2G	High Speed CAN Transceiver with Standby and V_{SPLIT} pin	SOIC 150 8 GREEN (Matte Sn, JEDEC MS−012) (Pb−Free)	3000 / Tape & Reel
NCV7342D13R2G	High Speed CAN Transceiver with Standby and V_{IO} pin		
NCV7342MW3R2G	High Speed CAN Transceiver with Standby and V_{IO} pin	DFN 8 Wettable Flank (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

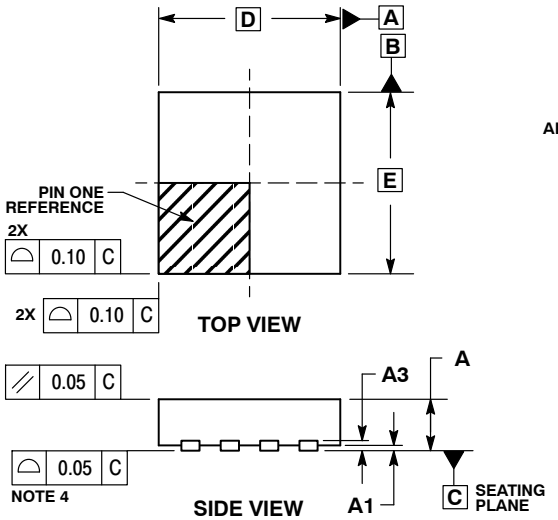
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

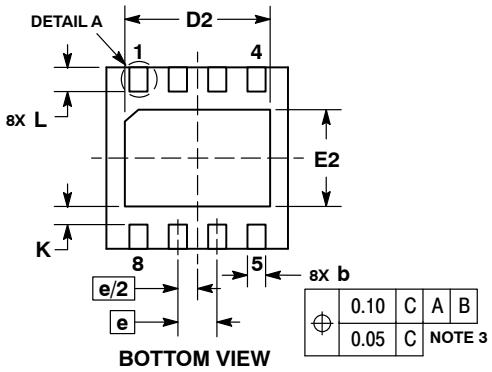
ON Semiconductor®

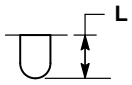
DFN8, 3x3, 0.65P
CASE 506DG
ISSUE A

DATE 28 APR 2016

SCALE 2:1





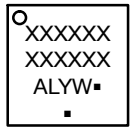


DETAIL A
ALTERNATE TERMINAL CONSTRUCTION

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	3.00 BSC	
D2	2.30	2.50
E	3.00 BSC	
E2	1.50	1.70
e	0.65 BSC	
K	0.30 TYP	
L	0.35	0.45

GENERIC MARKING DIAGRAM*

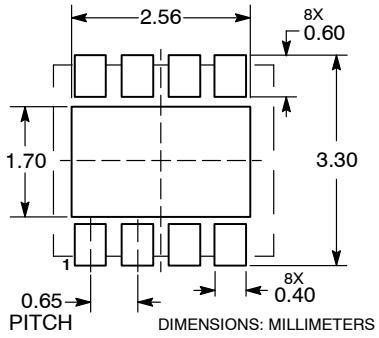


XXXXXX= Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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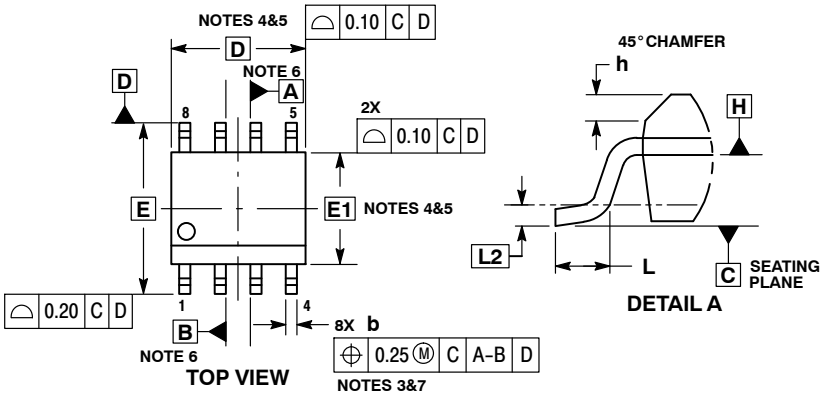
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

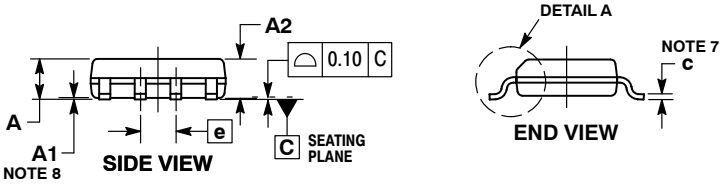
ON Semiconductor®

SCALE 1:1

SOIC−8
CASE 751AZ
ISSUE B

DATE 18 MAY 2015

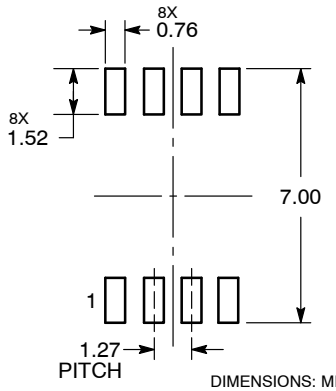




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006 mm PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.75
A1	0.10	0.25
A2	1.25	---
b	0.31	0.51
c	0.10	0.25
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
h	0.25	0.41
L	0.40	1.27
L2	0.25 BSC	

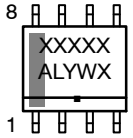
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

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