

NTTFS5116PL

MOSFET – Power -60 V, -20 A, 52 mΩ

Features

- Low $R_{DS(on)}$
- Fast Switching
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Load Switches
- DC Motor Control
- DC-DC Conversion

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	-60	V
Gate-to-Source Voltage			V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	-5.7	A
		$T_A = 100^{\circ}\text{C}$		-4.0	
Power Dissipation $R_{\theta JA}$ (Note 1)		$T_A = 25^{\circ}\text{C}$	P_D	3.2	W
		$T_A = 100^{\circ}\text{C}$		1.6	
Continuous Drain Current $R_{\theta JC}$ (Note 1)		$T_C = 25^{\circ}\text{C}$	I_D	-20	A
		$T_C = 100^{\circ}\text{C}$		-14	
Power Dissipation $R_{\theta JC}$ (Note 1)		$T_C = 25^{\circ}\text{C}$	P_D	40	W
		$T_C = 100^{\circ}\text{C}$		20	
Pulsed Drain Current	$t_p = 10\ \mu\text{s}$	I_{DM}	-76	A	
Operating Junction and Storage Temperature			T_J , T_{stg}	-55 to +175	$^{\circ}\text{C}$
Source Current (Body Diode)			I_S	-20	A
Single Pulse Drain-to-Source Avalanche Energy	$L = 0.1\ \text{mH}$	E_{AS}	45	mJ	
		I_{AS}	30	A	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 1)	$R_{\theta JC}$	3.8	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	47	

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).

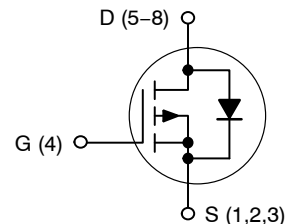


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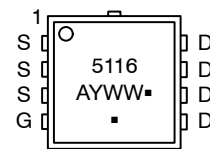
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
-60 V	52 mΩ @ -10 V	-20 A
	72 mΩ @ -4.5 V	

P-Channel MOSFET



WDFN8
(μ8FL)
CASE 511AB

MARKING DIAGRAM



5116 = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTTFS5116PLTAG	WDFN8 (Pb-Free)	1500/Tape & Reel
NTTFS5116PLTWG	WDFN8 (Pb-Free)	5000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTTFS5116PL

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			69.7		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = -60\text{ V}$	$T_J = 25^\circ\text{C}$		-1.0	μA
			$T_J = 125^\circ\text{C}$		-100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\text{ }\mu\text{A}$	-1		-3	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			-6.2		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -6\text{ A}$		37	52	m Ω
		$V_{GS} = -4.5\text{ V}, I_D = -4.4\text{ A}$		51	72	
Forward Transconductance	g_{FS}	$V_{DS} = -15\text{ V}, I_D = -6\text{ A}$		11		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = -30\text{ V}$		1258		pF
Output Capacitance	C_{oss}			127		
Reverse Transfer Capacitance	C_{rss}			84		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -10\text{ V}, V_{DS} = -48\text{ V}, I_D = -5\text{ A}$		25		nC
		$V_{GS} = -4.5\text{ V}, V_{DS} = -48\text{ V}, I_D = -5\text{ A}$		14		
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -48\text{ V}, I_D = -5\text{ A}$		1		nC
Gate-to-Source Charge	Q_{GS}			4		
Gate-to-Drain Charge	Q_{GD}			7		
Plateau Voltage	V_{GP}			3.1		
Gate Resistance	R_G			5.3		Ω

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -48\text{ V}, I_D = -5\text{ A}, R_G = 6\text{ }\Omega$		15		ns
Rise Time	t_r			58		
Turn-Off Delay Time	$t_{d(off)}$			30		
Fall Time	t_f			37		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = -5\text{ A}$	$T_J = 25^\circ\text{C}$		-0.79	-1.2	V
			$T_J = 125^\circ\text{C}$		-0.64		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = -100\text{ A}/\mu\text{s}, I_S = -5\text{ A}$		20			ns
Charge Time	t_a			15			
Discharge Time	t_b			5			
Reverse Recovery Charge	Q_{RR}			19			nC

2. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

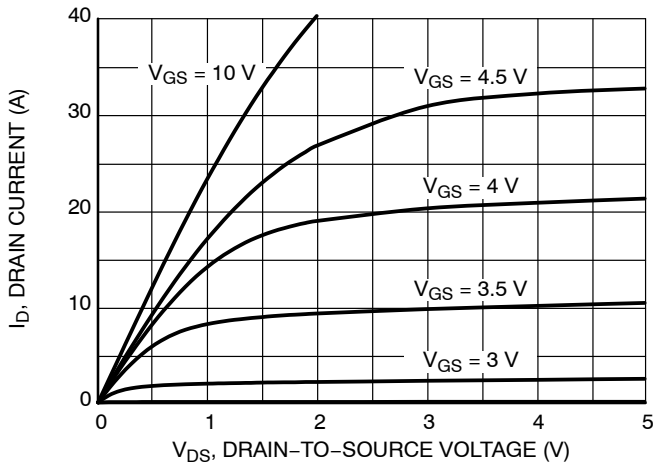


Figure 1. On-Region Characteristics

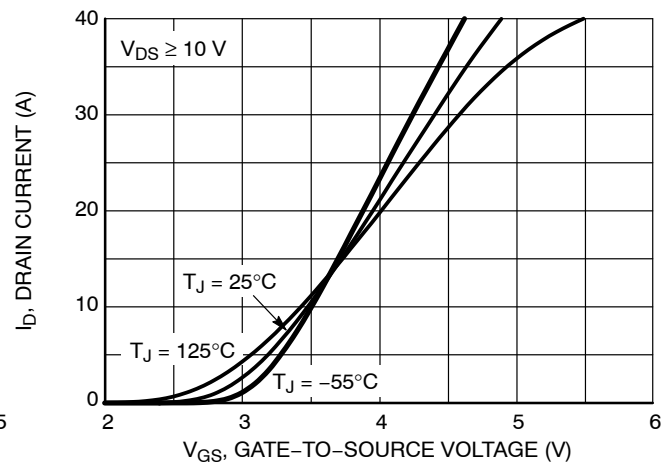


Figure 2. Transfer Characteristics

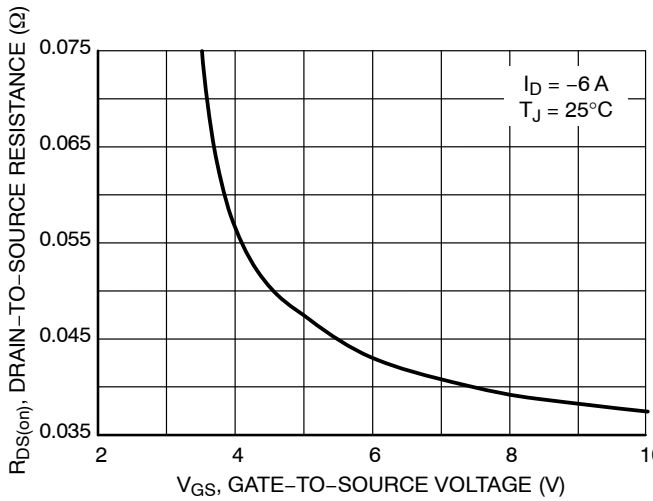


Figure 3. On-Resistance vs. Gate-to-Source Voltage

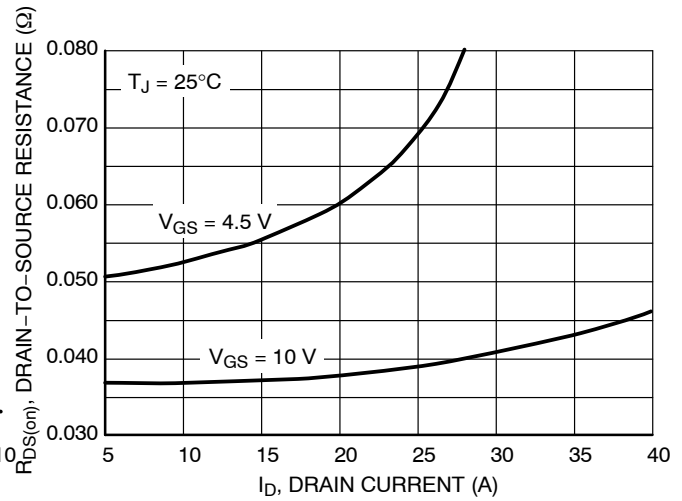


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

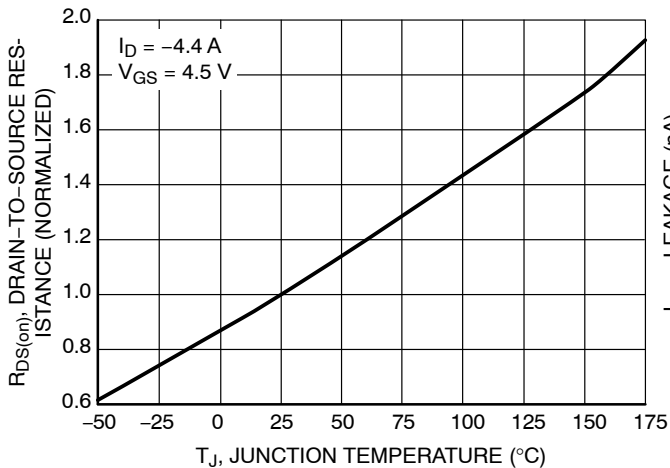


Figure 5. On-Resistance Variation with Temperature

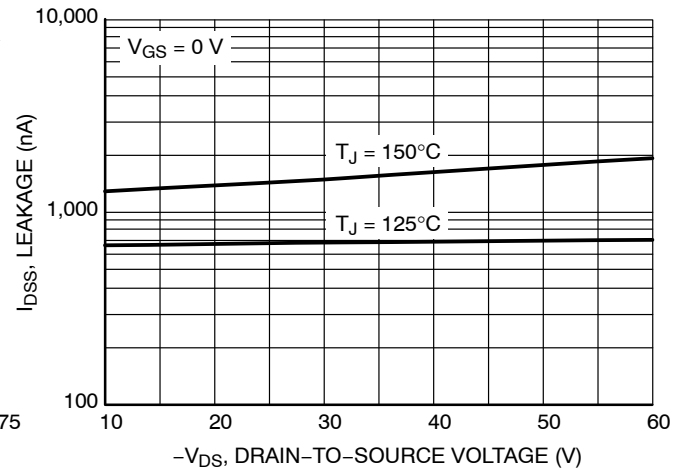


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

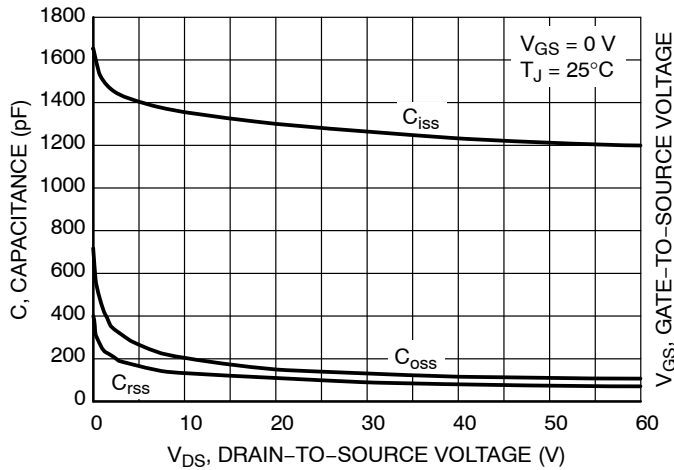


Figure 7. Capacitance Variation

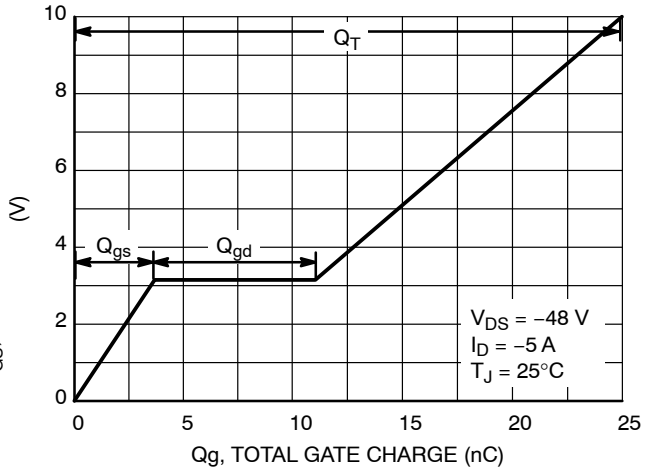


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

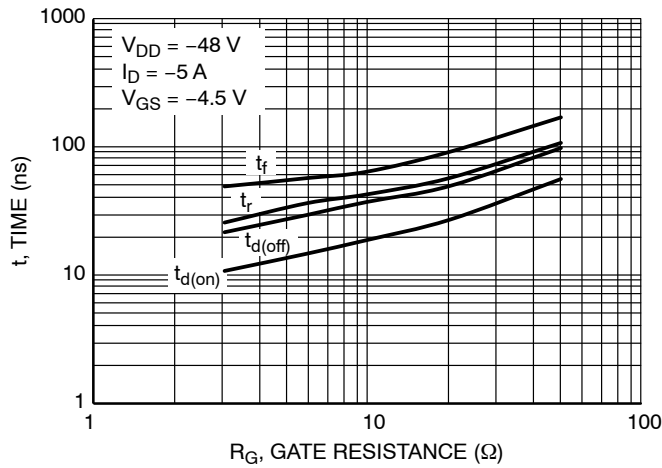


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

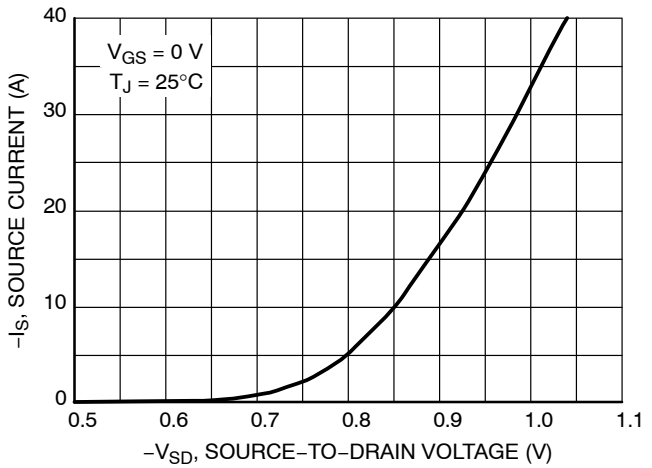


Figure 10. Diode Forward Voltage vs. Current

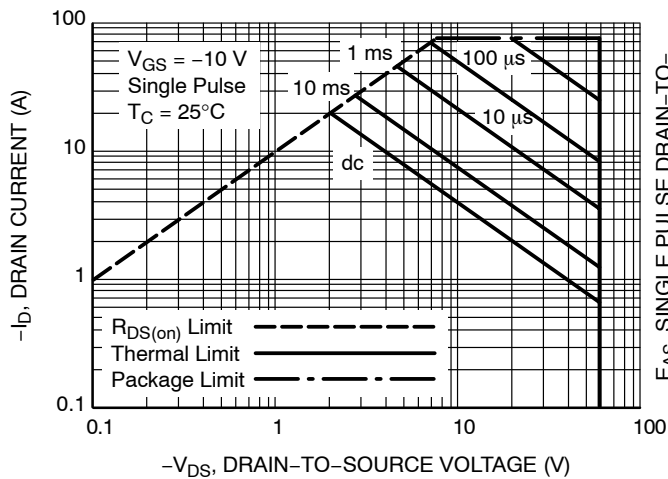


Figure 11. Maximum Rated Forward Biased Safe Operating Area

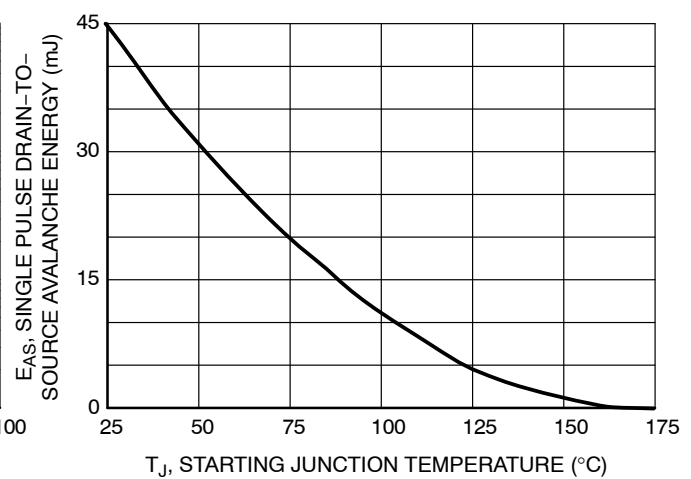


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

NTTFS5116PL

TYPICAL CHARACTERISTICS

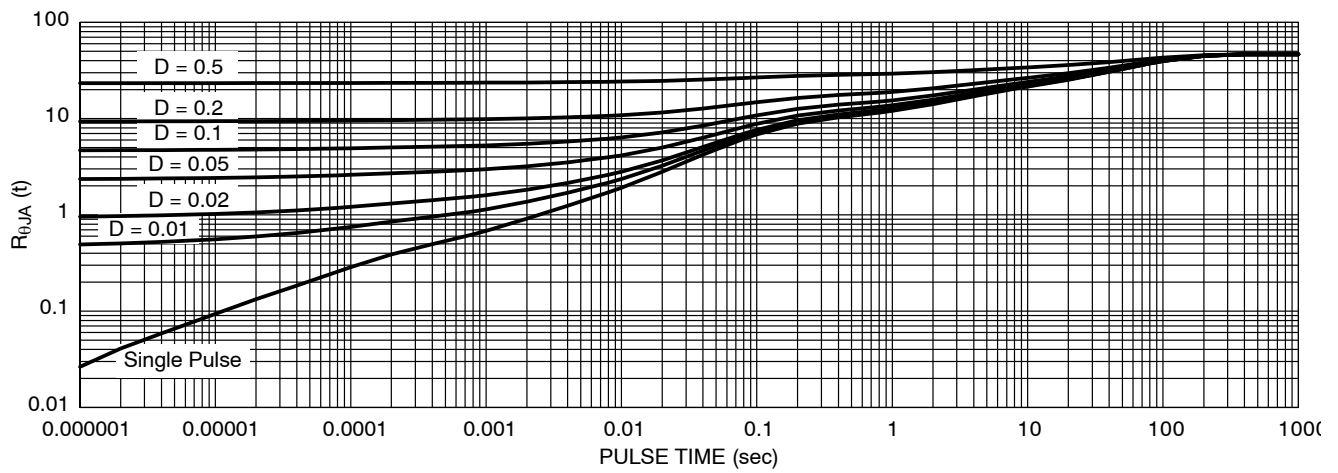


Figure 13. Thermal Response

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

WDFN8 3.3x3.3, 0.65P
CASE 511AB
ISSUE D

DATE 23 APR 2012



GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D	3.30 BSC			0.130 BSC		
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E	3.30 BSC			0.130 BSC		
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
e	0.65 BSC			0.026 BSC		
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.65	0.80	0.95	0.026	0.032	0.037
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0 °	---	12 °	0 °	---	12 °

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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