## Overview

The Ezairo 7100 series of open-programmable DSP-based systems is designed to meet the high performance and stringent power consumption requirements of advanced hearing aids and hearing implant devices.

With five times more processing power, the exceptionally power-efficient Ezairo 7100 System-on-Chip (SoC) provides built-in flexibility to support evolving algorithm, wireless and system-level needs.

The high-precision quad-core architecture is the industry's most integrated, flexible and power efficient single chip solution. When combined with non-volatile memory and wireless transceivers, it forms a complete hardware platform.

The new series is ideally suited for manufacturers wishing to develop their own novel algorithms or deploy customized algorithm suites from one of our solution partners.
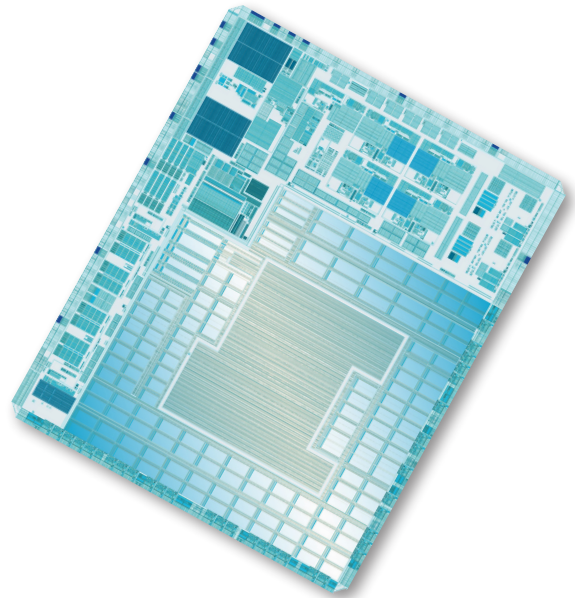
Key Features

High Performance
Five times more processing power than previous Ezairo systems at the same current consumption. A maximum clock speed of 15.36 MHz and clock throttling capabilities extend the computing capability.

Ultra-low Power Consumption
Industry-leading power consumption of less than 0.7 mA @ 10.24 MHz helps system designers achieve the most challenging power consumption targets in high-end devices.

Programmable Flexibility
The open-programmable architecture can be customized to the specific signal processing needs of manufacturers. Algorithms and features can be modified or completely new concepts implemented.

Wireless Control
The integrated wireless controller supports efficient data transfer to and from wireless transceivers. Compatible with various wireless technologies (NFMI, RF) including multi-radio systems.
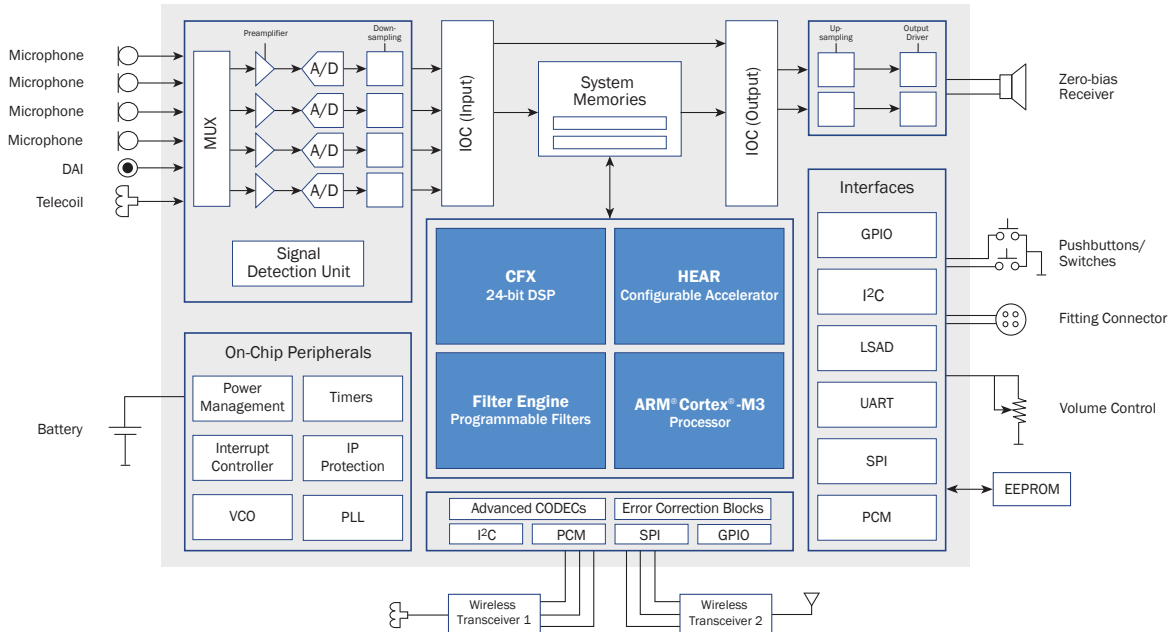
Ultra-high Audio Fidelity
85 dB system dynamic range, input dynamic range up to 110 dB, along with low system noise help to preserve detailed sound.

Ultra-low Delay
Programmable Filter Engine supports an ultra-low delay audio path of 0.044 ms (44 μs) for superior performance of features such as occlusion management.

Architecture Diagram

Additional Features

Quad-core Processing
- 24-bit open programmable CFX DSP core
- HEAR configurable accelerator
- ARM Cortex-M3 processor
- Programmable Filter Engine
- Selectable system clock speeds up to 15.36 MHz
- Clock throttling capability

Audio Performance
- 85 dB system dynamic range
- Input dynamic range extendable to 110 dB
- Group delay using Filter Engine low-delay path: 44 µs
- High power audio output option (up to 139 dB SPL)

Wireless Subsystem
- Fully programmable
- Hardwired CODECs (G.722, CVSD)
- Error correction support (Reed-Solomon, Hamming)
- Dedicated wireless interfaces

Interfaces
- 6 parallel inputs for microphones, telecoil and direct audio
- Signal detection unit for all inputs
- 2 digital direct drive outputs for zero-bias receivers
- Configurable interfaces: 2 PCM, 2 I^2C, 2 SPI, UART and multiple GPIOs
- Configurable LSAD

Other Features
- Supports higher density non-volatile memory
- Integrated power management ensures proper operation under all battery conditions
- Advanced encryption to protect proprietary algorithm intellectual property
- Interface hardware and IDE available to support product development activities

Packaging
- Ezairo 7100 bumped die
- Ezairo 7110 hybrid format (includes Ezairo 7100 die and a 2 Mb EEPROM)

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