Digital hearing: An embedded concept

When it comes to developing a silicon strategy, there are few applications that pose a more daunting challenge than modern hearing aids. Similar to portable consumer-oriented devices such as smartphones, there is a constant drive to enhance power efficiency and performance, while reducing system size. Christophe Waechchi, Product Manager at ON Semiconductor, looks at the key considerations for implementing integrated circuitry into a hearing aid hardware platform.

Innovation in hearing aid design is now lowering the visual impact of these devices, with new models emerging which are situated deeper into the ear canal. Behind-the-ear (BTE) devices are gradually being supplanted by completely-in-the-canal (CIC) and invisible-in-the-canal (ITC) products. This trend requires further system miniaturisation.

The digital signal processing (DSP) architecture employed is clearly critical to the hearing aid design’s effectiveness. Device manufacturers can select from a number of architectural options. At one extreme of the spectrum is the closed, fixed function approach and at the other lies the generic, open-programmable approach, with architectures that have differing degrees of both situated in-between.

There are advantages and disadvantages of both open-programmable and closed architectures. With a closed architecture, the signal processing scheme is hardwired into the DSP chip, with the benefit that power budget and PCB utilisation are both relatively low, but system flexibility is lost.

The more ‘open’ an architecture is, the greater the software flexibility a manufacturer has to play with. With open-programmable architectures, signal processing algorithms can be modified. The architecture can support a raft of signal processing possibilities (sound, images and sensor data) across many applications. This heightened flexibility will lead to increased size and greater power consumption, making open-programmable architectures far from ideal for modern hearing aids.

A semi-programmable architecture can to some extent nullify the inherent disadvantages of a closed approach by enabling some programmability. Key signal processing functions are hardwired in logic blocks. These are complemented by a programmable DSP, which enables implementation of additional signal processing capabilities in software. While some flexibility is gained, semi-programmable architectures still have to forfeit a modicum of power efficiency.

Another approach is an application-specific, open-programmable architecture. These are optimised to meet the signal processing needs of a very specific application combined with the software flexibility open architectures afford. Though not as power efficient as closed architectures, most of the efficiency limitations can be overcome through well-organised chip design and a suitable process technology.

Once the DSP architecture has been decided upon, the next issue to address is how to partition the circuitry. Design engineers must deliberate over which components functional blocks should be combined and integrated into a single chip, co-packaged together or remain discrete. Flexibility is of prime importance when making partitioning decisions - if blocks are integrated on a solitary system-on-a-chip (SoC) die then valuable space will be saved. However, the possibility of altering any of the functional blocks disappears and the entire chip must be re-spun if changes are necessary, which can be both time consuming and expensive. For instance, it is hard to predict which wireless standards are going to emerge or when. If, therefore, the wireless communication functionality is integrated into the SoC, the system will be locked into a specific wireless standard for as long as that SoC is utilised. Some blocks have functionality that is mature and stable – they are hence highly suited to integration. Others, such as wireless communication, may change depending on which technology is adopted.

When this is the case a separate chip is advised.

For hearing aid hardware platforms, the increasing complexity of signal processing algorithms is driving the need for greater computing capability. Transitioning to smaller process nodes will allow this and also help satisfy ever-growing power consumption and package format demands. This must be weighed up against the fact that design and manufacturing complexity increases significantly when process geometries are used and the greater capital costs involved.

Hearing aid platforms are now often based on multiple processor cores, as this will enable boosted performance and reduced power consumption. Standard cores offering programmable flexibility have reached a stage where they can be used in tandem with specialised cores for certain processing tasks and thus optimise power consumption. Adoption of standard cores not only shortens development time, it also reduces the potential technical risks. By following a standard core approach, design resources can be allocated to other areas where differentiation may be sought and value added.

On Semiconductor
www.onsemi.com
01753 626 718 Enter 208