Driving Efficient Power Solutions from Standby to Active Mode
(from line to load)

Dhaval Dalal
Technical Marketing Director

Christophe Basso
Applications Manager
Agenda

• Power train overview – new complexities
• Challenges (PSMA roadmap, energy standards)
• Solutions for standby power savings
• Solutions for active mode savings
• Conclusions/Questions
The Power Train – Line to Load

- Trend towards multiple power processing stages
- New complexity demands system level solutions
Challenges – A PSMA Perspective

Optimal Topologies
Better Components
ICs
Power Semiconductors

SOURCE:
POWER SOURCES MANUFACTURERS ASSOC.
Regulatory Trends

• Standby power requirements in effect in various parts of the world
  – IEA, Energy-star, Blue Angel, CECP
  – Requirements depend on type of equipment
  – Input power levels are reducing
  – Only 25% of energy consumed in standby

• Active mode efficiency is the next frontier
  – Test methodology defined (CEC)
  – EPA/CEC sponsored contest
  – Some OEMs driving their own standards
Lowering *standby* power

Skip-cycle or Frequency foldback?

Christophe Basso, application manager
ON Semiconductor, Toulouse, France
What is *standby* power…?

- A supply is left connected to the line without load, the power drawn from the mains shall be minimum.
- Battery chargers, AC/DC wall adapters etc.
- A system goes into sleep-mode while still having some intelligent activity.
- TV sets (LED is on, μP waiting for remote control), VCRs

EC recommendations:

<table>
<thead>
<tr>
<th>Rated Input Power</th>
<th>No-load power consumption</th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Phase 1</td>
<td>Phase 2</td>
<td>Phase 3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.1.2001</td>
<td>1.1.2003</td>
<td>1.1.2005</td>
<td></td>
</tr>
<tr>
<td>≥ 0.3 W and &lt; 15 W</td>
<td>1.0 W</td>
<td>0.75 W</td>
<td>0.30 W</td>
<td></td>
</tr>
<tr>
<td>≥ 15 W and &lt; 50 W</td>
<td>1.0 W</td>
<td>0.75 W</td>
<td>0.50 W</td>
<td></td>
</tr>
<tr>
<td>≥ 50 W and &lt; 75 W</td>
<td>1.0 W</td>
<td>0.75 W</td>
<td>0.75 W</td>
<td></td>
</tr>
</tbody>
</table>
Where are the *losses* coming from?

1. Capacitive losses: \( \frac{1}{2} \cdot C \cdot V^2 \cdot f_{sw} \)
2. Biasing network
3. Controller current
4. Gate charge: \( Qg \cdot f_{sw} \)
5. Start-up network

No-load losses can easily go up to 1W!
Standard connection

Half-wave connection
Only 27% in gain 😞
Suppose we want to start-up in 250ms with:
CVcc = 22µF, UVLO = 12V
Istartup total (IC + capacitor) = 50µA
Universal mains input, 100 – 370VDC
A 250ms time sequence imposes a current of: \( i = \frac{12 \cdot 22\mu A}{250m} = 1mA \)

- **Standard connection**: \( R = \frac{100-12}{1m} = 88k\Omega \)
  \[ P@370VDC = 1.55W! \]
- **Half-wave connection**: 28kΩ
  \[ P@370VDC = 1.22W! \]
- **High-voltage technology**:
  \( I_{source} = 4mA \), then startup time equals 66ms
  \[ P@370VDC = 13mW! \]
  \[ P = 35\mu VDC \]
Switching frequency: *THE* actor in the low-standby tragedy…

« Why not further reducing the duty-cycle? »

- Gate-charge losses are almost independent of duty-cycle
- MOSFET drain-node capacitive losses are not eliminated
- Controller internal activity is still important (all blocks active)
- Minimum duty-cycle is also limited to LEB + prop. delay

Psst! Why don’t you decrease the switching frequency?
The *first* approach: hysteretic regulation

Slicing the switching pattern...

- introduced 20 years ago with the MC33063…
- also called…ripple regulator!
- generates a lot of noise
- Excellent natural standby!
**Novel** approach: mixing *fixed frequency* and *skip cycle*…

Standard CM controller

CM controller + skip comparator

NCP120X
NCP120X for noise free operation in standby...

Max peak current

Power goes down

Skip cycle current limit

Cycle skipping in standby
Low peak current!

NCP120X
A practical solution using NCP1203/1217...

A 84mW@230VAC standby power at no-load was measured!
The controller self-supply: a designer’s nightmare

- burst frequency is low
- pulse packet is narrow
- can’t afford to lose energy…

Too lossy!

- increase the aux. turn ratio → degrades overload protection
- decrease the aux. turn ratio → can’t self-supply the IC
Fault detection independent of Vcc.

Vcc aux. does not collapse in short-circuit!

Decision point is independent of Vcc!

NCP1230
Frequency reduction via Quasi-Resonance

“Switching ON at the *minimum* drain-source voltage...”

It brings:

- Soft switching ⇒ smaller MOSFET...
- ZVS ⇒ reduced Miller effect on Qg
- Less EMI noise ⇒ RF friendly
- Discontinuous conduction only ⇒ easy to stabilize
- Core reset offers better short-circuit performance
- With good transformers ⇒ no RCD clamp!
What are **Hard** and **Soft** switching SMPS??

Vds is maximum

Spike is very noisy

**EMI** is so bad...

Soft rising

ZVS

No spike!

So smooth for EMI!
Core reset detection ensures $BCM^*$ operation

Switching period moves w. line and load variations:

$$T_{sw} = I_p \cdot L_p \cdot \left[ \frac{1}{V_{indc}} + \frac{1}{\frac{N_p}{N_s} \cdot (V_{out} + V_f)} \right]$$

Bulk ripple introduces natural EMI jittering!!
Free-running operation **needs** a frequency clamp!

![Diagram showing free running frequency versus output power](image)

- **Free running frequency versus output power**
- Traditional free-running systems
- Transition BCM to VFM*
- User adjustable limit
- Down to zero duty-cycle

* VFM = Variable Frequency Mode

[NCP1205](www.onsemi.com)
The *Feedback* voltage determines the operating mode

- Pnominal
- P goes down
- Standby
- Toff expands

Frequency foldback takes place at 1/3rd of the max. Ip

No noise!

NCP1205
A 30W universal mains demonstration board

Pin @ no-load = 108mW@240VAC!!
Drain-source waveforms at different power levels

P1 = 30W @ Vin = 200VAC
P1 > P2 > P3 > P4

Multiple wave jumping

NCP1205
Frequency reduction via $T_{off}$ expansion

- $V_{driver}$
- $I_{peak}$
- $T_{off}$ expands
- $I_p = constant$
- $I_p$ reduction to lower audible noise
- $I_p = constant$
Frequency reduction via $T_{off}$ expansion

- Fixes min/max. Fsw
- Fix max. Ip

**Diagram:**
- NCP1215
- Line
- N

**Components:**
- FB NC
- CT NC
- CS Vcc
- GND Gate

**Note:**
- Line connections and components are shown in detail.
Toff expansion brings extremely low standby…
Power Factor Correction – observing the FB signal

Max Ip

Skip

Delay truncated

regulation

Skip + 20%

Standby entered here

Standby left here

Standby confirmed

No delay

NCP1230
Power Factor Correction – **standby** improvement

Shut-down your PFC in standby-mode and pass the 100mW barrier…
**Power Factor Correction – auto-shutdown controller**

- NCP1600 observes the FB signal:
  - a) enters skip mode and maintains Vout
  - b) shuts itself off until normal mode
- implements follow-boost mode
- borderline operation with Fsw clamp
- works with any PWM controllers!

NCP1600
Power Factor Correction – first fixed frequency DCM!

\[ d_{\text{cycle}} = \frac{t_{\text{cycle}}}{T_{\text{sw}}} = \frac{t_{\text{on}} + t_{\text{dem}}}{T_{\text{sw}}} \]

\[ \langle I_{\text{coil}} \rangle_{T_{\text{sw}}} = \frac{V_{\text{in}}}{2L} \left( t_{\text{on}} \cdot d_{\text{cycle}} \right) \]

Keeping this term constant
\[ \langle I_{\text{coil}} \rangle \text{ follows } V_{\text{in}} \ldots \]

**NCP1601** principle of operation (patented by ON)
Power Factor Correction – ease of implementation

NCP1601 a truly simple application schematic!!

Negative Sensing
Rsense down to 100mΩ
Secured start-up
How to measure low standby power?

• using a DC supply (e.g. 325V) and measuring incoming I and V
  → the best is to use a good old needle amp-meter which mechanically integrates bursts…
  → the difference between DC results and AC results is around 10-15% more for AC.
• use a wattmeter (highest current sens.) toggled in accumulation mode and integrate W-hours.
Summary

• **Skip cycle** offers a simple mean to improve standby:
  - cheapest method to slice the switching pattern
  - combined with a startup source, it gives good results
  - It generates some output ripple
  - If the skip occurs at high peak, acoustical noise can be heard

• **Free-running Frequency foldback** requires a more complex controller:
  - implement ZVS operation
  - offers soft transition between normal operation and light load
  - generates lower ripple level compared to skip
  - The controllers gains in complexity
  - Discrete valley jumps can make noise

• **Quasi-fixed Ton, Toff expansion** further simplifies the control section:
  - ease of implementation, both on silicon and final circuit
  - Audio range operation requires peak compression
Improving PFC Efficiency

- CCM for higher power, CRM/DCM for lower power
- Topology improvements drive component changes

- Better \( \text{trr} \) for CCM
- Lower VF for CRM/DCM

\( \text{Vo} \propto \text{Vin} \)
- Smaller FET and L
- Lower PFC losses
- Wider Vin for SMPS

- Control maximum power
- Lower \( R_{ds-on} \)
- Lower Ton losses (CCM)
Follower Boost Waveform
(MC33260, NCP1600)

Traditional output

Vo (Follower Boost)

Vac

Load
MC33260 – Apps Diagram

Vo: 200-400 V => •33% Reduction in Conduction Losses
•43% Reduction in Inductor Size
NCP1650 - CCM PFC Control

Typical Applications
- power up to 5 kW
- Server Power Converters
- Front end for Distributed Power Systems
- Desktop Power Systems

Features
- Average Current Mode PWM
- Fixed Frequency Operation
- Continuous or discontinuous mode operation
- Shutdown Function
- Fast Line/Load Transient Compensation
  - Over Voltage Protection
  - Accurate Power Limit
  - Current Limit
  - Brownout Protection

Benefits
- Unity Power Factor
- Predictable Filtering Requirements
- User Flexibility
- Helps Meet Standby Regulations
- Better Performance to Line or Load Changes
- High Reliability
- Allows use of smaller power components
- Avoids excessive heating
NCP1650 - Competition

<table>
<thead>
<tr>
<th>Power Limit Specs</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>NCP1650</strong> Power Multiplier Gain (-40 to 125 deg C)</td>
<td>11.8</td>
<td>12.8</td>
<td>13.3</td>
<td>1/V</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>108.5</td>
<td>112.7</td>
<td>%</td>
</tr>
<tr>
<td><strong>UCCxxxxx</strong> Power Limit (-40 to 85 deg C) (based on V^2 scheme)</td>
<td>375</td>
<td>420</td>
<td>485</td>
<td>µ W</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>112</td>
<td>129.3</td>
<td>%</td>
</tr>
</tbody>
</table>

- NCP1650 cuts the excess power requirement by more than 50% (from 29.3% to 12.7%)
  - These numbers come directly from spec tables
- Other PFC controllers have NO power limiting or offer less accuracy compared to the above
Improving SMPS Efficiency

- Topology Upgrade (Flyback -> Forward -> Bridge)
- Soft-switching extends range (QR, Active clamp etc)
- Component level improvements (FET, sync rec etc)
Active Clamp Topology

- Off-line Active Clamp Forward Converters
  - Clamp Circuit (Switch and cap) resets the core
  - This topology allows soft-switching
  - Synchronous Rectification available naturally
Single Stage Option

- Elimination of a power processing stage
- Requires single switch, single magnetic, single rectifier & single cap
- Low frequency output ripple can be high
- Ideal for mid-high (12-150) voltage output systems
On-Board Power Conversion

- Need efficient in-rush protection
- Isolated dc-dc module size shrink drivers
  - Topology
  - Packaging
  - Integration
  - Components
- Architecture shift to IBCs
- Evolution of point of load solutions
Hot Swap Controller and FET

Controller

This approach is complex
Power resistor increases cost and losses

Sense Resistor

FET

Current Solution
NIS5101 - SMART HotPlug™

Fully Integrated controller and FET

- Linear Current Limit
- Thermal Protection
- SOA Operation Guaranteed
- 40 mΩ, 110 Volt FET
- Extremely Simple to Design
- Cost Effective
NCP1560 Demo Board

Basic Forward Converter:

- Vin: 35-75 V (Telecom Input)
- Vout: 3.3 V @ 30 A (100 W)
- Dimensions: 2.5” x 3.0” x 0.4”

High Efficiency Forward Converter Implemented Using NCP1560:

![Diagram of Basic Forward Converter and High Efficiency Forward Converter Implemented Using NCP1560]
NCP1030 – Low power regulator

NCP103x replaces

NCP1030
NCP1030 Demonstration Board

- An isolated bias supply for a telecom system was built using the NCP1030. The supply delivers 2 W at 12 V.
- The supply is ideal for biasing a secondary side controller.
- A discontinuous flyback topology is used.
- Application Note AND8119/D describes the bias supply design.
- Please contact your sales representative for availability of demonstration boards.
Conclusions

- Opportunities for efficiency improvement at every stage of the power train
- Newer architectures and components optimized for them will help achieve the goals cost effectively