MC34063A, MC33063A, SC34063A, SC33063A, NCV33063A

Inverting Regulator - Buck, Boost, Switching

1.5 A

The MC34063A Series is a monolithic control circuit containing the primary functions required for DC–to–DC converters. These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in Step–Down and Step–Up and Voltage–Inverting applications with a minimum number of external components. Refer to Application Notes AN920A/D and AN954/D for additional design information.

Features
- Operation from 3.0 V to 40 V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.5 A
- Output Voltage Adjustable
- Frequency Operation to 100 kHz
- Precision 2% Reference
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

This device contains 79 active transistors.

Figure 1. Representative Schematic Diagram
# MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Voltage</td>
<td>$V_{CC}$</td>
<td>40</td>
<td>Vdc</td>
</tr>
<tr>
<td>Comparator Input Voltage Range</td>
<td>$V_{IR}$</td>
<td>−0.3 to +40</td>
<td>Vdc</td>
</tr>
<tr>
<td>Switch Collector Voltage</td>
<td>$V_{C(switch)}$</td>
<td>40</td>
<td>Vdc</td>
</tr>
<tr>
<td>Switch Emitter Voltage (V$P_{1}$ = 40 V)</td>
<td>$V_{E(switch)}$</td>
<td>40</td>
<td>Vdc</td>
</tr>
<tr>
<td>Switch Collector to Emitter Voltage</td>
<td>$V_{CE(switch)}$</td>
<td>40</td>
<td>Vdc</td>
</tr>
<tr>
<td>Driver Collector Voltage</td>
<td>$V_{C(driver)}$</td>
<td>40</td>
<td>Vdc</td>
</tr>
<tr>
<td>Driver Collector Current (Note 1)</td>
<td>$I_{C(driver)}$</td>
<td>100</td>
<td>mA</td>
</tr>
<tr>
<td>Switch Current</td>
<td>$I_{SW}$</td>
<td>1.5</td>
<td>A</td>
</tr>
</tbody>
</table>

## Power Dissipation and Thermal Characteristics

Plastic Package, P, P1 Suffix

- $T_A = 25\,^\circ C$  
  - $P_D$ 1.25 W  
  - Thermal Resistance $R_{IJA}$ 115 °C/W  

SOIC Package, D Suffix

- $T_A = 25\,^\circ C$  
  - $P_D$ 625 mW  
  - Thermal Resistance $R_{IJA}$ 160 °C/W  

DFN Package

- $T_A = 25\,^\circ C$  
  - $P_D$ 1.25 mW  
  - Thermal Resistance $R_{IJA}$ 80 °C/W  

## Operating Junction Temperature

$T_J$ +150 °C

## Operating Ambient Temperature Range

$T_A$ 0 to +70 °C

## Storage Temperature Range

$T_{stg}$ −65 to +150 °C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum package power dissipation limits must be observed.
2. This device series contains ESD protection and exceeds the following tests: Human Body Model 4000 V per MIL−STD−883, Method 3015. Machine Model Method 400 V.
3. NCV prefix is for automotive and other applications requiring site and change control.
## ELECTRICAL CHARACTERISTICS

(VCC = 5.0 V, TA = Tlow to Thigh [Note 4], unless otherwise specified.)

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>OSCILLATOR</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency (VPin 5 = 0 V, CT = 1.0 nF, TA = 25°C)</td>
<td>fosc</td>
<td>24</td>
<td>33</td>
<td>42</td>
<td>kHz</td>
</tr>
<tr>
<td>Charge Current (VCC = 5.0 V to 40 V, TA = 25°C)</td>
<td>Ichg</td>
<td>24</td>
<td>35</td>
<td>42</td>
<td>μA</td>
</tr>
<tr>
<td>Discharge Current (VCC = 5.0 V to 40 V, TA = 25°C)</td>
<td>Idischg</td>
<td>140</td>
<td>220</td>
<td>260</td>
<td>μA</td>
</tr>
<tr>
<td>Discharge to Charge Current Ratio (Pin 7 to VCC, TA = 25°C)</td>
<td>Idischg/Ichg</td>
<td>5.2</td>
<td>6.5</td>
<td>7.5</td>
<td>–</td>
</tr>
<tr>
<td>Current Limit Sense Voltage (Ichg = Idischg, TA = 25°C)</td>
<td>Vipk(sense)</td>
<td>250</td>
<td>300</td>
<td>350</td>
<td>mV</td>
</tr>
<tr>
<td><strong>OUTPUT SWITCH</strong> (Note 5)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Saturation Voltage, Darlington Connection (Isw = 1.0 A, Pins 1, 8 connected)</td>
<td>VCE(sat)</td>
<td>–</td>
<td>1.0</td>
<td>1.3</td>
<td>V</td>
</tr>
<tr>
<td>Saturation Voltage (Note 6) (Isw = 1.0 A, RPin 8 = 82Ω to VCC, Forced β = 20)</td>
<td>VCE(sat)</td>
<td>–</td>
<td>0.45</td>
<td>0.7</td>
<td>V</td>
</tr>
<tr>
<td>DC Current Gain (Isw = 1.0 A, VCE = 5.0 V, TA = 25°C)</td>
<td>hFE</td>
<td>50</td>
<td>75</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Collector Off–State Current (VCE = 40 V)</td>
<td>Ic(off)</td>
<td>–</td>
<td>0.01</td>
<td>100</td>
<td>μA</td>
</tr>
<tr>
<td><strong>COMPARATOR</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Threshold Voltage</td>
<td>Vth</td>
<td>1.225</td>
<td>1.25</td>
<td>1.275</td>
<td>V</td>
</tr>
<tr>
<td>TA = 25°C</td>
<td></td>
<td>1.21</td>
<td>–</td>
<td>1.29</td>
<td></td>
</tr>
<tr>
<td>TA = Tlow to Thigh</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Threshold Voltage Line Regulation (VCC = 3.0 V to 40 V)</td>
<td>Regline</td>
<td>–</td>
<td>1.4</td>
<td>5.0</td>
<td>mV</td>
</tr>
<tr>
<td>MC33063, MC34063</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MC33063V, NCV33063</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Bias Current (Vin = 0 V)</td>
<td>IIB</td>
<td>–</td>
<td>–20</td>
<td>–400</td>
<td>nA</td>
</tr>
<tr>
<td><strong>TOTAL DEVICE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Current (VCC = 5.0 V to 40 V, CT = 1.0 nF, Pin 7 = VCC, VPin 5 ≥ VIB, Pin 2 = GND, remaining pins open)</td>
<td>ICC</td>
<td>–</td>
<td>–</td>
<td>4.0</td>
<td>mA</td>
</tr>
</tbody>
</table>

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Tlow = 0°C for MC34063, SC34063; –40°C for MC33063, SC33063, MC33063V, NCV33063

5. Thigh = +70°C for MC34063, SC34063; +85°C for MC33063, SC33063; +125°C for MC33063V, NCV33063

6. If the output switch is driven into hard saturation (non–Darlington configuration) at low switch currents (≤ 300 mA) and high driver currents (≥ 30 mA), it may take up to 2.0 ms for it to come out of saturation. This condition will shorten the off time at frequencies ≥ 30 kHz, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non–Darlington configuration is used, the following output drive condition is recommended:

\[
\text{Forced } \beta \text{ of output switch: } \frac{I_C \text{ output}}{I_C \text{ driver} - 7.0 \text{ mA}} \geq 10
\]

* The 100 Ω resistor in the emitter of the driver device requires about 7.0 mA before the output switch conducts.
MC34063A, MC33063A, SC34063A, SC33063A, NCV33063A

**Figure 3. Oscillator Frequency**

![Graph of oscillator frequency](image)

- **VCC = 5.0 V, Pin 7 = VCC, Pin 5 = GND, TA = 25°C**

**Figure 4. Timing Capacitor Waveform**

![Graph of timing capacitor waveform](image)

- **Vcc = 5V, C\text{t} = 1.0 nF, TA = 25°C**
  - Pins 1, 5, 8 = open, Pin 7 = Vcc, Pin 2 = GND

**Figure 5. Emitter Follower Configuration Output**

- **Saturation Voltage versus Emitter Current**

![Graph of saturation voltage](image)

- **VCC = 5.0 V, Pins 1, 7, 8 = VCC, Pins 3, 5 = GND, TA = 25°C**
  - (See Note 7)

**Figure 6. Common Emitter Configuration Output**

- **Switch Saturation Voltage versus Collector Current**

![Graph of switch saturation voltage](image)

- **VCC = 5.0 V, Pin 7 = VCC, Pins 3, 5 = GND, TA = 25°C**
  - (See Note 7)

**Figure 7. Current Limit Sense Voltage versus Temperature**

![Graph of current limit sense voltage](image)

- **VCC = 5.0 V, \( I_{chg} = I_{dischg} \)**

**Figure 8. Standby Supply Current versus Supply Voltage**

![Graph of standby supply current](image)

- **C\text{t} = 1.0 nF, Pin 7 = VCC, Pin 2 = GND**

7. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

[www.onsemi.com](http://www.onsemi.com)
<table>
<thead>
<tr>
<th>Test</th>
<th>Conditions</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line Regulation</td>
<td>$V_{in} = 8.0 \text{ V to } 16 \text{ V}, I_O = 175 \text{ mA}$</td>
<td>$30 \text{ mV} = \pm 0.05%$</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>$V_{in} = 12 \text{ V}, I_O = 75 \text{ mA to } 175 \text{ mA}$</td>
<td>$10 \text{ mV} = \pm 0.017%$</td>
</tr>
<tr>
<td>Output Ripple</td>
<td>$V_{in} = 12 \text{ V}, I_O = 175 \text{ mA}$</td>
<td>$400 \text{ mVpp}$</td>
</tr>
<tr>
<td>Efficiency</td>
<td>$V_{in} = 12 \text{ V}, I_O = 175 \text{ mA}$</td>
<td>$87.7%$</td>
</tr>
<tr>
<td>Output Ripple With Optional Filter</td>
<td>$V_{in} = 12 \text{ V}, I_O = 175 \text{ mA}$</td>
<td>$40 \text{ mVpp}$</td>
</tr>
</tbody>
</table>

**Figure 9. Step-Up Converter**
8. If the output switch is driven into hard saturation (non–Darlington configuration) at low switch currents ($\leq 300$ mA) and high driver currents ($\geq 30$ mA), it may take up to $2.0 \mu s$ to come out of saturation. This condition will shorten the off time at frequencies $\geq 30$ kHz, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non–Darlington configuration is used, the following output drive condition is recommended.

Figure 10. External Current Boost Connections for $I_C$ Peak Greater than 1.5 A

9a. External NPN Switch

9b. External NPN Saturated Switch

(See Note 8)
Test | Conditions | Results
---|---|---
Line Regulation | $V_{in} = 15 \text{ V to } 25 \text{ V}, \ I_O = 500 \text{ mA}$ | $12 \text{ mV} = \pm 0.12\%$
Load Regulation | $V_{in} = 25 \text{ V}, \ I_O = 50 \text{ mA to } 500 \text{ mA}$ | $3.0 \text{ mV} = \pm 0.03\%$
Output Ripple | $V_{in} = 25 \text{ V}, \ I_O = 500 \text{ mA}$ | $120 \text{ mVpp}$
Short Circuit Current | $V_{in} = 25 \text{ V}, \ R_L = 0.1 \text{ } \Omega$ | $1.1 \text{ A}$
Efficiency | $V_{in} = 25 \text{ V}, \ I_O = 500 \text{ mA}$ | $83.7\%$
Output Ripple With Optional Filter | $V_{in} = 25 \text{ V}, \ I_O = 500 \text{ mA}$ | $40 \text{ mVpp}$

**Figure 11. Step–Down Converter**

**Figure 12. External Current Boost Connections for $I_C$ Peak Greater than 1.5 A**

11a. External NPN Switch 11b. External PNP Saturated Switch
Test | Conditions | Results
--- | --- | ---
Line Regulation | $V_{in} = 4.5 \text{ V to } 6.0 \text{ V}, I_O = 100 \text{ mA}$ | 3.0 mV = ±0.012%
Load Regulation | $V_{in} = 5.0 \text{ V}, I_O = 10 \text{ mA to } 100 \text{ mA}$ | 0.022 V = ±0.09%
Output Ripple | $V_{in} = 5.0 \text{ V}, I_O = 100 \text{ mA}$ | 500 mVpp
Short Circuit Current | $V_{in} = 5.0 \text{ V}, R_L = 0.1 \Omega$ | 910 mA
Efficiency | $V_{in} = 5.0 \text{ V}, I_O = 100 \text{ mA}$ | 62.2%
Output Ripple With Optional Filter | $V_{in} = 5.0 \text{ V}, I_O = 100 \text{ mA}$ | 70 mVpp

Figure 13. Voltage Inverting Converter

Figure 14. External Current Boost Connections for $I_C$ Peak Greater than 1.5 A

13a. External NPN Switch 13b. External PNP Saturated Switch
Figure 15. Printed Circuit Board and Component Layout
(Circuits of Figures 9, 11, 13)

INDUCTOR DATA

<table>
<thead>
<tr>
<th>Converter</th>
<th>Inductance ((\mu)H)</th>
<th>Turns/Wire</th>
</tr>
</thead>
<tbody>
<tr>
<td>Step–Up</td>
<td>170</td>
<td>38 Turns of #22 AWG</td>
</tr>
<tr>
<td>Step–Down</td>
<td>220</td>
<td>48 Turns of #22 AWG</td>
</tr>
<tr>
<td>Voltage–Inverting</td>
<td>88</td>
<td>28 Turns of #22 AWG</td>
</tr>
</tbody>
</table>

All inductors are wound on Magnetics Inc. 55117 toroidal core.
Figure 16. Printed Circuit Board for DFN Device
### Calculation

<table>
<thead>
<tr>
<th>Calculation</th>
<th>Step-Up</th>
<th>Step-Down</th>
<th>Voltage-Inverting</th>
</tr>
</thead>
</table>
| $t_{on}/t_{off}$ | \[
\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}
\] | \[
\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}
\] | \[
\frac{|V_{out}| + V_F}{V_{in} - V_{sat}}
\] |
| $(t_{on} + t_{off})$ | \[
\frac{1}{T}
\] | \[
\frac{1}{T}
\] | \[
\frac{1}{T}
\] |
| $t_{off}$ | \[
\frac{t_{on} + t_{off}}{t_{off} + 1}
\] | \[
\frac{t_{on} + t_{off}}{t_{off} + 1}
\] | \[
\frac{t_{on} + t_{off}}{t_{off} + 1}
\] |
| $t_{on}$ | \[
(t_{on} + t_{off}) - t_{off}
\] | \[
(t_{on} + t_{off}) - t_{off}
\] | \[
(t_{on} + t_{off}) - t_{off}
\] |
| $C_T$ | \[
4.0 \times 10^{-5} t_{on}
\] | \[
4.0 \times 10^{-5} t_{on}
\] | \[
4.0 \times 10^{-5} t_{off}
\] |
| $I_{pk(switch)}$ | \[
2I_{out(max)} \left(\frac{t_{on} + t_{off}}{t_{off} + 1}\right)
\] | \[
2I_{out(max)}
\] | \[
2I_{out(max)} \left(\frac{t_{on} + t_{off}}{t_{off} + 1}\right)
\] |
| $R_{sc}$ | \[
0.3/I_{pk(switch)}
\] | \[
0.3/I_{pk(switch)}
\] | \[
0.3/I_{pk(switch)}
\] |
| $L_{(min)}$ | \[
\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}}\right) t_{on(max)}
\] | \[
\left(\frac{V_{in(min)} - V_{sat} - V_{out}}{I_{pk(switch)}}\right) t_{on(max)}
\] | \[
\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}}\right) t_{on(max)}
\] |
| $C_O$ | \[
9 \frac{I_{out} t_{on}}{V_{ripple(pp)}}
\] | \[
\frac{I_{pk(switch)} t_{on} + t_{off}}{8V_{ripple(pp)}}
\] | \[
9 \frac{I_{out} t_{on}}{V_{ripple(pp)}}
\] |

$V_{sat}$ = Saturation voltage of the output switch.
$V_F$ = Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen:

- $V_{in}$ – Nominal input voltage.
- $V_{out}$ – Desired output voltage.
- $I_{out}$ – Desired output current.
- $f_{min}$ – Minimum desired output switching frequency at the selected values of $V_{in}$ and $I_{out}$.
- $V_{ripple(pp)}$ – Desired peak-to-peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

**NOTE:** For further information refer to Application Note AN920A/D and AN954/D.

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**Figure 17. Design Formula Table**
<table>
<thead>
<tr>
<th>Device</th>
<th>Package</th>
<th>Shipping①</th>
</tr>
</thead>
<tbody>
<tr>
<td>MC33063ADG</td>
<td>SOIC–8</td>
<td>98 Units / Rail</td>
</tr>
<tr>
<td></td>
<td>(Pb–Free)</td>
<td></td>
</tr>
<tr>
<td>MC33063ADR2G</td>
<td>SOIC–8</td>
<td>2500 Units / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>(Pb–Free)</td>
<td></td>
</tr>
<tr>
<td>SC33063ADR2G</td>
<td>SOIC–8</td>
<td>2500 Units / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>(Pb–Free)</td>
<td></td>
</tr>
<tr>
<td>MC33063AP1G</td>
<td>PDIP–8</td>
<td>50 Units / Rail</td>
</tr>
<tr>
<td></td>
<td>(Pb–Free)</td>
<td></td>
</tr>
<tr>
<td>MC33063AVDG</td>
<td>SOIC–8</td>
<td>98 Units / Rail</td>
</tr>
<tr>
<td></td>
<td>(Pb–Free)</td>
<td></td>
</tr>
<tr>
<td>MC33063AVDR2G</td>
<td>SOIC–8</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(Pb–Free)</td>
<td></td>
</tr>
<tr>
<td>NCV33063AVDR2G*</td>
<td>SOIC–8</td>
<td>2500 Units / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>(Pb–Free)</td>
<td></td>
</tr>
<tr>
<td>MC33063AVPG</td>
<td>PDIP–8</td>
<td>50 Units / Rail</td>
</tr>
<tr>
<td></td>
<td>(Pb–Free)</td>
<td></td>
</tr>
<tr>
<td>MC34063ADG</td>
<td>SOIC–8</td>
<td>98 Units / Rail</td>
</tr>
<tr>
<td></td>
<td>(Pb–Free)</td>
<td></td>
</tr>
<tr>
<td>MC34063ADR2G</td>
<td>SOIC–8</td>
<td>2500 Units / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>(Pb–Free)</td>
<td></td>
</tr>
<tr>
<td>SC34063ADR2G</td>
<td>SOIC–8</td>
<td>2500 Units / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>(Pb–Free)</td>
<td></td>
</tr>
<tr>
<td>MC34063AP1G</td>
<td>PDIP–8</td>
<td>50 Units / Rail</td>
</tr>
<tr>
<td></td>
<td>(Pb–Free)</td>
<td></td>
</tr>
<tr>
<td>SC34063AP1G</td>
<td>PDIP–8</td>
<td>50 Units / Rail</td>
</tr>
<tr>
<td></td>
<td>(Pb–Free)</td>
<td></td>
</tr>
<tr>
<td>MC33063MNTXG</td>
<td>DFN8</td>
<td>4000 Units / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>(Pb–Free)</td>
<td></td>
</tr>
</tbody>
</table>

①For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*NCV33063A: $T_\text{low} = -40^\circ\text{C}, T_\text{high} = +125^\circ\text{C}$. Guaranteed by design. NCV prefix is for automotive and other applications requiring site and change control.

SENSEFET is a trademark of Semiconductor Components Industries, LLC.
NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION a APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DETAILS A AND B SHOW OPTIONAL CONSTRUCTIONS FOR TERMINALS.

DIMENSIONS: MILLIMETERS

<table>
<thead>
<tr>
<th>DIM</th>
<th>MIN</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.80</td>
<td>1.00</td>
</tr>
<tr>
<td>A1</td>
<td>0.00</td>
<td>0.05</td>
</tr>
<tr>
<td>A3</td>
<td>0.20 REF</td>
<td></td>
</tr>
<tr>
<td>b</td>
<td>0.25</td>
<td>0.35</td>
</tr>
<tr>
<td>D</td>
<td>4.00 BSC</td>
<td></td>
</tr>
<tr>
<td>D2</td>
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<td>2.21</td>
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<tr>
<td>E</td>
<td>4.00 BSC</td>
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<tr>
<td>E2</td>
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<tr>
<td>e</td>
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<tr>
<td>K</td>
<td>0.20</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>0.30</td>
<td>0.50</td>
</tr>
<tr>
<td>L1</td>
<td>0.15</td>
<td></td>
</tr>
</tbody>
</table>

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot ",", may or may not be present.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
MECHANICAL CASE OUTLINE

PDIP-8
CASE 626-05
ISSUE P

DATE 22 APR 2015

NOTE 8

NOTES:
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACK-
   AGE SEATED IN JEDEC SEATING PLANE GAUGE G5-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH
   OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE
   NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM
   PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR
   TO DATUM C.
6. DIMENSION b2 IS MEASURED AT THE LEAD TIPS WITH THE
   LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE
   LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE
   CORNERS).

<table>
<thead>
<tr>
<th>INCHES</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.015</td>
</tr>
<tr>
<td>A1</td>
<td>0.115</td>
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<tr>
<td>b</td>
<td>0.014</td>
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<tr>
<td>b1</td>
<td>0.005</td>
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<tr>
<td>b2</td>
<td>0.000 TYP</td>
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<tr>
<td>C</td>
<td>0.008</td>
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<td>M2</td>
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<tr>
<td>M3</td>
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<td>M4</td>
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<tr>
<td>M5</td>
<td>0.350</td>
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</table>

***This information is generic. Please refer to device data sheet for actual part marking.***

PDIP-8 MARKING DIAGRAM

XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

XXXXXXX

A
WL
YYWWG

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**SOIC–8 NB**

**CASE 751–07**

**ISSUE AK**

**DATE 16 FEB 2011**

**NOTES:**
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

**DIMENSIONS:**

<table>
<thead>
<tr>
<th>MILLIMETERS</th>
<th>INCHES</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>4.80</td>
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<tr>
<td>B</td>
<td>3.80</td>
</tr>
<tr>
<td>C</td>
<td>1.35</td>
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<tr>
<td>D</td>
<td>0.51</td>
</tr>
<tr>
<td>E</td>
<td>1.75</td>
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<tr>
<td>F</td>
<td>0.53</td>
</tr>
<tr>
<td>G</td>
<td>0.10</td>
</tr>
<tr>
<td>H</td>
<td>0.19</td>
</tr>
<tr>
<td>J</td>
<td>0.40</td>
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<tr>
<td>K</td>
<td>0.25</td>
</tr>
<tr>
<td>L</td>
<td>1.27</td>
</tr>
</tbody>
</table>

**SOLDERING FOOTPRINT**

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “*”, may or may not be present. Some products may not follow the Generic Marking.

**GENERIC MARKING DIAGRAM**

**STYLES ON PAGE 2**
<table>
<thead>
<tr>
<th>STYLE 1:</th>
<th>STYLE 2:</th>
<th>STYLE 3:</th>
<th>STYLE 4:</th>
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</thead>
<tbody>
<tr>
<td>PIN 1. EMMITTER</td>
<td>PIN 1. COLLECTOR, DIE, #1</td>
<td>PIN 1. DRAIN, DIE #1</td>
<td>PIN 1. ANODE</td>
</tr>
<tr>
<td>PIN 1. DRAIN 1</td>
<td>PIN 1. SOURCE</td>
<td>PIN 1. INPUT</td>
<td>PIN 1. COLLECTOR, DIE #1</td>
</tr>
<tr>
<td>PIN 1. SOURCE 1</td>
<td>PIN 1. N-GATE</td>
<td>PIN 1. GROUND</td>
<td>PIN 1. ANODE</td>
</tr>
<tr>
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<td>PIN 1. GROUND</td>
<td>PIN 1. ANODE</td>
</tr>
<tr>
<td>PIN 1. INPUT</td>
<td>PIN 1. DRAIN</td>
<td>PIN 1. OUTPUT</td>
<td>PIN 1. BASE, #1</td>
</tr>
<tr>
<td>PIN 1. SOURCE</td>
<td>PIN 1. DRAIN</td>
<td>PIN 1. OUTPUT</td>
<td>PIN 1. SOURCE</td>
</tr>
<tr>
<td>PIN 1. INPUT</td>
<td>PIN 1. DRAIN</td>
<td>PIN 1. COMMON</td>
<td>PIN 1. BASE, #1</td>
</tr>
<tr>
<td>PIN 1. DRAIN</td>
<td>PIN 1. SOURCE</td>
<td>PIN 1. COMMON</td>
<td>PIN 1. BASE, #1</td>
</tr>
<tr>
<td>PIN 1. DRAIN</td>
<td>PIN 1. SOURCE</td>
<td>PIN 1. SOURCE</td>
<td>PIN 1. BASE, #1</td>
</tr>
<tr>
<td>PIN 1. DRAIN</td>
<td>PIN 1. SOURCE</td>
<td>PIN 1. SOURCE</td>
<td>PIN 1. BASE, #1</td>
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<tr>
<td>PIN 1. SOURCE</td>
<td>PIN 1. SOURCE</td>
<td>PIN 1. SOURCE</td>
<td>PIN 1. BASE, #1</td>
</tr>
</tbody>
</table>

**DESCRIPTION:**

- **STYLE 13:**
  - PIN 1. N.C.
  - PIN 1. SOURCE
  - PIN 1. DRAIN
  - PIN 1. DRAIN
  - PIN 1. DRAIN
  - PIN 1. DRAIN
  - PIN 1. DRAIN
  - PIN 1. DRAIN

- **STYLE 14:**
  - PIN 1. N-SOURCE
  - PIN 1. N-SOURCE
  - PIN 1. N-SOURCE
  - PIN 1. N-SOURCE
  - PIN 1. N-SOURCE
  - PIN 1. N-SOURCE
  - PIN 1. N-SOURCE
  - PIN 1. N-SOURCE

- **STYLE 15:**
  - PIN 1. ANODE
  - PIN 1. SOURCE
  - PIN 1. SOURCE
  - PIN 1. SOURCE
  - PIN 1. SOURCE
  - PIN 1. SOURCE
  - PIN 1. SOURCE
  - PIN 1. SOURCE

- **STYLE 16:**
  - PIN 1. ANODE
  - PIN 1. ANODE
  - PIN 1. ANODE
  - PIN 1. ANODE
  - PIN 1. ANODE
  - PIN 1. ANODE
  - PIN 1. ANODE
  - PIN 1. ANODE

- **STYLE 17:**
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  - PIN 1. VCC
  - PIN 1. VCC
  - PIN 1. VCC
  - PIN 1. VCC
  - PIN 1. VCC
  - PIN 1. VCC
  - PIN 1. VCC

- **STYLE 18:**
  - PIN 1. I/O LINE 1
  - PIN 1. I/O LINE 1
  - PIN 1. I/O LINE 1
  - PIN 1. I/O LINE 1
  - PIN 1. I/O LINE 1
  - PIN 1. I/O LINE 1
  - PIN 1. I/O LINE 1
  - PIN 1. I/O LINE 1

- **STYLE 19:**
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  - PIN 1. GND
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- **STYLE 20:**
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- **STYLE 21:**
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  - PIN 1. BASE, #1
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  - PIN 1. BASE, #1
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- **STYLE 22:**
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- **STYLE 23:**
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  - PIN 1. I/O LINE 1

- **STYLE 24:**
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  - PIN 1. I/O LINE 1

- **STYLE 25:**
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- **STYLE 26:**
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  - PIN 1. I/O LINE 1
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  - PIN 1. I/O LINE 1
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  - PIN 1. I/O LINE 1
  - PIN 1. I/O LINE 1

- **STYLE 27:**
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  - PIN 1. I/O LINE 1

- **STYLE 28:**
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