Design of a QR Adapter with Improved Efficiency and Low Standby Power
Agenda

1. Quasi-Resonance (QR) Generalities
2. The Valley Lockout Technique
3. The NCP1379/1380
4. Step by Step Design Procedure
5. Performances of a 60 W Adapter Featuring Valley Lockout
Agenda

1. Quasi-Resonance (QR) Generalities
2. The Valley Lockout Technique
3. The NCP1379/1380
4. Step by Step Design Procedure
5. Performances of a 60 W Adapter Featuring Valley Lockout
What is Quasi-Square Wave Resonance?

- MOSFET turns on when $V_{DS}(t)$ reaches its minimum value.
  - Minimizes switching losses
  - Improves the EMI signature
Quasi-Resonance Operation

- In DCM, $V_{DS}$ must drop from $(V_{in} + V_{reflect})$ to $V_{in}$
- Because of $L_p$-$C_{lump}$ network → oscillations appear
- Oscillation half period: $t_x = \pi \sqrt{L_p C_{lump}}$
A Need to Limit the Switching Frequency

• In a self-oscillating QR, $F_{sw}$ increases as the load decreases

  Higher losses at light load if $F_{sw}$ is not limited

• 2 methods to limit $F_{sw}$:
  – Frequency clamp with frequency foldback
  – Changing valley with valley lockout
Frequency Clamp in QR Converters

- In light load, frequency increases and hits clamp
  - Multiple valley jumps
  - Jumps occur at audible range
  - Creates signal instability
Agenda

1. Quasi-Resonance (QR) Generalities
2. The Valley Lockout Technique
3. The NCP1379/1380
4. Step by Step Design Procedure
5. Performances of a 60 W Adapter Featuring Valley Lockout
The Valley Lockout

- As the load decreases, the controller changes valley (1st to 4th valley in NCP1380)
- The controller stays locked in a valley until the output power changes significantly.
  - No valley jumping noise
  - Natural switching frequency limitation

![Diagram showing VCO mode and QR operation withvals](image-url)
The Valley Lockout

- FB comparators select the valley and pass the information to a counter.
- The hysteresis of FB comparators locks the valley.
- 2 possible operating set points for a given FB voltage.

![Graph showing VCO vs. V_FB (V)]

- **V_FB increases** ($P_{OUT}$ increases)
- **V_FB decreases** ($P_{OUT}$ decreases)
Agenda

1. Quasi-Resonance (QR) Generalities
2. The Valley Lockout Technique
3. The NCP1379/1380
4. Step by Step Design Procedure
5. Performances of a 60 W Adapter Featuring Valley Lockout
NCP1379/1380 Features

• Operating modes:
  – QR current-mode with valley lockout for noise immunity
  – VCO mode in light load for improved efficiency

• Protections
  – Over power protection
  – Soft-start
  – Short circuit protection
  – Over voltage protection
  – Over temperature protection
  – Brown-Out

❖ Mass production: Q4 2009
QR Mode with Valley Lockout

- **Operating principle:**
  - Locks the controller into a valley (up to the 4th) according to FB voltage.
  - Peak current adjusts according to FB voltage to deliver the necessary output power.

- **Advantages**
  - Solves the valley jumping instability in QR converters
  - Achieves higher min $F_{\text{sw}}$ and lower max $F_{\text{sw}}$ than in traditional QR converters
  - Reduce the transformer size
VCO Mode

- Occurs when $V_{FB} < 0.8$ V ($P_{out}$ decreasing) or $V_{FB} < 1.4$ V ($P_{out}$ increasing)
- Fixed peak current (17.5% of $I_{pk,max}$), variable frequency set by the FB loop.
Combined ZCD and OPP

- Zero-Crossing Detection (ZCD) and Over Power Protection (OPP) are achieved by reading the Aux. winding voltage
  - ZCD function used during the off-time of MOSFET (positive voltage).
  - OPP function used during the on-time of MOSFET (negative voltage)
NCP1380 Versions

- 4 versions of NCP1380: A, B, C and D

<table>
<thead>
<tr>
<th></th>
<th>OTP</th>
<th>OVP</th>
<th>BO</th>
<th>Auto-Recovery</th>
<th>Latched</th>
</tr>
</thead>
<tbody>
<tr>
<td>NCP1380 / A</td>
<td>X</td>
<td>X</td>
<td></td>
<td>Over current protection</td>
<td>X</td>
</tr>
<tr>
<td>NCP1380 / B</td>
<td>X</td>
<td>X</td>
<td></td>
<td>Over current protection</td>
<td>X</td>
</tr>
<tr>
<td>NCP1380 / C</td>
<td></td>
<td>X</td>
<td>X</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>NCP1380 / D</td>
<td></td>
<td>X</td>
<td>X</td>
<td></td>
<td>X</td>
</tr>
</tbody>
</table>

**OTP**: Over Temperature Protection

**OVP**: Over Voltage Protection

**BO**: Bown-Out
Short-Circuit Protection

- Internal 80 ms timer for short-circuit validation.
- Additional CS comparator with reduced LEB to detect winding short-circuit.
- \[ V_{CS\text{(stop)}} = 1.5 \times V_{ILIMIT} \]
Short-Circuit Protection (A and C versions)

- A and C versions: the fault is latched.
  - $V_{CC}$ is pulled down to 5 V and waits for ac removal.

![Diagram of Short-Circuit Protection](image)
Short Circuit Protection (B and D)

- Auto-recovery short circuit protection: the controller tries to restart
- Auto-recovery imposes a low burst in fault mode.

Low average input power in fault condition
Fault Pin Combinations

- **OVP / OTP**
  - NCP1380 A & B versions

- **OVP / BO**
  - NCP1380 C & D versions, NCP1379

- OVP and OTP or OVP and BO combined on one pin.
- Less external components needed.
Agenda

1. Quasi-Resonance (QR) Generalities
2. The Valley Lockout Technique
3. The NCP1379/1380
4. Step by Step Design Procedure
5. Performances of a 60 W Adapter Featuring Valley Lockout
Step by Step Design Procedure

- Calculating the QR transformer
- Predicting the switching frequency
- Implementing Over Power Compensation
- Improving the efficiency at light load with the VCO mode
- Choosing the startup resistors
- Implementing synchronous rectification
Design Example

- Power supply specification:
  - \( V_{out} = 19 \text{ V} \)
  - \( P_{out} = 60 \text{ W} \)
  - \( F_{sw,min} = 45 \text{ kHz} \) (at \( V_{in} = 100 \text{ Vdc} \))
  - 600 V MOSFET
  - \( V_{in} = 85 \sim 265 \text{ Vrms} \)
  - Standby power consumption < 100 mW @ 230 Vrms
Turns Ratio Calculation

- Derate maximum MOSFET $BV_{dss}$:
  \[ V_{ds,max} = BV_{dss}k_D \]
  \( k_D \): derating factor

- For a maximum bulk voltage, select the clamping voltage:
  \[ V_{clamp} = V_{ds,max} - V_{in,max} - V_{os} \]
  \( V_{os} \): diode overshoot

- Deduce turns ratio:
  \[ N_{ps} = \frac{N_s}{N_p} = \frac{k_c(V_{out} + V_f)}{V_{clamp}} \]

  \( k_c \): clamping coef.
  \( k_c = \frac{V_{clamp}}{V_{reflect}} \)
How to Choose $k_c$

- $k_c$ choice dependant of $L_{\text{leak}}$ (leakage inductance of the transformer)
- $k_c$ value can be chosen to equilibrate MOS conduction losses and clamping resistor losses.

$$P_{\text{Rclamp}} = k_{\text{leak}} \frac{P_{\text{out}}}{\eta} \frac{k_c}{k_c - 1}$$

$$P_{\text{MOS, on}} = R_{\text{dson}} \frac{4 P_{\text{out}}^2}{3 \eta^2 V_{\text{in,min}}^2} \left( \frac{1}{V_{\text{in,min}}} + \frac{k_c}{B V_{\text{dss}} k_D - V_{\text{in,max}} - V_{\text{os}}} \right)$$

Curves plotted for:
- $R_{\text{dson}} = 0.77$ Ω at $T_j = 110$
- $P_{\text{out}} = 60$ W
- $V_{\text{in,min}} = 100$ Vdc
Primary Peak Current and Inductance

\[ P_{out} = \frac{1}{2} L_{pri} I_{pri, peak}^2 F_{sw} \eta \]

\[ T_{sw} = \frac{I_{pri, peak} L_{pri}}{V_{in, min}} + \frac{I_{pri, peak} L_{pri} N_{ps}}{V_{out} + V_f} + \pi \sqrt{\frac{L_{pri} C_{lump}}{F_{sw}} \eta} \]

\[ I_{pri, peak} = \frac{2 P_{out}}{\eta} \left( \frac{1}{V_{in, min}} + \frac{N_{ps}}{V_{out} + V_f} \right) + \pi \sqrt{\frac{2 P_{out} C_{lump} F_{sw}}{\eta}} \]

\[ L_{pri} = \frac{2 P_{out}}{I_{pri, peak}^2 F_{sw} \eta} \]
RMS Current

- Calculate maximum duty-cycle at maximum $P_{out}$ and minimum $V_{in}$:

$$d_{max} = \frac{I_{pri,peak}L_{pri}}{V_{in,min}} F_{sw,min}$$

- Deduce primary and secondary RMS current value:

$$I_{pri,rms} = I_{pri,peak} \sqrt{\frac{d_{max}}{3}}$$

$$I_{sec,rms} = \frac{I_{pri,peak}}{N_{ps}} \sqrt{\frac{1-d_{max}}{3}}$$

**$I_{pri,rms}$ and $I_{sec,rms}$** → Losses calculation
Based on equations from slides 11 to 14:

- **Turns ratio:**
  \[ N_{ps} = \frac{k_c (V_{out} + V_f)}{B_{vds} k_D - V_{in,max} - V_{os}} = \frac{1.3 \times (19 + 0.8)}{600 \times 0.85 - 375 - 10} \Rightarrow N_{ps} \approx 0.25 \]

- **Peak current:**
  \[ I_{pri,peak} = \frac{2P_{out}}{\eta} \left( \frac{1}{V_{in,min}} + \frac{N_{ps}}{V_{out} + V_f} \right) + \pi \sqrt{\frac{2P_{out} C_{lump} F_{sw}}{\eta}} \]
  \[ = \frac{2 \times 60}{0.85} \left( \frac{1}{100} + \frac{0.25}{19.8} \right) + \pi \sqrt{\frac{2 \times 60 \times 250 \times 0.85}{0.85}} \Rightarrow I_{pri,peak} = 3.32 \ A \]

- **Inductance:**
  \[ L_{pri} = \frac{2P_{out}}{I_{pri,peak} F_{sw} \eta} = \frac{2 \times 60}{3.32^2 \times 45 \times 0.85} \Rightarrow L_{pri} = 285 \ \mu H \]

- **Max. duty-cycle:**
  \[ d_{max} = \frac{I_{pri,peak} L_{pri}}{V_{in,min}} F_{sw,min} = \frac{3.32 \times 285 \mu}{100} \times 45 \Rightarrow d_{max} = 0.43 \]

- **Primary rms current:**
  \[ I_{pri,rms} = I_{pri,peak} \sqrt{\frac{d_{max}}{3}} = 3.32 \sqrt{\frac{0.43}{3}} \Rightarrow I_{pri,rms} = 1.26 \ A \]

- **Secondary rms current:**
  \[ I_{sec,rms} = \frac{I_{pri,peak}}{N_{ps}} \sqrt{\frac{1 - d_{max}}{3}} = \frac{3.32}{0.25} \sqrt{\frac{1 - 0.43}{3}} \Rightarrow I_{sec,rms} = 5.8 \ A \]
Predicting the Switching Frequency

- The controller changes valley as the load decreases. 
  
  => How can we predict the switching frequency evolution as the load varies?

- Depending upon the power increase or decrease, the FB levels at which the controller changes valley are different => valley lockout
Predicting the Switching Frequency

- Knowing the FB threshold values, we can calculate $F_{sw}$ evolution and the corresponding $P_{out}$.

\[
F_{sw} = \left( \frac{V_{FB}}{4R_{sense}} + V_{in,dc} \frac{t_{prop}}{L_p} \right) \frac{1}{L_p \left( \frac{1}{V_{in,dc}} + \frac{N_{ps}}{V_{out} + V_f} \right) + (1+2n)\pi \sqrt{L_p C_{lump}}} 
\]

\[
P_{out} = \frac{1}{2} L_p \left( \frac{V_{FB}}{4R_{sense}} + V_{in,dc} \frac{t_{prop}}{L_p} \right)^2 F_{sw} \eta 
\]

Replace $V_{FB}$ by the valley thresholds values in the previous slide.
Predicting the Switching Frequency

- Calculate by hand (using the previous equations) or use the Mathcad spreadsheet to deduce the maxima of the switching frequency => EMI

![Graph showing predicted switching frequencies](image)
VCO Mode

- The switching frequency is set by the end of charge of $C_t$ capacitor
- The end of charge of $C_t$ capacitor is controlled by the FB loop

![VCO Mode Diagram]

**Timing capacitor voltage**

Load

$V_{Ct}$

Controlled by FB loop

(Timing capacitor voltage)
4th Valley to VCO Mode Transition

- Output load slightly decreases:

![Graph showing load, V_FB, and V_FBth transitions between 4th valley and VCO mode with time periods T_sw1 and T_sw2.]
How to Calculate $C_t$ Capacitor?

- Switching frequency at the end of the 4th valley operation ($V_{FB} = 0.8 \ V$):

$$T_{sw,4th-VCO} = \left( \frac{0.8}{4R_{sense}} + t_{prop} \frac{V_{in,max}\sqrt{2}}{L_p} \right) L_p \left( \frac{1}{V_{in,max}\sqrt{2}} + \frac{N_{ps}}{V_{out} + V_f} \right) + 7\pi\sqrt{L_p C_{OSS}}$$

- $T_{sw}$ gap between 4th valley and VCO mode must not exceed 10 µs (based on lab experiments) for $V_{FB} = 1.4 \ V$ (hysteresis):

$$T_{sw,VCO} = T_{sw,4th-VCO} + 10 \ \mu s$$

- The relationship between $V_{FB}$ and $V_{Ct}$ is:

$$V_{Ct} = 6.5 - (10 / 3)V_{FB} = 6.5 - (10 / 3) \times 1.4 = 1.83 \ V$$

$$C_t = \frac{I_{Ct} T_{sw,VCO}}{1.83}$$
**$C_t$ Design Example**

- Switching frequency at the end of the 4\(^{th}\) valley operation:

  
  \[
  T_{sw,4th-VCO} = \left( \frac{0.8}{4 \times 0.23} + 300n \frac{265\sqrt{2}}{285\mu} \right) 285\mu \left( \frac{1}{265\sqrt{2}} + \frac{0.25}{19 + 0.8} \right) + 7\pi \sqrt{285\mu \times 250\mu}
  \]

  = 10.7 \mu s

- $T_{sw}$ gap between 4\(^{th}\) valley and VCO mode must not exceed 10 \mu s (based on lab experiments):

  \[
  T_{sw,VCO} = T_{sw,4th-VCO} + 10 \mu s = 10.7\mu + 10\mu = 20.7\mu s
  \]

- The timing capacitor value is:

  \[
  C_t = \frac{I_{ct}T_{sw,VCO}}{1.83} = \frac{20\mu \times 20.7\mu}{1.83} = 226 pF
  \]

- Finally, we choose $C_t = 200$ pF
OPP: How it Works?

- $L_{aux}$ with flyback polarity swings to $-N V_{IN}$ during the on time.
- Adjust amount of OPP voltage with $(R_{zcd} + R_{opu}) // R_{opl}$.
- $V_{CS,max} = 0.8 \text{ V} + V_{OPP}$
- The diode bypass $R_{opu}$ during the off-time for optimum zero-crossing detection.

![Diagram of OPP circuit](image-url)
OPP Amount Needed for the Design

- Because of the propagation delay, at high line:

\[ I_{pk(high)} = \frac{0.8}{R_{sense}} + V_{in,max} \sqrt{2 \frac{t_{prop}}{L_p}} \]

\[ I_{pk(high)} = \frac{0.8}{0.23} + \frac{265\sqrt{2 \times 600 \times 10^{-9}}}{290 \times 10^{-6}} = 4.32\ A \]

- The switching frequency is:

\[ T_{sw(high)} = I_{pk(high)} L_p \left( \frac{1}{V_{in,max} \sqrt{2}} + \frac{N_{ps}}{V_{out} + V_f} \right) + \pi \sqrt{L_p C_{lump}} \]

\[ T_{sw(high)} = 4.32 \times 290 \times 10^{-6} \left( \frac{1}{265\sqrt{2}} + \frac{0.25}{19 + 0.8} \right) + \pi \sqrt{285 \times 10^{-6} \times 250 \times 10^{-12}} = 19.5\ \mu s \]

- The power capability at high line is:

\[ P_{out(high)} = \frac{1}{2} L_p I_{pk(high)}^2 \frac{1}{T_{sw(high)}} \eta \]

\[ P_{out(high)} = \frac{1}{2} \frac{290 \times 10^{-6} \times 4.32^2}{19.5 \times 10^{-6}} \times 0.85 = 116\ W \]
Amount of OPP Voltage Needed

- Limit the output power to $P_{out(\text{limit})} = 70$ W at high line.
- What is the peak current $I_{pk(\text{limit})}$ corresponding to $P_{out(\text{limit})}$?

\[
I_{pk(\text{limit})} = \frac{L_p \left( \frac{1}{V_{in(max),dc}} + \frac{N_{ps}}{V_{out} + V_f} \right) + \sqrt{L_p^2 \left( \frac{1}{V_{in(max),dc}} + \frac{N_{ps}}{V_{out} + V_f} \right)^2 + 2 \frac{L_p \eta}{P_{out(\text{limit})}} \pi \sqrt{L_p C_{lump}}} - \frac{L_p \eta}{P_{out(\text{limit})}}}{\frac{L_p \eta}{P_{out(\text{limit})}}}
\]

\[
I_{pk(\text{limit})} = \frac{285 \mu \left( \frac{1}{375} + \frac{0.25}{19 + 0.8} \right) + \sqrt{\left(285 \mu \right)^2 \left( \frac{1}{375} + \frac{0.25}{19 + 0.8} \right)^2 + 2 \frac{285 \mu \times 0.85}{70} \pi \sqrt{285 \mu \times 250 \mu}}}{285 \mu \times 0.85 \frac{70}{70}} = 2.67 \text{ A}
\]

- Amount of OPP voltage needed:

\[
V_{OPP} = 0.8 \left( 1 - \frac{I_{pk(\text{limit})}}{I_{pk(max)}} \right)
\]

\[
V_{OPP} = 0.8 \left( 1 - \frac{2.67}{4.32} \right) = 300 \text{ mV}
\]
Calculating the OPP Resistors

- The amount of OPP voltage needed to limit $P_{\text{out}}$ to 70 W is: $V_{\text{OPP}} = 300 \text{ mV}$

- Resistor divider law:

  $$\frac{R_{\text{opu}} + R_{\text{zcd}}}{R_{\text{opl}}} = \frac{N_{p,\text{aux}} V_{\text{IN}} - V_{\text{OPP}}}{V_{\text{OPP}}}$$

  $$\frac{R_{\text{opu}} + R_{\text{zcd}}}{R_{\text{opl}}} = \frac{0.18 \times 375 - 0.3}{0.3} = 224$$

- We choose: $R_{\text{opl}} = 1 \text{ k}\Omega$ and $R_{\text{zcd}} = 1 \text{ k}\Omega$

  $$R_{\text{opu}} = 221 R_{\text{opl}} - R_{\text{zcd}}$$

  $$R_{\text{opu}} = 223 \text{ k}\Omega$$
Why is the OPP Non Dissipative?

- Input voltage information given by auxiliary winding
- In light load: VCO mode $\Rightarrow T_{sw}$ expands, thus the average current in the resistor bridge decreases

\[
I_{\text{bridge,avg}} = \frac{1}{R_{zcd} + R_{\text{opu}} + R_{\text{opl}}} \left( \frac{t_{\text{on}}}{T_{\text{sw}}} N_{p,\text{aux}} V_{IN} + \frac{1}{R_{\text{opu}} + R_{\text{opl}}} \frac{t_{\text{off}}}{T_{\text{sw}}} (V_{CC} + V_f) \right)
\]

- Previous example: $R_{\text{opu}} = 220 \text{ k}\Omega$, $R_{\text{opl}} = 1 \text{ k}\Omega$, $R_{zcd} = 1 \text{ k}\Omega$
  
  At light load ($P_{out} = 4 \text{ W}$), $t_{\text{on}} = 1.2 \mu\text{s}$, $t_{\text{off}} = 3.6 \mu\text{s}$, $T_{\text{sw}} = 40 \mu\text{s}$

\[
I_{\text{bridge,mean}} = \frac{1}{220k + 1k + 1k} \frac{1.2\mu}{40\mu} \times 0.18 \times 375 + \frac{1}{220k + 1k} \frac{3.6\mu}{40\mu} 16 = 15 \mu\text{A}
\]
• The startup resistor can either be connected:
  - To the bulk capacitor with $R_{\text{startup}}$
  - To the half-wave – for a similar charging current, take $R_{\text{startup}}/\pi$
Startup Capacitor Calculation

- \( C_{Vcc} \) calculated to allow the power supply to close the loop before \( V_{CC} \) falls below \( V_{CC(\text{off})} \)

\[
C_{Vcc} = \frac{\left( I_{CC3A} + Q_g F_{sw} \right) t_{reg}}{V_{CC(\text{on})} - V_{CC(\text{off})}}
\]

\[
C_{Vcc} = \frac{(2.4m + 17n \times 45000) \times 10m}{17 - 9} = 3.9 \mu F
\]

We choose \( C_{Vcc} = 4.7 \mu F \)

- Needed startup current to charge \( C_{Vcc} \):

\[
I_{Cvcc} = \frac{V_{CC(\text{on})} C_{Vcc}}{t_{\text{startup}}}
\]

\[
I_{Cvcc} = \frac{17 \times 4.7 \mu A}{2.8} = 28.5 \mu A
\]
Startup Resistor Calculation

• Bulk capacitor connection
  ➢ Resistor calculation:
  \[ R_{\text{startup}} = \frac{V_{\text{in,min}} \sqrt{2}}{I_{\text{CcC}} + I_{\text{CC(start)}}} \]
  \[ R_{\text{startup}} = \frac{85\sqrt{2}}{28.5\mu + 15\mu} = 2.76 \text{M} \Omega \]
  ➢ Power dissipation:
  \[ P_{\text{startup}} = \frac{(V_{\text{in,max}} \sqrt{2} - V_{\text{CC}})^2}{R_{\text{startup}}} \]
  \[ P_{\text{startup}} = \frac{(265\sqrt{2} - 16)^2}{2.68 \text{M}} = 55 \text{mW} \]

• Half wave connection
  ➢ Resistor calculation:
  \[ R_{\text{startup}} = \frac{V_{\text{in,min}} \sqrt{2}}{I_{\text{CcC}} + I_{\text{CC(start)}}} \]
  \[ R_{\text{startup}} = \frac{85\sqrt{2}/\pi}{28.5\mu + 15\mu} = 880 \text{k} \Omega \]
  ➢ Power dissipation:
  \[ P_{\text{startup}} = \frac{(V_{\text{in,max}} \sqrt{2} - V_{\text{CC}})^2}{R_{\text{startup}}} \]
  \[ P_{\text{startup}} = \frac{(265\sqrt{2}/\pi - 16)^2}{880 \text{k}} = 16 \text{mW} \]

Half wave connection saves 39 mW!
Synchronous Rectification

- High rms currents in secondary side → increased losses in the output diode.
- Replace the diode with a MOSFET featuring a very low $R_{DS(on)}$.

<table>
<thead>
<tr>
<th>+</th>
<th>-</th>
</tr>
</thead>
<tbody>
<tr>
<td>Increased efficiency</td>
<td>Degraded light load and standby power consumption</td>
</tr>
</tbody>
</table>
Losses in the Sync. Rect. Switch

\[ P_{\text{Q_{sync}}} = P_{\text{ON}} + P_{\text{Q_{diode}}} \]

- **Body diode conduction losses**
  \[ P_{\text{Q_{diode}}} = V_f I_{\text{out}} F_{\text{sw}} t_{\text{delay}} \]
  Low if \( t_{\text{delay}} \) small

- **MOSFET conduction losses**
  \[ P_{\text{ON}} = R_{DS(on)} I_{sec,rms}^2 \]

- **Losses in the Sync. Rect. switch are mainly conduction losses.**

- Body diode conducts before the MOSFET is turned-on.
  
  ![Diagram](image)

  No switching losses
Choosing the Sync. Rect. MOSFET

- Target around 1 W conduction losses in Sync. Rect. switch to avoid using an heatsink.

\[ R_{DS(on120)} = \frac{1W}{I_{sec,RMS}^2} \]

- \( V_{out} = 19 \) V
- \( F_{sw,min} = 45 \) kHz
- Universal mains

<table>
<thead>
<tr>
<th>Product</th>
<th>( R_{DS(on110)} ) (mΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MBR20H150</td>
<td>70</td>
</tr>
<tr>
<td>R_{DS(on110)}</td>
<td>50</td>
</tr>
<tr>
<td>R_{DS(on110)}</td>
<td>30</td>
</tr>
</tbody>
</table>

\[ P_{loss}(W) \]

\[ I_{out}(A) \]
60 W QR Sync. Rect. Calculations

- **Body diode losses:**
  \[ P_{Q\text{diode}} = V_f I_{\text{out}} F_{sw} t_{\text{delay}} = 0.7 \times 3.2 \times 45000 \times 70n \]
  \[ P_{Q\text{diode}} = 7 \text{ mW} \]

- **MOSFET losses:**
  \[ P_{\text{ON}} = R_{DS(on)} I_{20} I_{\text{sec, rms}}^2 = 30m \times 5.8^2 \]
  \[ P_{\text{ON}} = 1W \]

- **Total Sync. Rect. switch losses:**
  \[ P_{Q\text{sync}} = 1 + 0.007 \approx 1W \]

- **Losses into the MBR20200 diode:**
  2.6 W

- **Power loss saving:**
  1.6 W
Agenda

1. Quasi-Resonance (QR) Generalities
2. The valley lockout technique
3. The NCP1379/1380
4. Step by step design procedure
5. Performances of a 60 W adapter featuring valley lockout
NCP1380B in a 19 V, 60 W adapter
Startup

- Startup resistor connected to the **bulk rail** ($R_{\text{startup}} = 2.7 \ \text{M}\Omega$)
  - $T_{\text{startup}} = 2.68 \ \text{s}$

- Startup resistor connected to the **half-wave** ($R_{\text{startup}} = 910 \ \text{k}\Omega$)
  - $T_{\text{startup}} = 2.1 \ \text{s}$
Transient Load Step

- Load step: 3% to 100% of output load with a slew rate of 1 A / µs
- $V_{in} = 230$ Vrms

The overshoot / undershoot is 1% of the nominal value of $V_{out}$
Short-Circuit

- A short-circuit is made at the board output.
- The circuit pulses with a low burst (5%)
- The measured averaged input power is: $P_{in} = 412.4 \text{ mW}$ for $V_{in} = 230 \text{ Vrms}$
## Efficiency

<table>
<thead>
<tr>
<th>115 Vrms</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{out}$ (W)</td>
<td>$P_{out}$ (%)</td>
</tr>
<tr>
<td>60.6</td>
<td>100</td>
</tr>
<tr>
<td>45.5</td>
<td>75</td>
</tr>
<tr>
<td>30.3</td>
<td>50</td>
</tr>
<tr>
<td>15.2</td>
<td>25</td>
</tr>
<tr>
<td>1.0</td>
<td>1.30</td>
</tr>
<tr>
<td>0.7</td>
<td>0.94</td>
</tr>
<tr>
<td>0.5</td>
<td>0.69</td>
</tr>
</tbody>
</table>

**Average efficiency**

(25, 50, 75, 100% of $P_{out\text{,max}}$): 87.9%

<table>
<thead>
<tr>
<th>230 Vrms</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{out}$ (W)</td>
<td>$P_{out}$ (%)</td>
</tr>
<tr>
<td>60.6</td>
<td>100</td>
</tr>
<tr>
<td>45.5</td>
<td>75</td>
</tr>
<tr>
<td>30.3</td>
<td>50</td>
</tr>
<tr>
<td>15.2</td>
<td>25</td>
</tr>
<tr>
<td>1.0</td>
<td>1.325</td>
</tr>
<tr>
<td>0.7</td>
<td>0.958</td>
</tr>
<tr>
<td>0.5</td>
<td>0.71</td>
</tr>
</tbody>
</table>

**Average efficiency**

(25, 50, 75, 100% of $P_{out\text{,max}}$): 87.7%
Improving the No Load Consumption

- At very low output load, the TL431 bias is removed using a special circuit:
No Load Consumption

- $R_{\text{startup}}$ connected to the bulk rail:
  - Without TL431 bias:
    
    | Voltage   | Power Input $P_{\text{in}}$ | Power Output $P_{\text{out}}$ |
    |-----------|-----------------------------|-----------------------------|
    | 115 Vrms  | 60 mW                       | 0 W                         |
    | 230 Vrms  | 98 mW                       | 0 W                         |
  
  - With TL431 bias:
    
    | Voltage   | Power Input $P_{\text{in}}$ | Power Output $P_{\text{out}}$ |
    |-----------|-----------------------------|-----------------------------|
    | 115 Vrms  | 98 mW                       | 0 W                         |
    | 230 Vrms  | 128 mW                      | 0 W                         |

3 MΩ resistor to discharge X2 capacitor included
No Load Consumption

- $R_{\text{startup}}$ connected to the half wave:

  - Without TL431 bias, $R_{\text{startup}} = 1.1 \text{ M}\Omega$ ($T_{\text{startup}} = 2.6 \text{ s} @ 85 \text{ Vrms}$)

<table>
<thead>
<tr>
<th>Voltage</th>
<th>$P_{\text{out}}$</th>
<th>$P_{\text{in}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>115 Vrms</td>
<td>0 W</td>
<td>55 mW</td>
</tr>
<tr>
<td>230 Vrms</td>
<td></td>
<td>90 mW</td>
</tr>
</tbody>
</table>

3 MΩ resistor to discharge X2 capacitor included
Synchronous Rectification Schematic

- TL431 and NCP4302 bias removed at light load.
## Efficiency and No Load Consumption

<table>
<thead>
<tr>
<th>115 Vrms</th>
<th>230 Vrms</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Eff. (%)</strong></td>
<td><strong>Eff. (%)</strong></td>
</tr>
<tr>
<td><strong>Pin (W)</strong></td>
<td><strong>Pin (W)</strong></td>
</tr>
<tr>
<td>60.5</td>
<td>60.5</td>
</tr>
<tr>
<td>45.4</td>
<td>45.4</td>
</tr>
<tr>
<td>30.3</td>
<td>30.3</td>
</tr>
<tr>
<td>15.2</td>
<td>15.2</td>
</tr>
<tr>
<td>1.0</td>
<td>1.0</td>
</tr>
<tr>
<td>0.7</td>
<td>0.7</td>
</tr>
<tr>
<td>0.5</td>
<td>0.5</td>
</tr>
</tbody>
</table>

Average efficiency (25, 50, 75, 100% of \(P_{out,\text{max}}\)): **89.5%**

Average efficiency (25, 50, 75, 100% of \(P_{out,\text{max}}\)): **89.1%**

- **No load consumption:**

<table>
<thead>
<tr>
<th>115 Vrms</th>
<th>230 Vrms</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Pin = 62 mW</strong></td>
<td><strong>Pin = 107 mW</strong></td>
</tr>
</tbody>
</table>

\(P_{out} = 0\) W
Conclusion

• The valley lockout technique allows to solve the valley jumping problem in QR power supplies.

• NCP1380, NCP1379 features:
  • QR current-mode with valley lockout for noise immunity for high load.
  • VCO mode in light load for improved efficiency.
  • OPP, OVP, BO, OTP, soft-start for building safe power supplies

• A complete design method has been presented.

• It is possible to achieve standby power consumption below 100 mW at 230 Vrms with the NCP1380.

• Good efficiency at light load with Sync. Rect if the bias of the TL431 and the Sync. Rec. controller is removed.

• Mathcad spreadsheet and simulations models available.
For More Information

- View the extensive portfolio of power management products from ON Semiconductor at www.onsemi.com

- View reference designs, design notes, and other material supporting the design of highly efficient power supplies at www.onsemi.com/powersupplies