ON Semiconductor®

Half-Bridge Drivers
A Transformer or an All-Silicon Drive?

Agenda

- Topologies using a half-bridge configuration
- The difference between soft and hard-switching
- The gate-drive transformer
- The all-silicon-solution
- Comparison
- Conclusions

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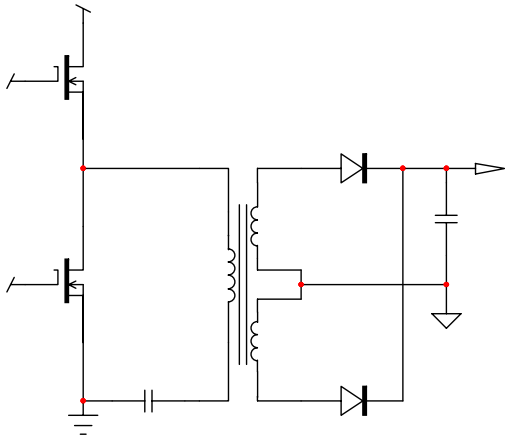
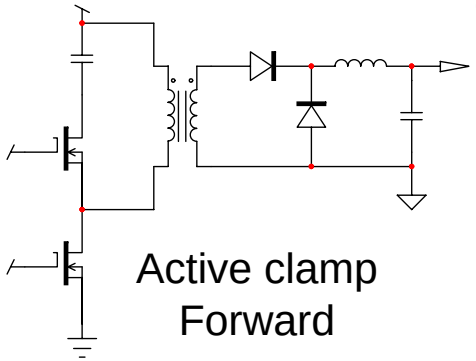
Topology Trend for High Efficiency

- Hard Switching
  - Flyback
  - Forward
  - 2-sw flyback
  - 2-sw forward
  - Full bridge

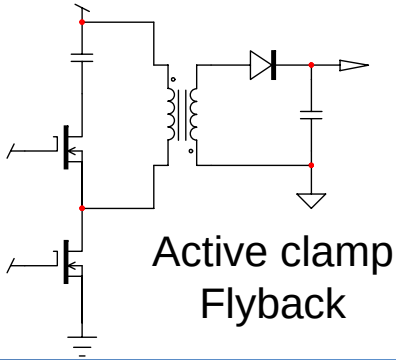
- Soft Switching
  - LLC-HB resonant
  - Active clamp forward
  - Active clamp flyback
  - Asymmetrical half-bridge
  - Full bridge with phase shift



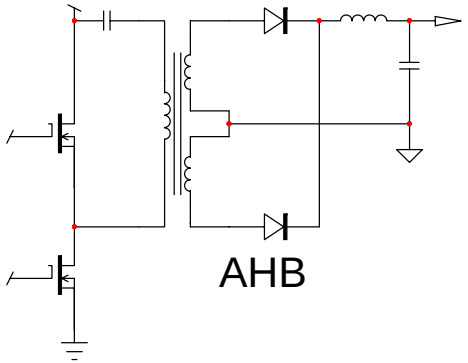
LLC-HB



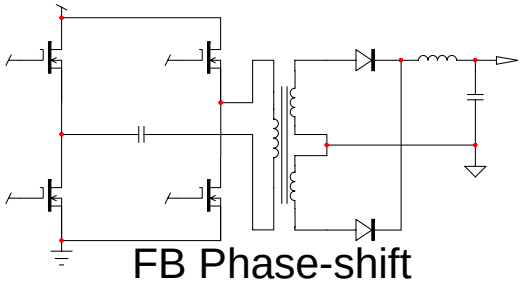
Active clamp
Forward



Active clamp
Flyback



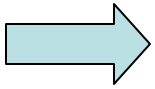
AHB



FB Phase-shift

The High-Side Switch

- To achieve high efficiency, the topologies with ZVS (**Z**ero-**V**oltage **S**witching) behavior are preferred.
- All the soft switching topologies implement the power switch with floating reference pin, e.g. the source pin of MOSFET.
- Why are MOSFETs used in soft switching applications?
  - High frequency operation
  - Body diode (current loop for ZVS)



How to drive the high side MOSFET?

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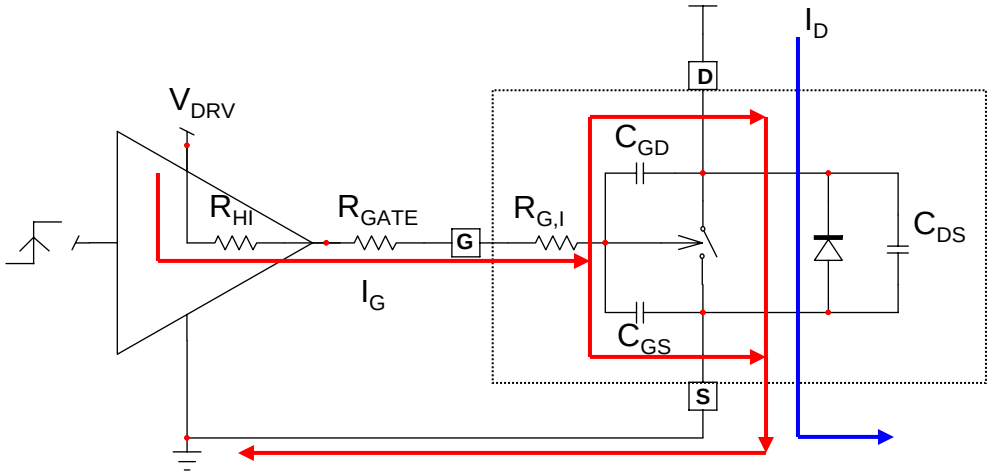
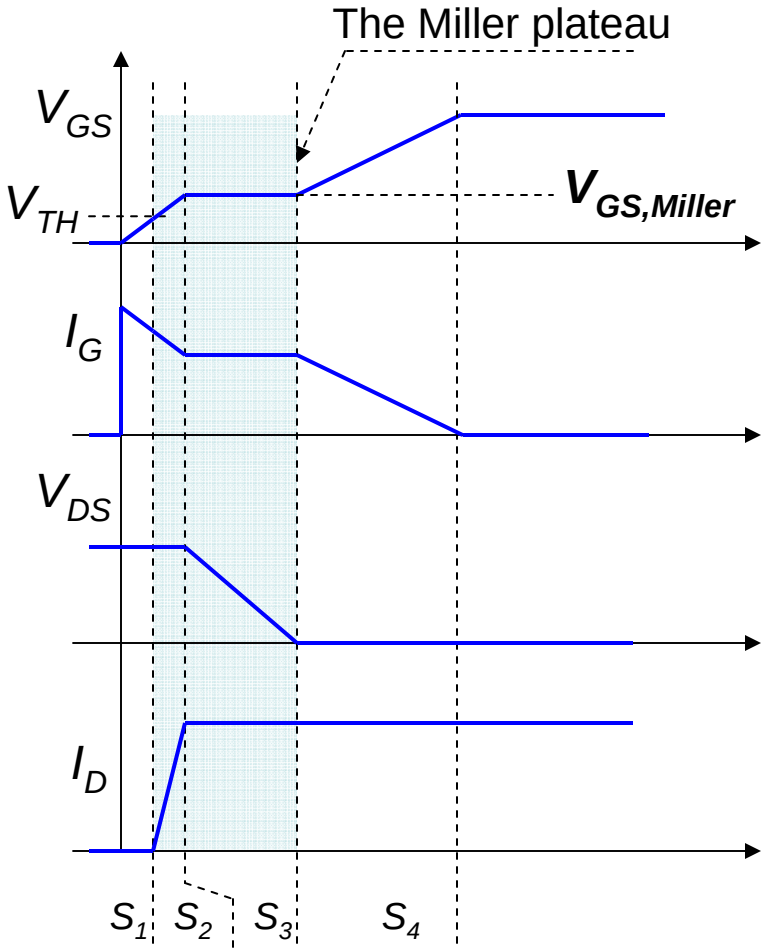
Turn-on Procedure for Hard-switching

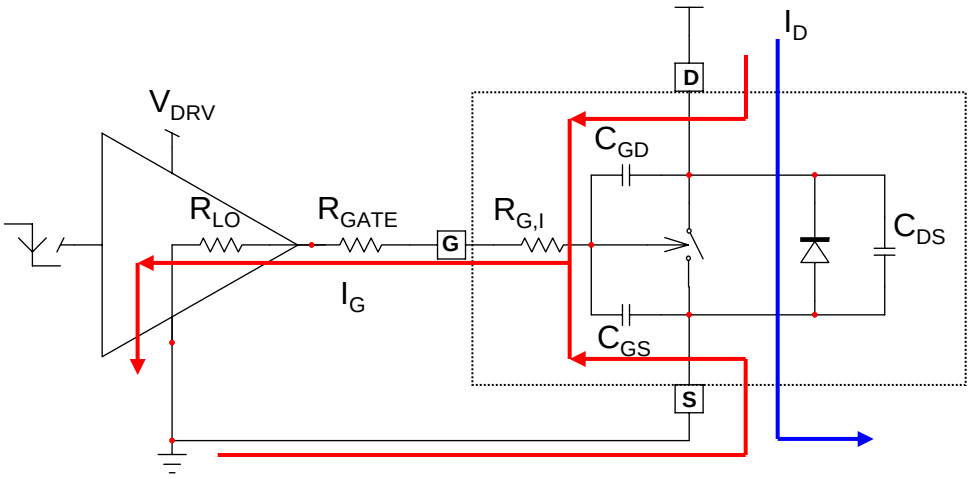


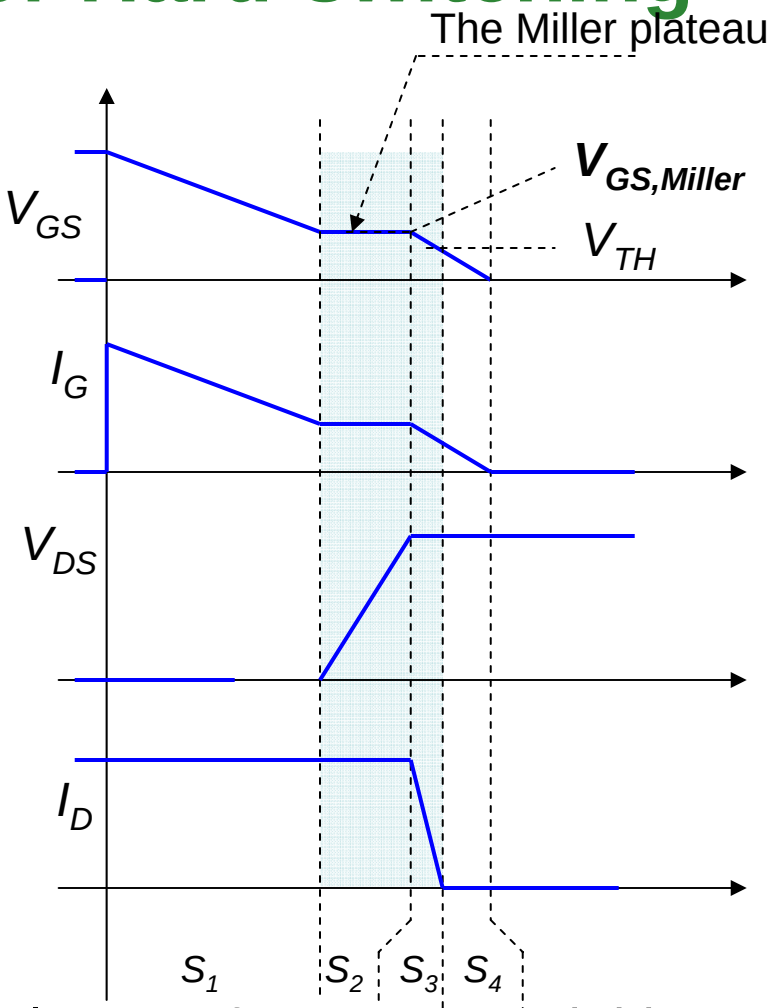


The miller plateau is caused by C_{GD}

- Stages 2 and 3 dominate the switching losses of MOSFET and driver.
- DRV's source capability as V_{GS} is around $V_{GS,Miller}$ is important.

Turn-off Procedure for Hard-switching

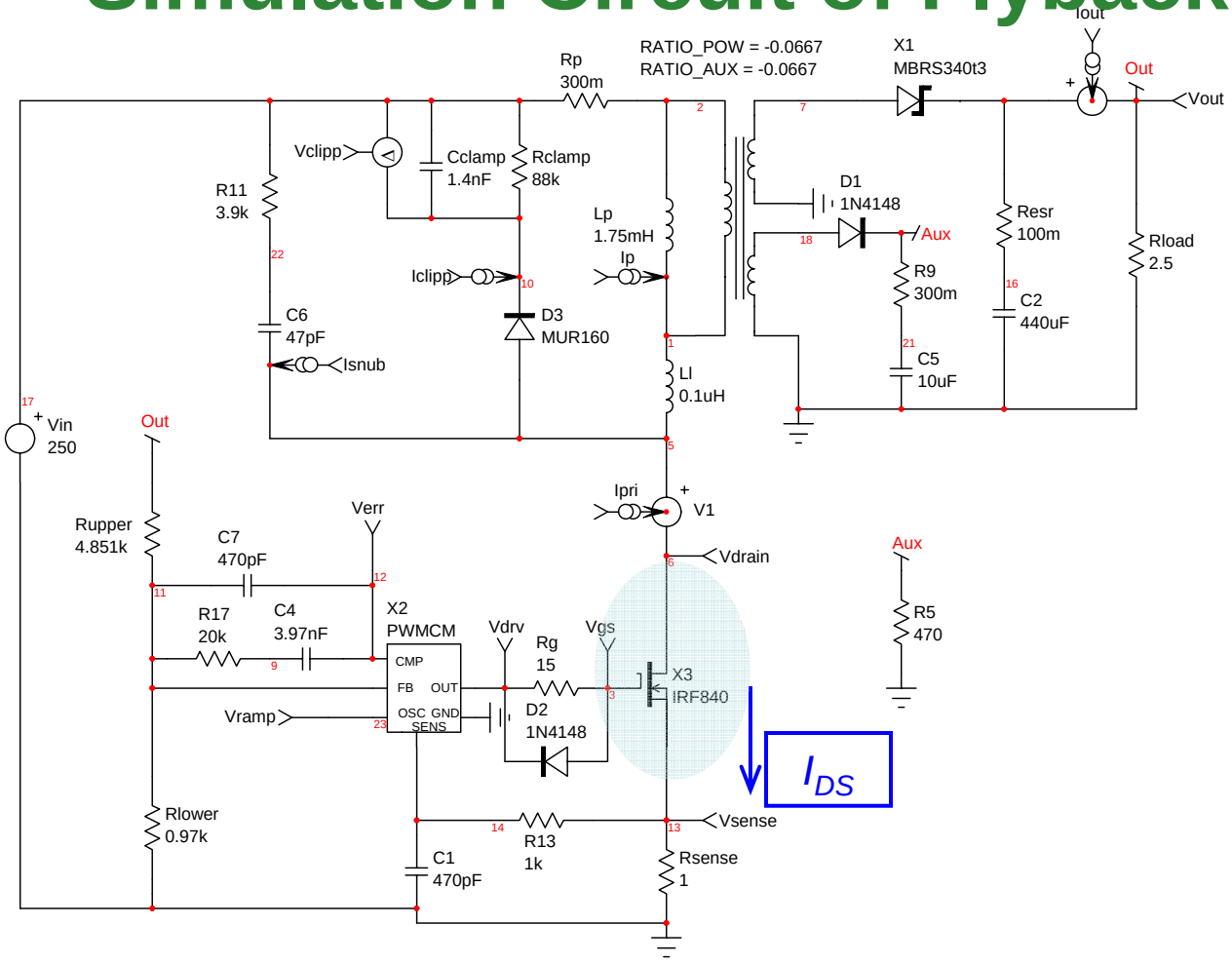




The miller plateau is caused by C_{GD}

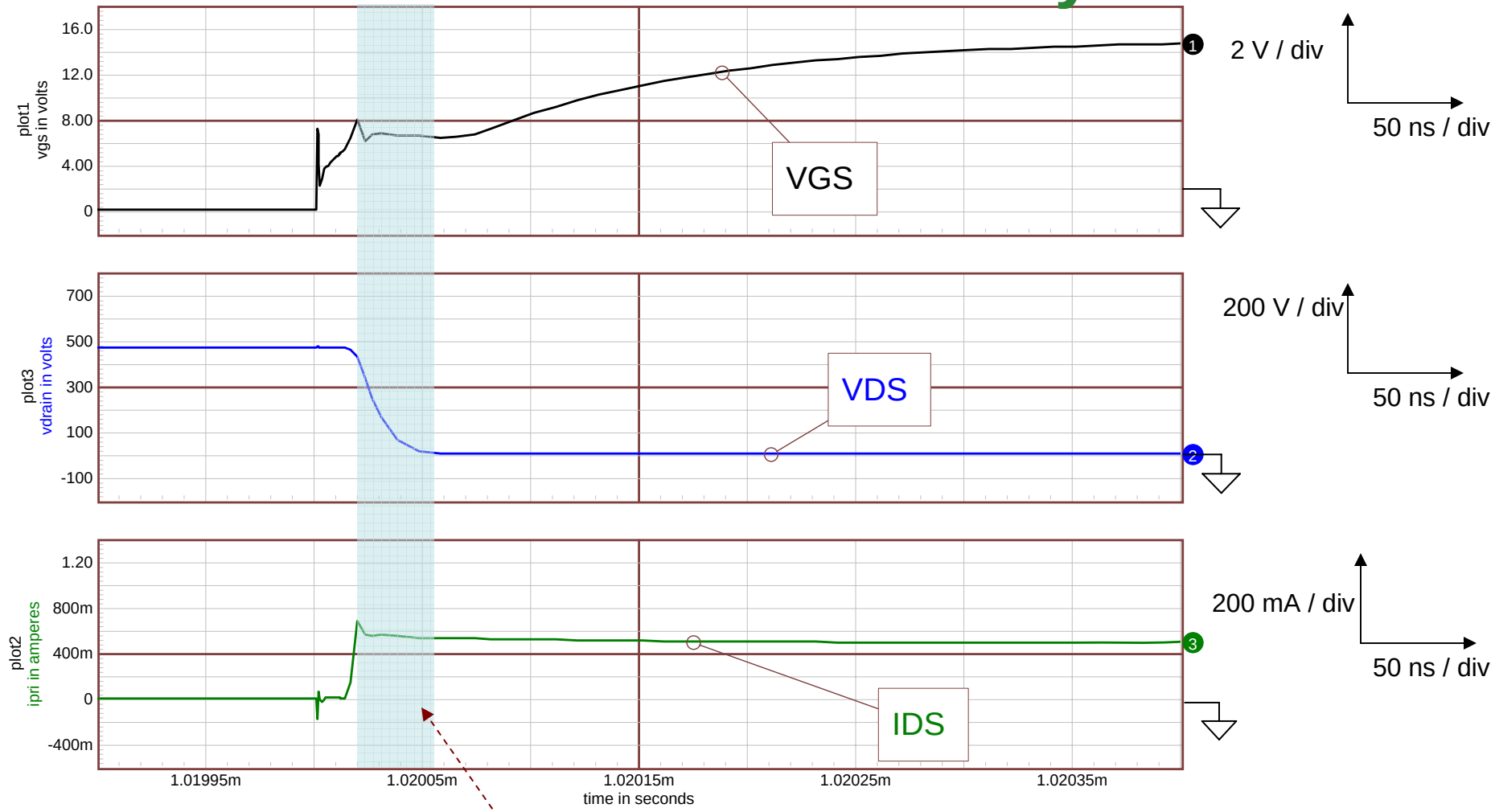
- Stages 2 and 3 dominate the switching losses of MOSFET and driver.
- DRV's sink capability as V_{GS} is around $V_{GS,Miller}$ is important.

Simulation Circuit of Flyback



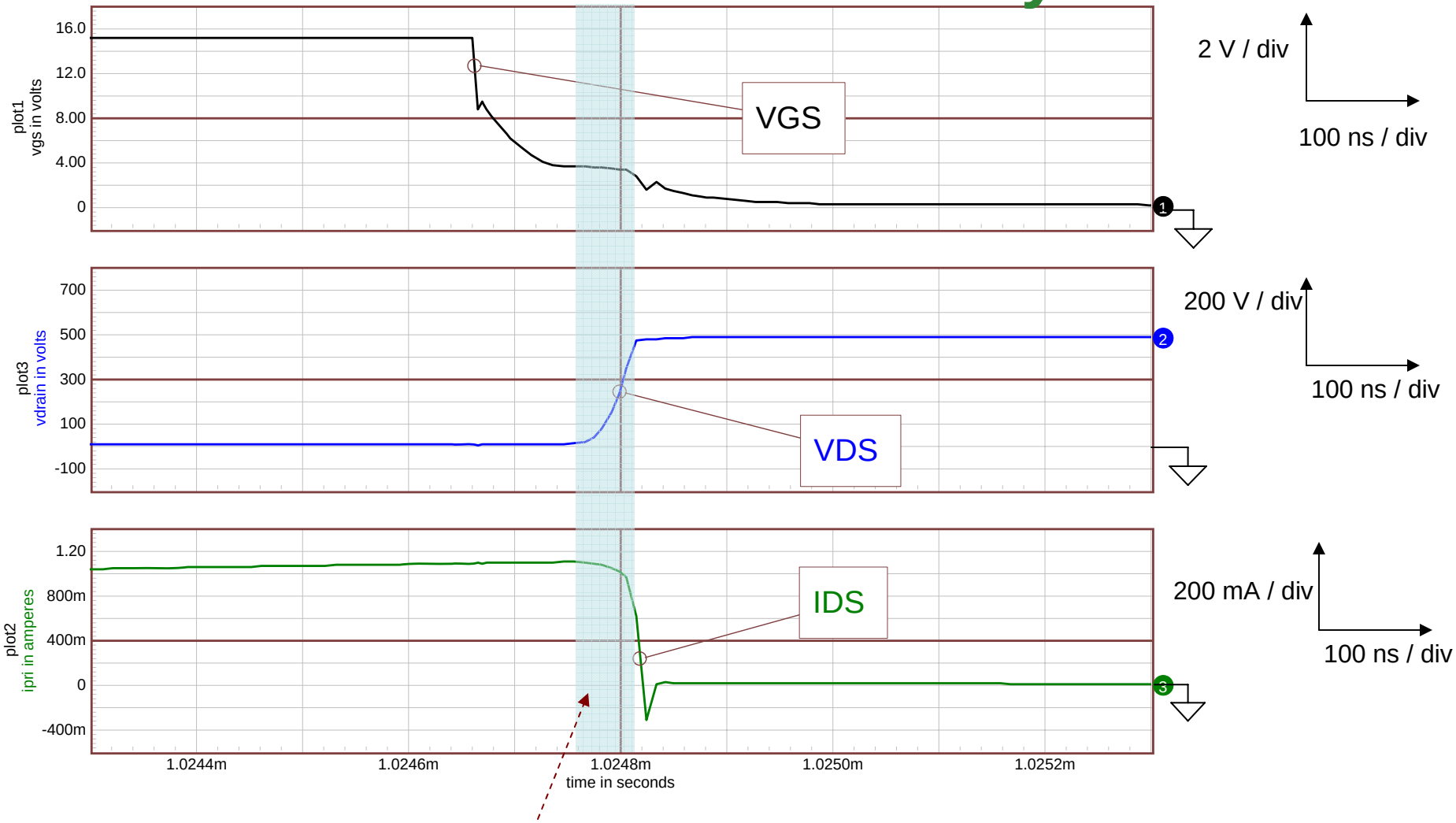
- Simulate the V_{GS}, V_{DS}, and I_{DS} on Flyback.

Turn-on Simulation of Flyback



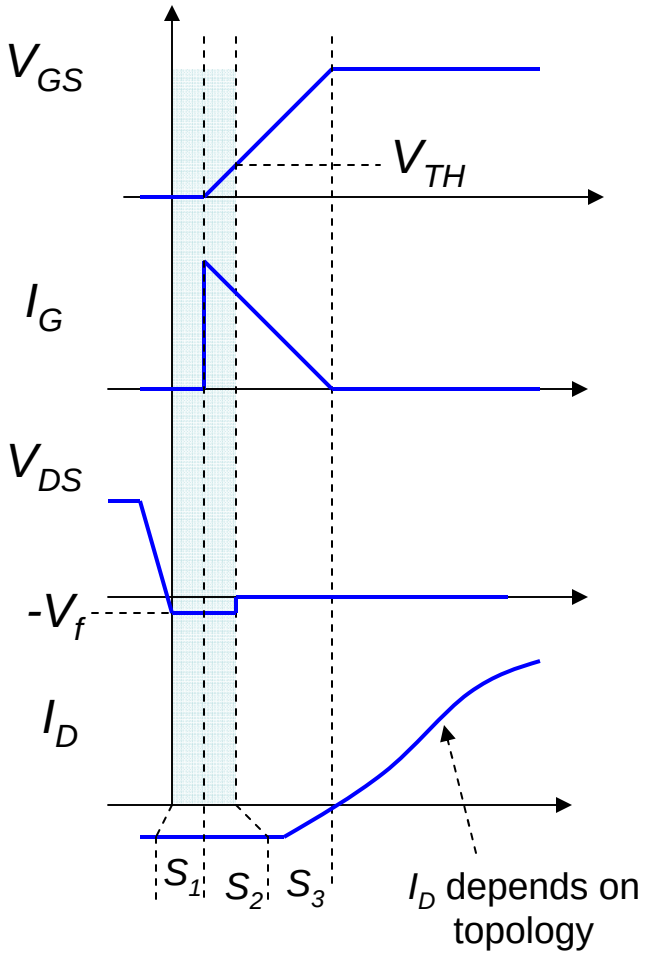
- V_{GS} rises with Miller effect.

Turn-off Simulation of Flyback



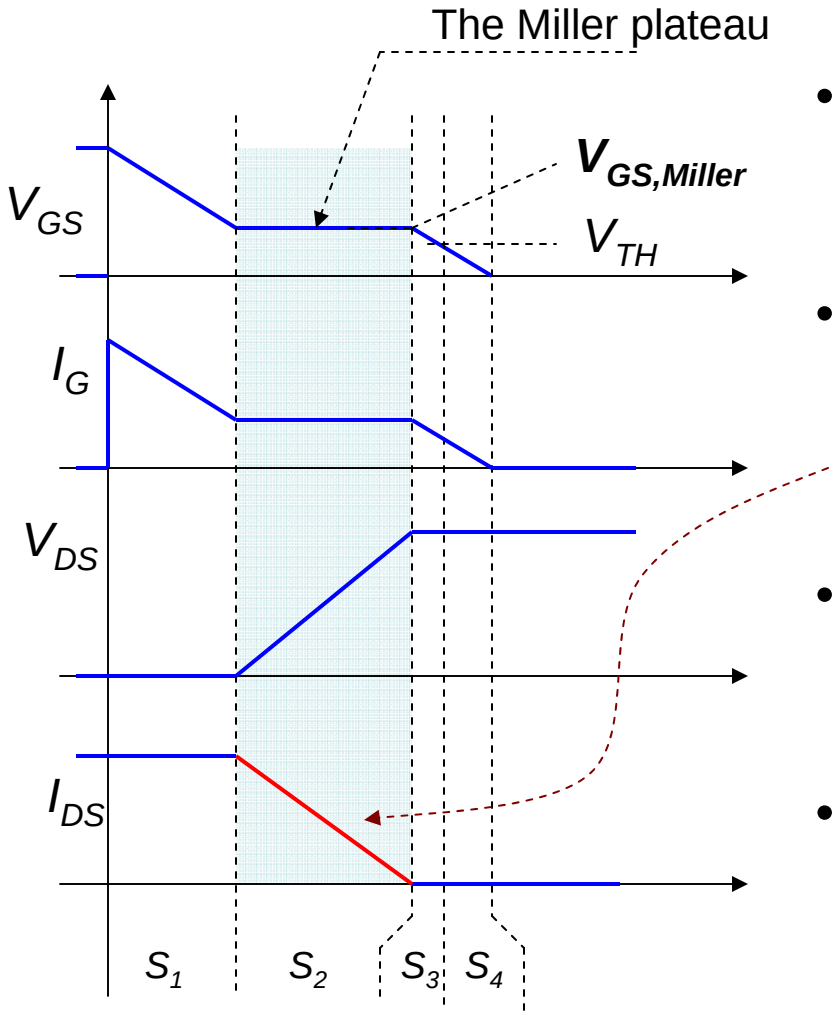
- Turn off with Miller effect.

Turn-on Procedure for Soft-switching



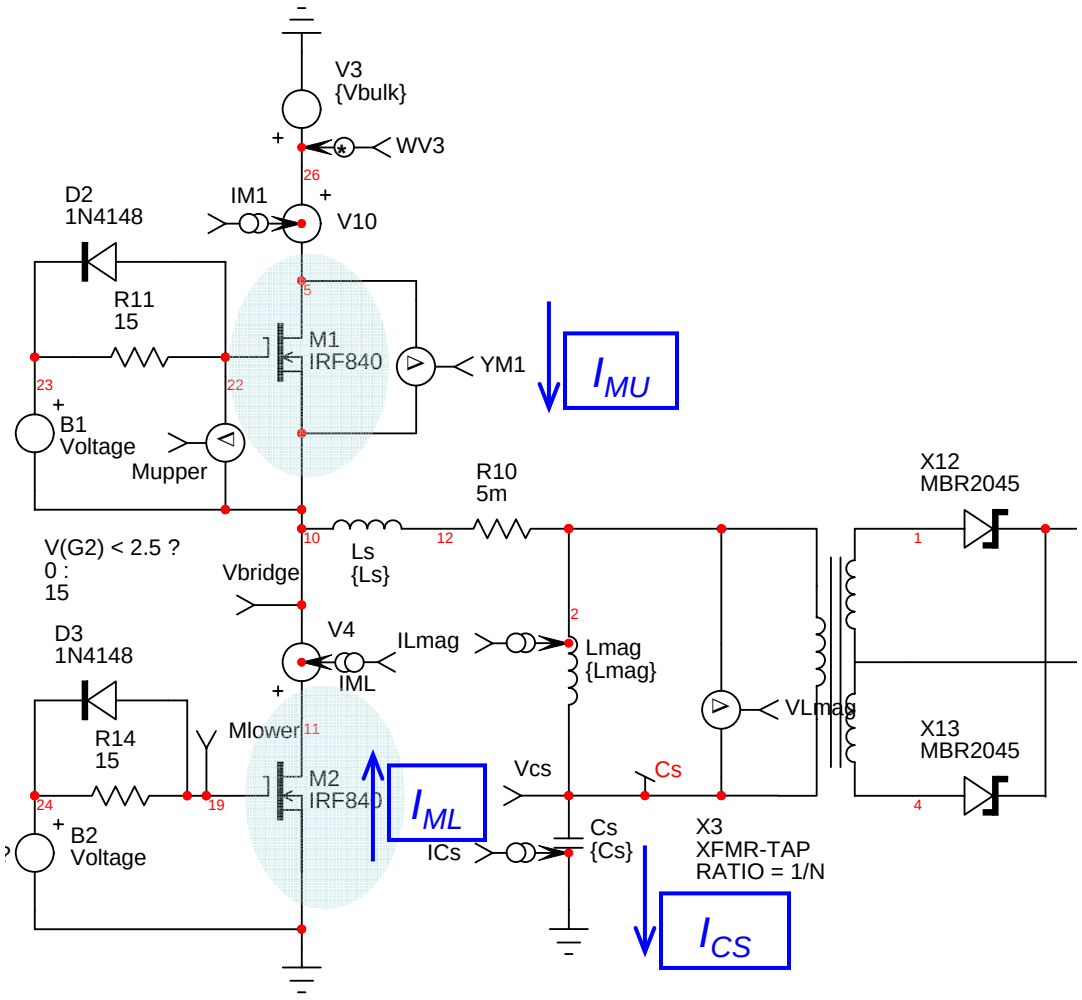
- Because of ZVS, there is no Miller effect as turning on.
- The switching losses are dominated by
  - The dead time (to reduce S_1), and
  - Source capability to charge C_{GS} to reduce S_2
- Less driver capability requirement.

Turn-off Procedure for Soft-switching



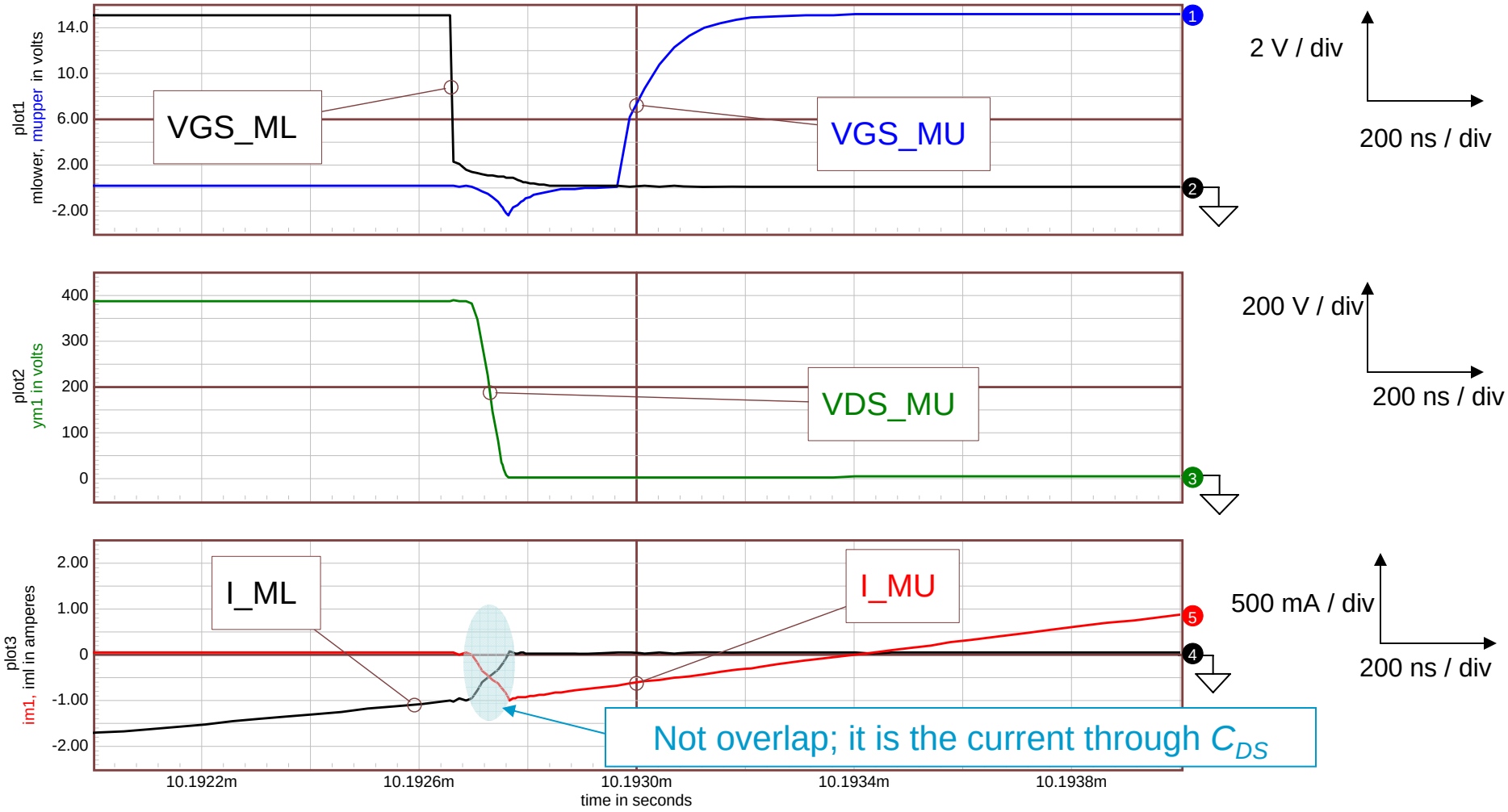
- Similar as hard-switching: The Miller plateau exists as turning off.
- The difference is that I_{DS} also reduces at this duration since I_{DS} will go through the opposite MOSFET as V_{DS} changes.
- To avoid overlap between 2 MOSFETs, minimize the duration of S_1 ~ S_4.
- Strong DRV's sink capability is needed.

Simulation Circuit of LLC-HB



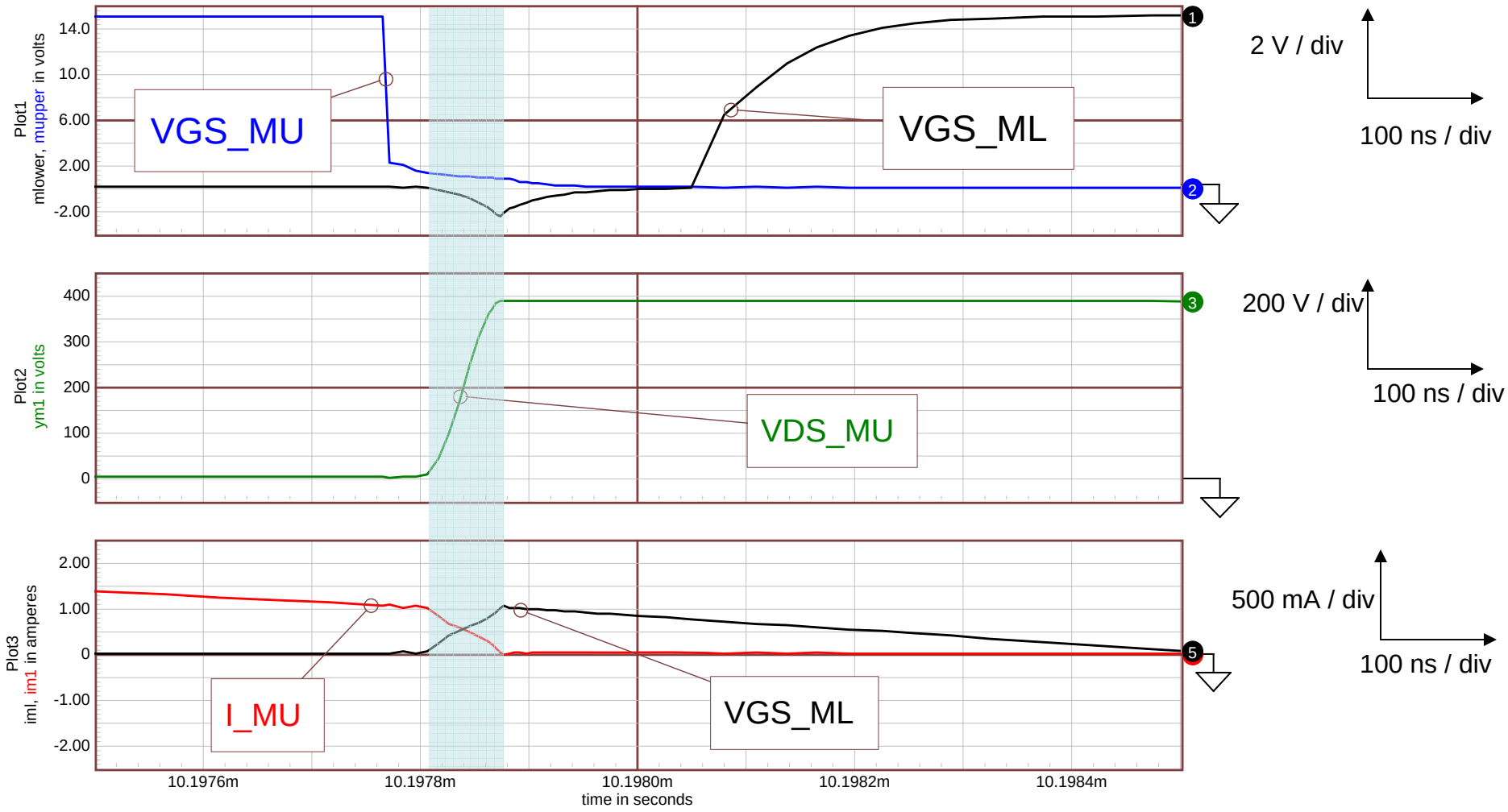
- Simulate the V_{GS_MU}, V_{DS_MU}, and I_{MU} on LLC-HB
- To ease the reading of current, the direction of I_{MU} and I_{ML} is referred to I_{CS}.

Turn-on Simulation of LLC-HB



- V_{GS_ML} off, I_{CS} reduces V_{DS_MU} for ZVS.
- V_{DS_MU} is 0 V BEFORE V_{GS_MU}, so V_{GS_MU} rises smoothly.

Turn-off Simulation of LLC-HB



- Strong turn off capability is required.

Driver Comparison between Hard-Switching and Soft-Switching

	Hard-switching	**Soft-switching**
Source capability requirement	Medium	Low
Sink capability requirement	High	High
Dead time accuracy requirement	Accurate	Accurate

The Solutions for High-Side Driver

- Transformer-based solution
  - Single DRV input
  - Dual DRV inputs
- Silicon integrated circuit driver: dual outputs
  - Single DRV input
  - Dual DRV inputs

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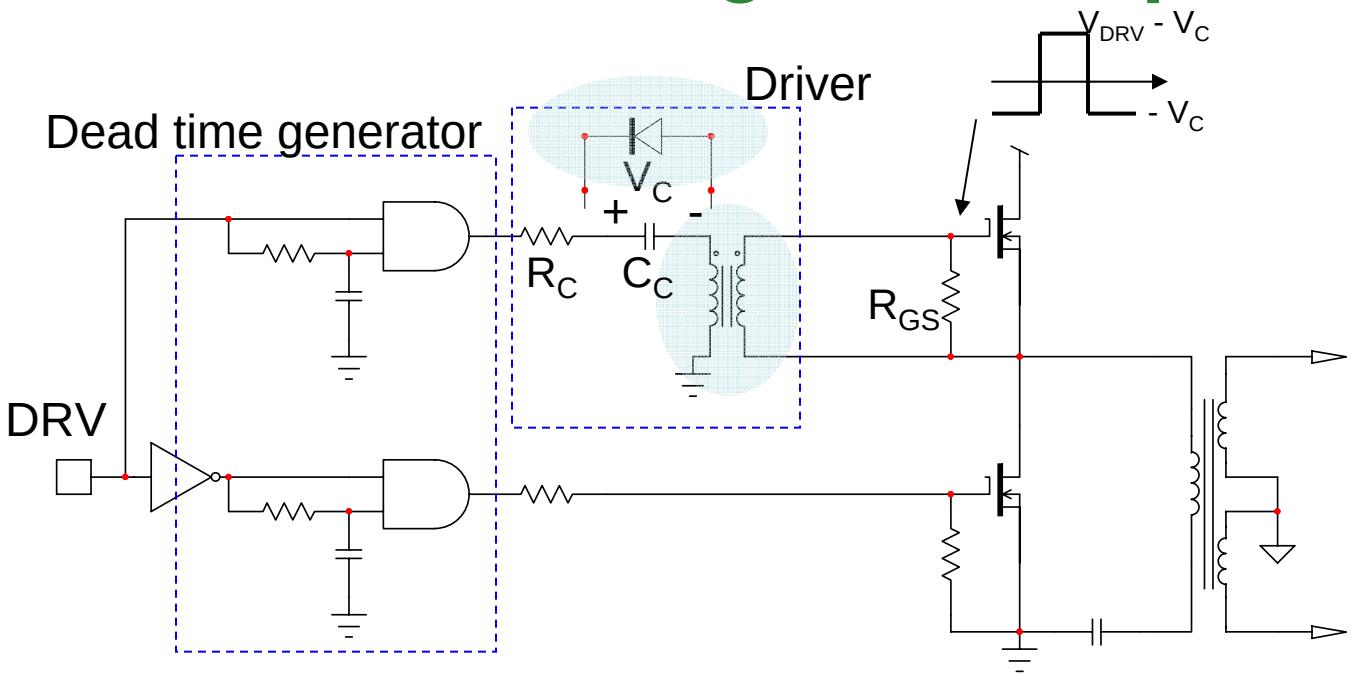
Consideration as Designing Driver Transformer

- Ground-referenced floating drive – keep 500 V isolation if a 400 V pre-regulated PFC exists.
- Minimize the leakage inductance - the delay between output and input windings may kill the power MOSFETs.
- Follow Faraday's law – keep V*T constant, otherwise, saturate.
- Keep enough margin from saturation – the worst case happens with transient load at high line.
- High permeability ferrite – minimize the I_M.
- Keep high sink current capability

Single DRV Input



$$V_C = DV_{DRV}$$

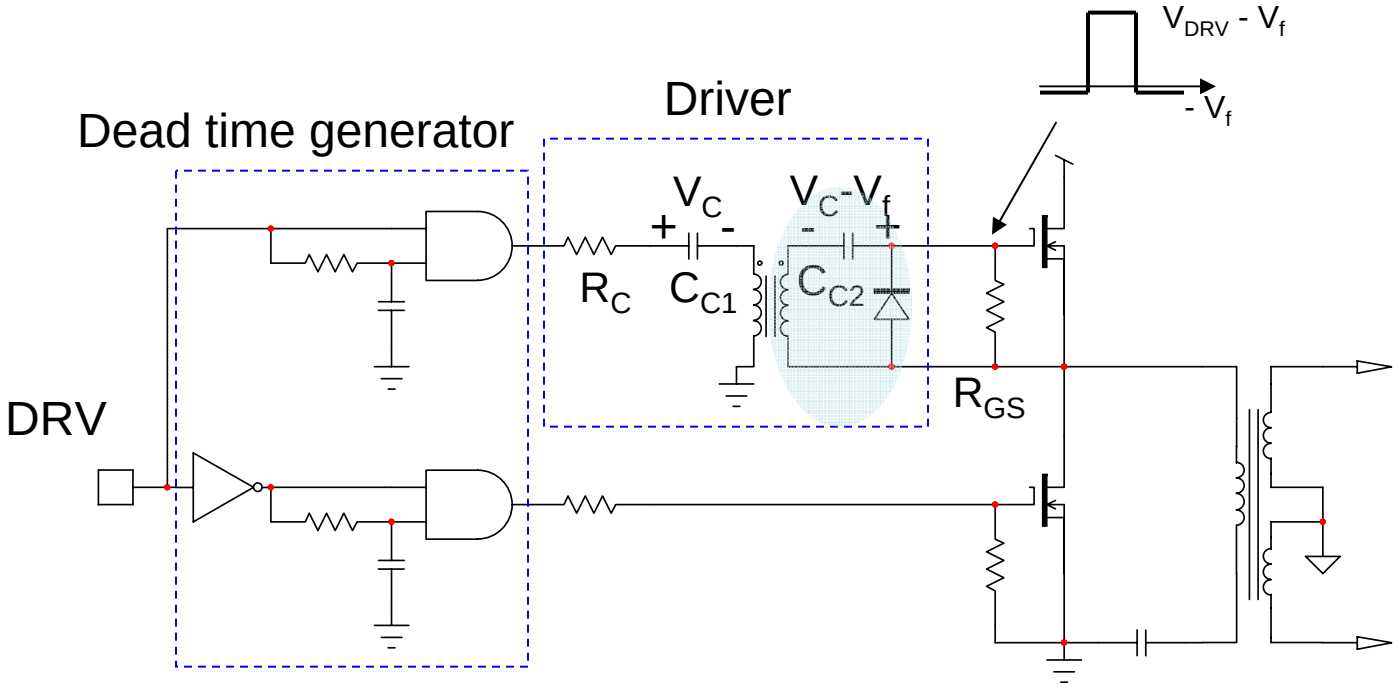
$$Q > \frac{1}{R_C}\sqrt{\frac{L_M}{C_C}} = 0.5$$

$$R_C \geq \frac{1}{Q}\sqrt{\frac{L_M}{C_C}} = 2\sqrt{\frac{L_M}{C_C}}$$

C_C to reset the driver transformer and R_C to damp the *L*-*C* resonance.

- An ac coupling capacitor (C_C) is needed to reset the driver transformer flux.
- The amplitude of V_{GS} is dependent on duty. ☹
- With ($-V_C$) to turn off at steady state, but the sink capability is limited at start-up. ☹
- Need a fast time constant (L_M//R_{GS} * C_C) to avoid flux walking due to the fast transient.
- Watch out the ringing between C_C and drive transformer at skip mode or UVLO, a diode is needed to damp the ringing.

Single DRV Input with DC Restore

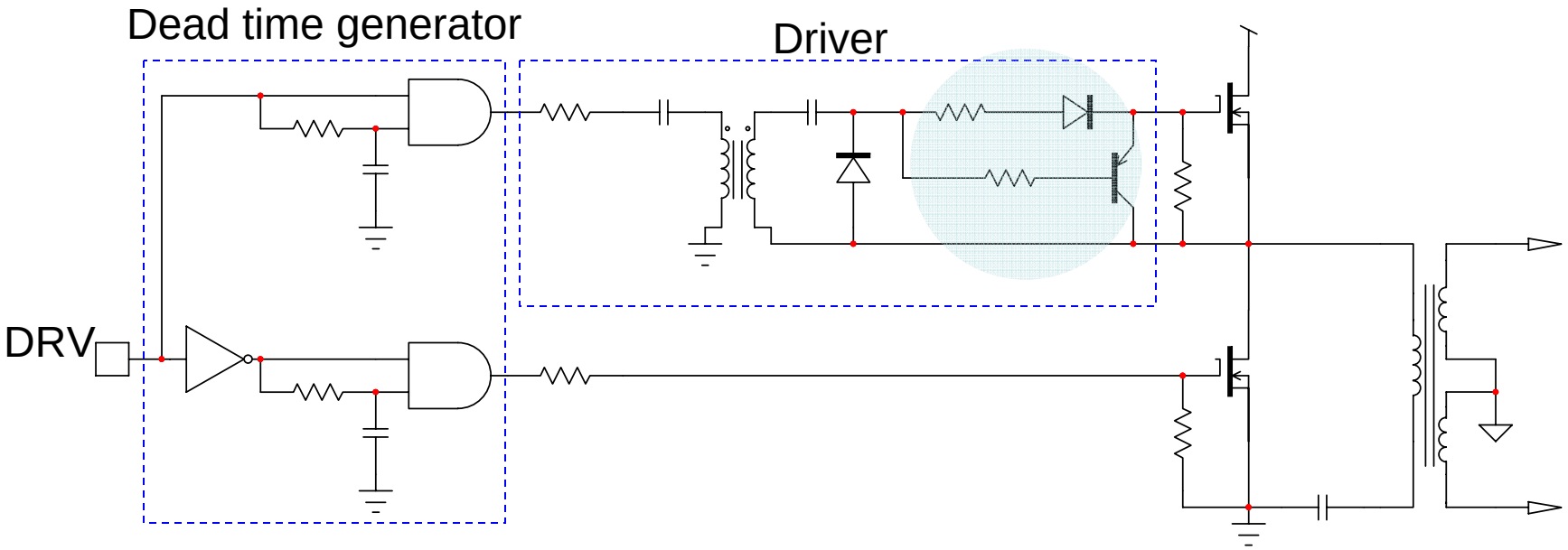


$$V_C = DV_{DRV}$$

$$R_C \geq 2\sqrt{\frac{L_M}{C_C}}$$

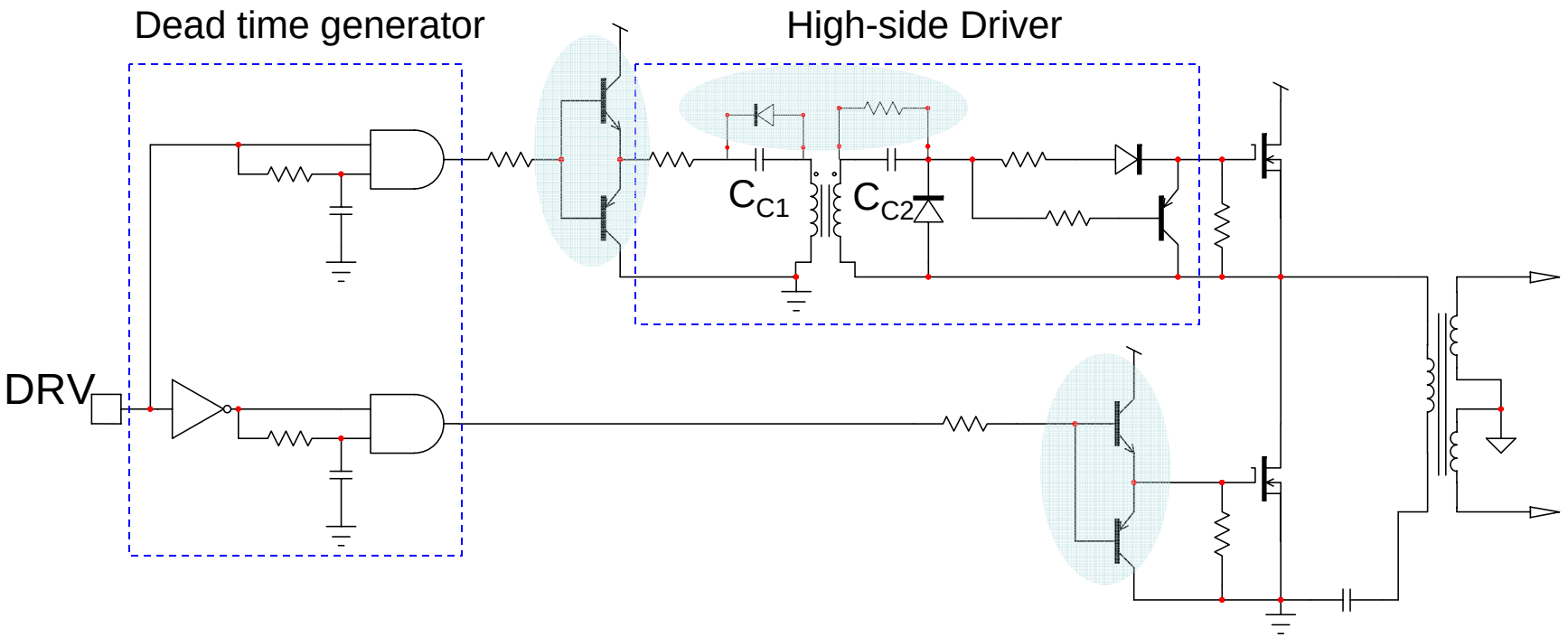
- V_{GS} amplitude is independent on duty ratio at steady state.
- Limited sink capability. ☹

Single DRV Input with PNP Turn-Off



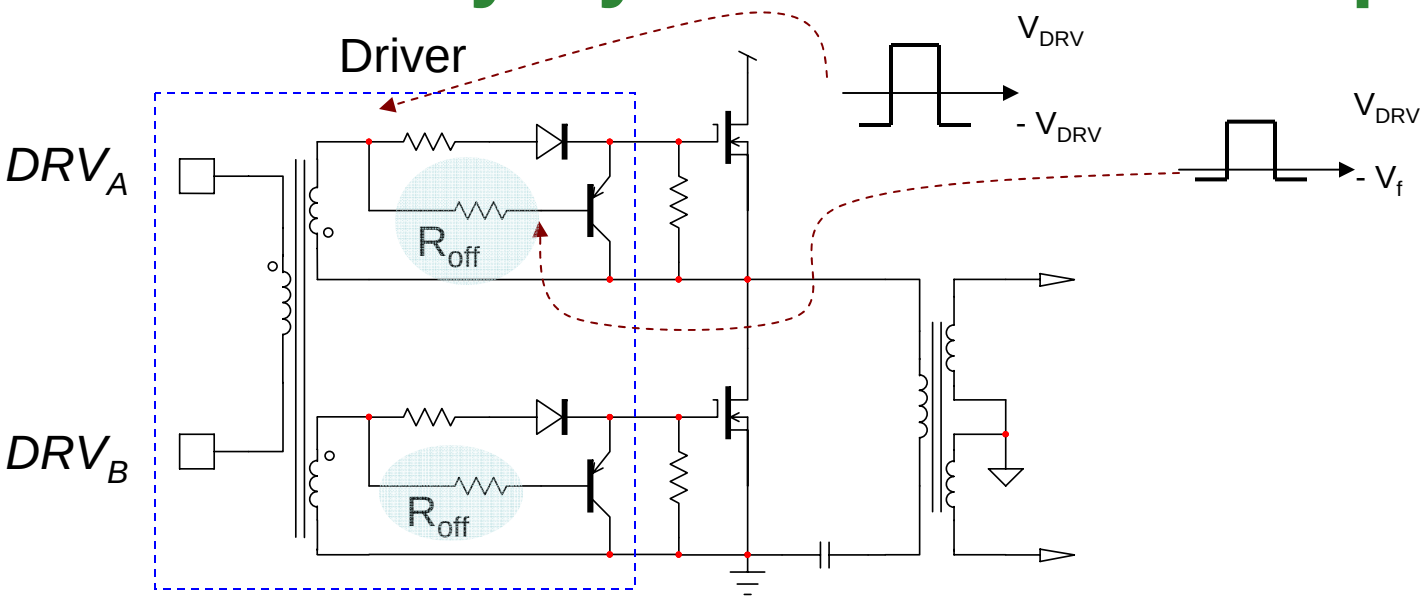
- A pnp transistor + diode help to improve the switching off.

Don’t Forget the AND Gate



- Add the totem-pole drivers if output capability of AND gate is limited.
- Is the design finished?
  ➔ No, not yet. Pay attention to the ringing among C_{C1}, C_{C2} and driver transformer when skip or UVLO. A diode and resistor to damp the ringing. ☹

Dual Polarity Symmetrical DRV Inputs



- DRV_A and DRV_B are opposite-polarity and symmetrical ➔ no ac coupling capacitor.
- This is suitable for push-pull type circuit, e.g. LLC-HB, but NOT for asymmetrical type, e.g. AHB or active clamp. ☹
- Pay attention to the flux of driver transformer at line/load transient.
- The strong turn off capability is still needed. ☹
- Pay attention to the delay caused by the leakage inductance. ➔ minimize the leakage inductance and use dual output windings instead of single output winding.
- Extra losses caused by voltage drop on R_{off}. ☹

The Driver Transformer

- Pros
  - A transformer is more robust than a die!
  - Less sensitivity to spurious noise and high dV/dt pulses
  - Cheap?

- Cons
  - Complicated circuits
  - Pay attention on extreme line/line condition & off mode ……
  - Pay attention on the leakage inductance and isolation
  - Is the sink capability strong enough?

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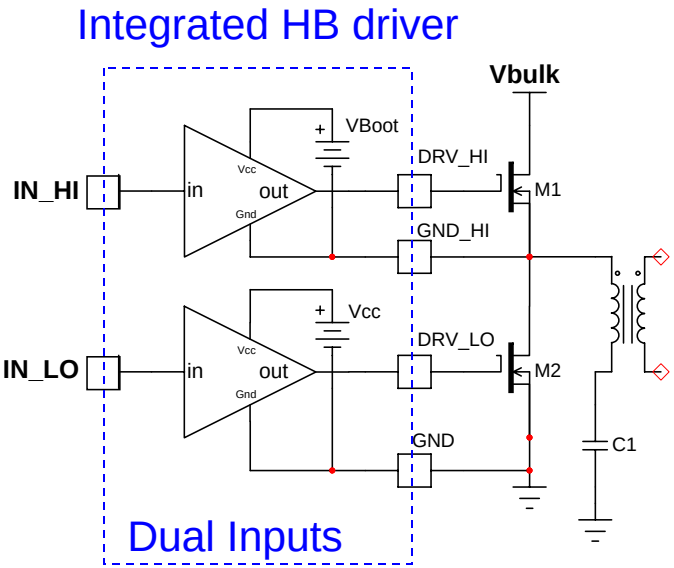
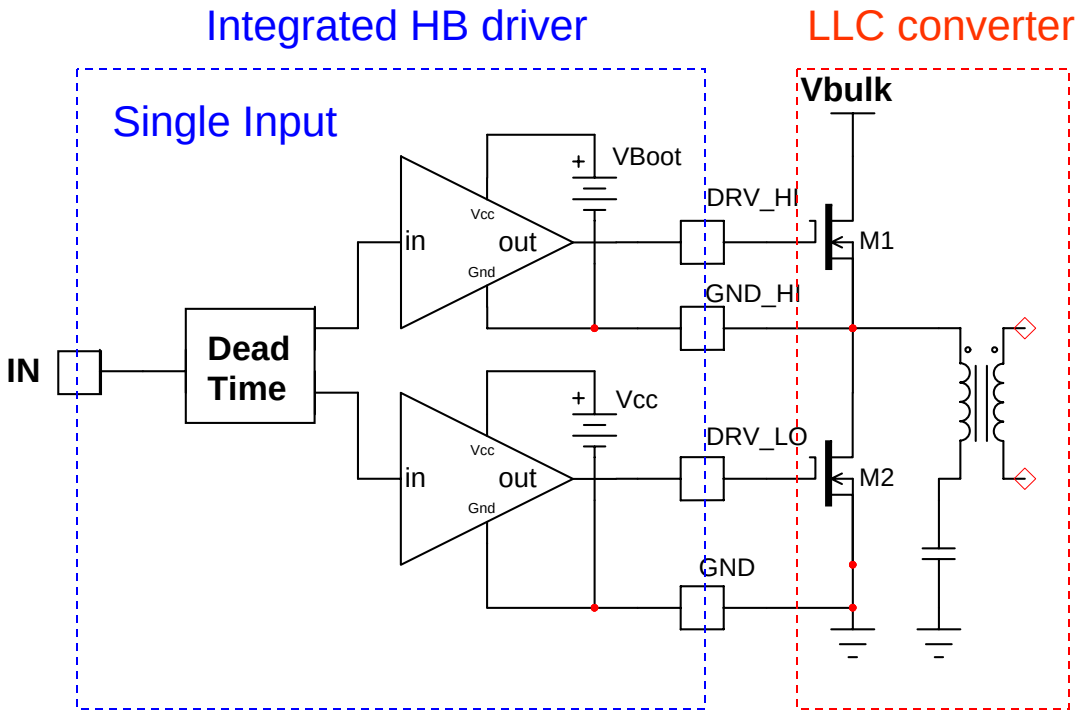
Silicon Half Bridge Driver Principle

- Principle
  - Single or dual inputs
  - High & low side driver

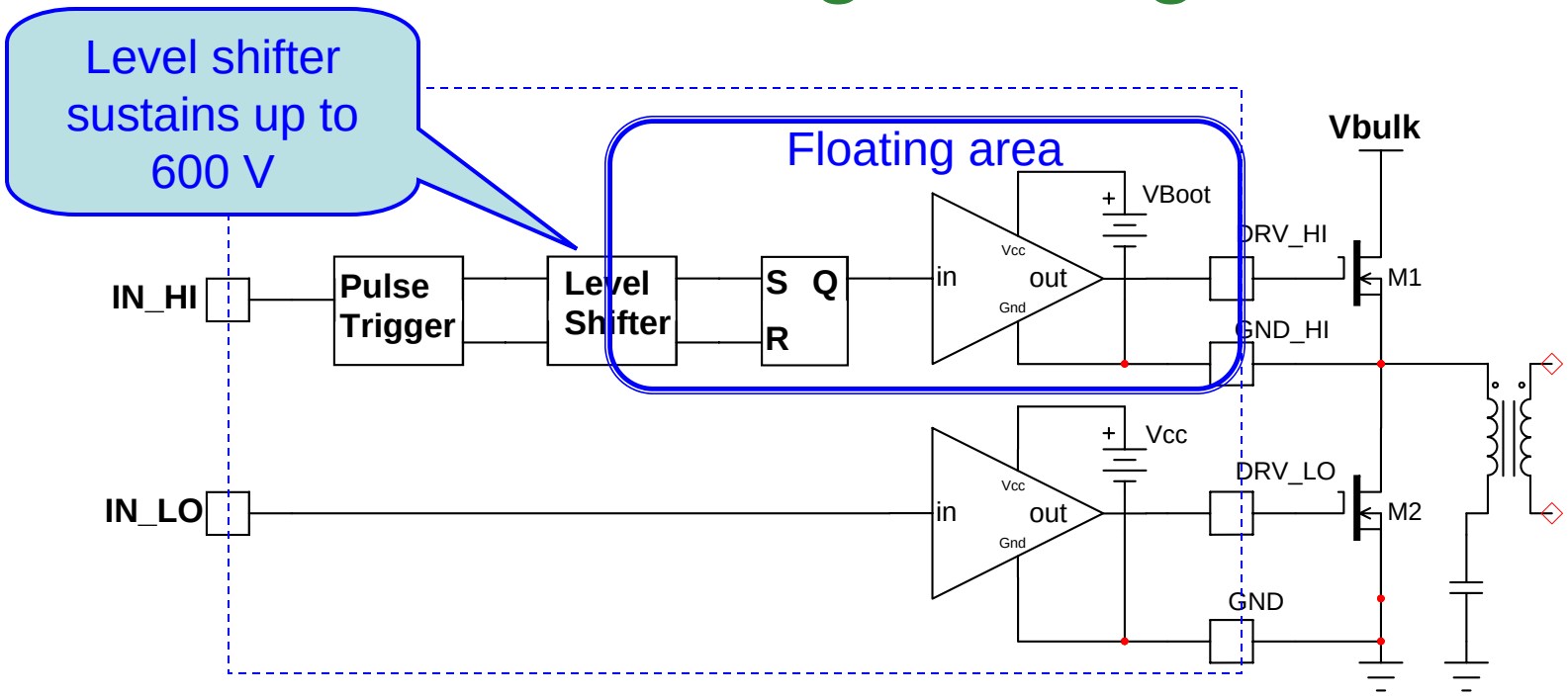




Silicon Solution, What are its Limits?

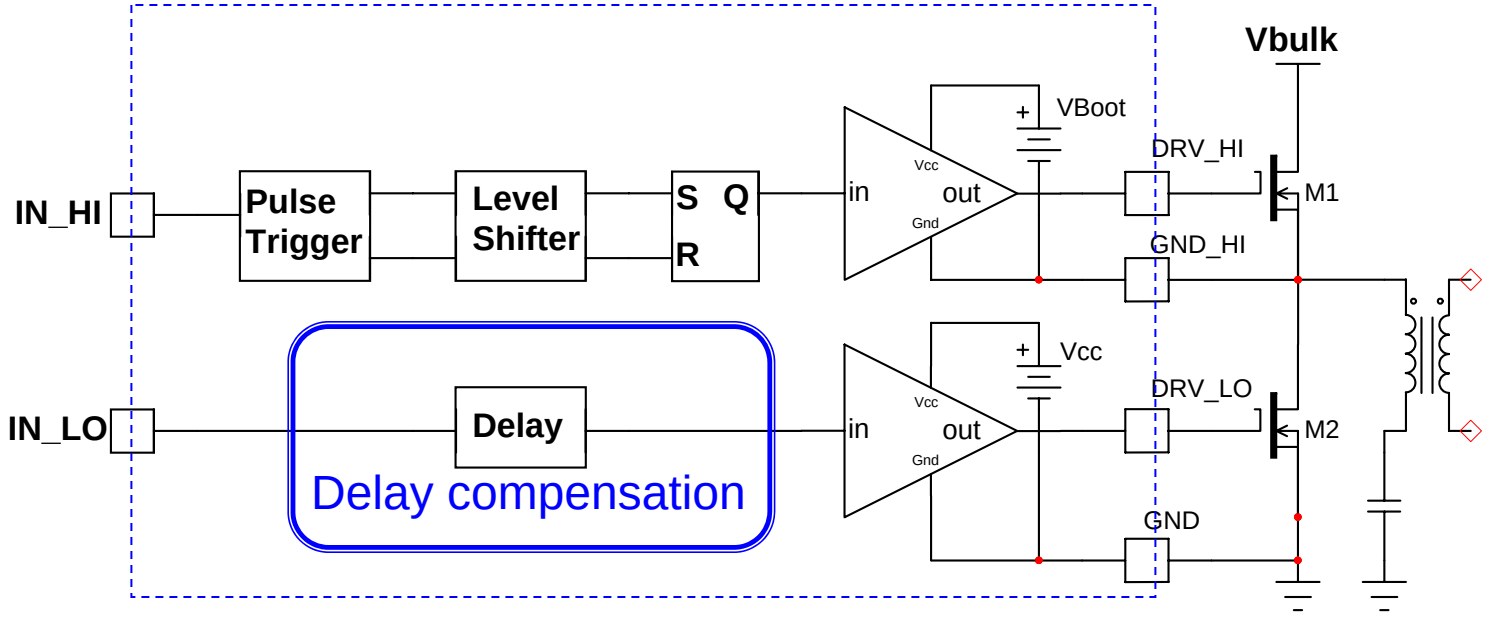
- High-side isolation – 600 V is reached within the silicon.
- Matched propagation delay between high and low side drive – Prevents any unbalanced transformer usage.
- High side driver supply – Bootstrap supply is requested.
- Noise immunity – Negative voltage robustness of the high side driver.

Silicon Solution, High Voltage Isolation



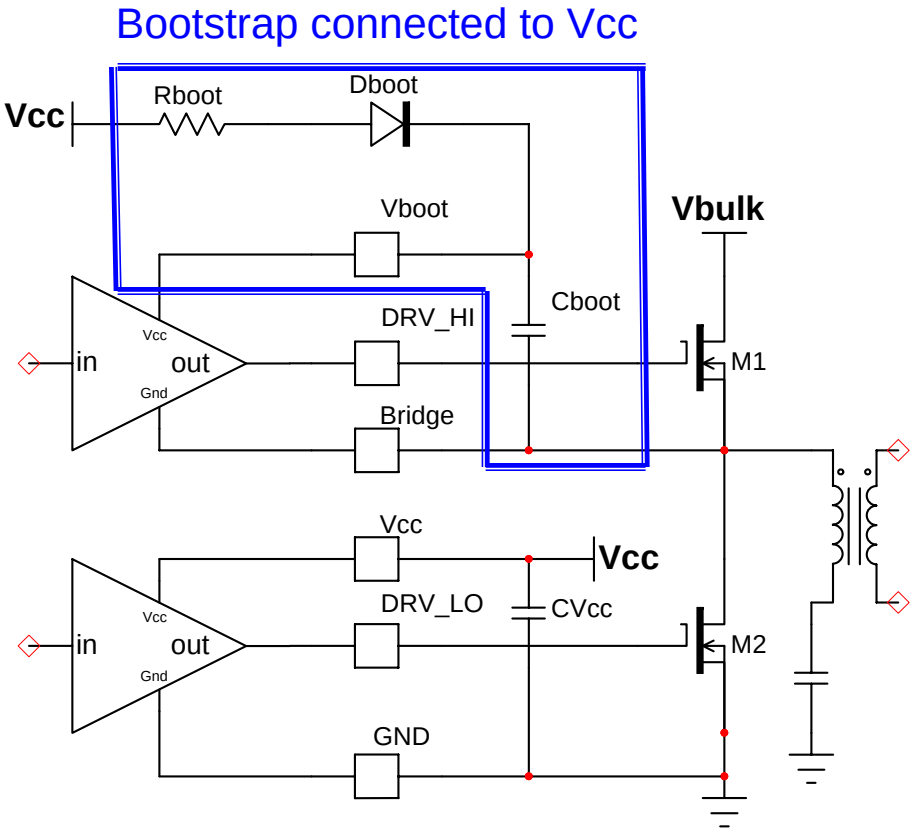
- Pulse trigger: generates pulse on each edge from IN_HI input.
- Level shifter: shifts pulses from GND reference to GND_HI reference.
- SR flip flop: latches pulses information from the level shifter.

Silicon Solution, Matched Propagation Delay



- Delay is inserted on the fastest path: Low side driver path
  - ➔ to compensate: Pulse trigger + level shifter and SR flip-flop delays.

Silicon Solution, High Side Driver Supply



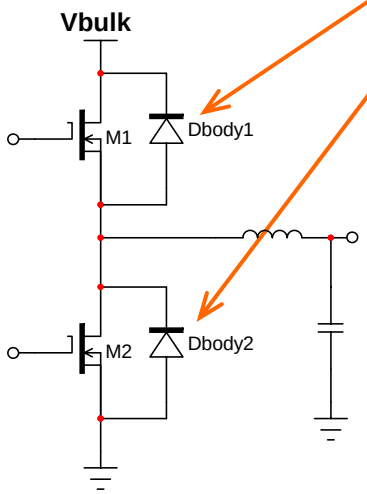
Bootstrap Step:

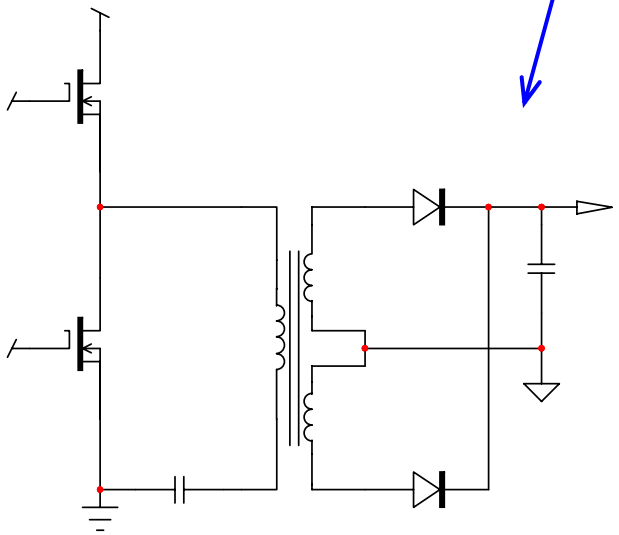
- Step 1: M_2 is closed ➔ C_{boot} is grounded: C_{boot} is refueled via V_{cc}.
- Step 2: M_1 & M_2 are opened ➔ Bridge pin is floating, D_{boot} is blocked & C_{boot} supplies floating area.
- Step 3: M_1 is closed ➔ bridge pin moved to bulk level, D_{boot} is still blocked & C_{boot} supplies floating area.

- Bootstrap technique is used for supplying the high side driver

Root of High Side Driver Negative Voltage?

- Let's focus on the half-bridge branch:
  - the load connected to a half-bridge branch is inductive:
  - like an LLC-HB
  - Or with the most simple case in a synchronous buck (where body diodes of the mosfet are represented).

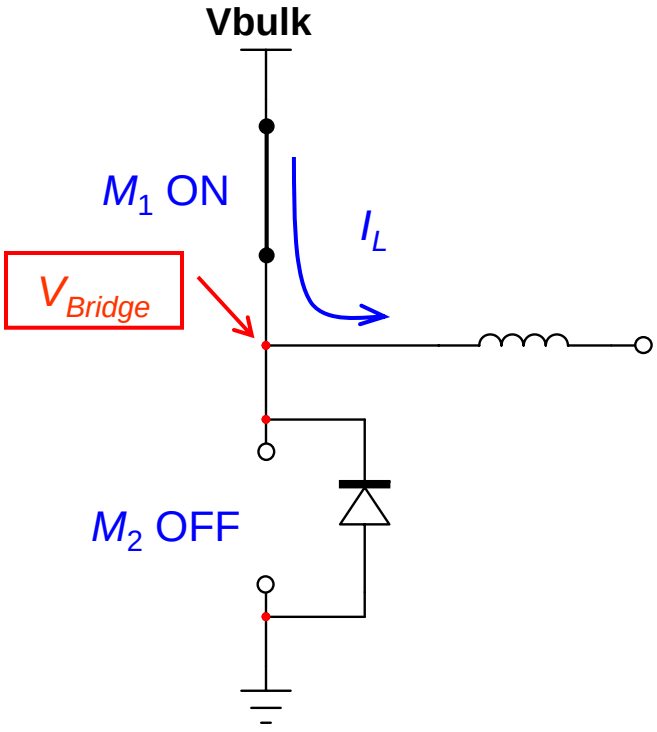




LLC-HB

Theory: Buck Converter Operation

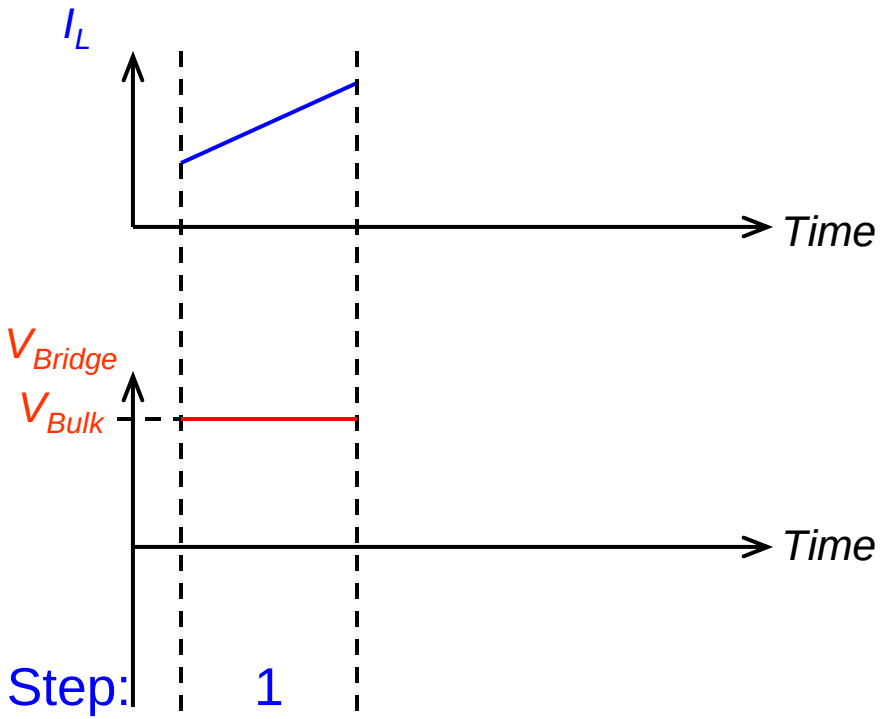
- 1st step of the buck converter:



Step 1:

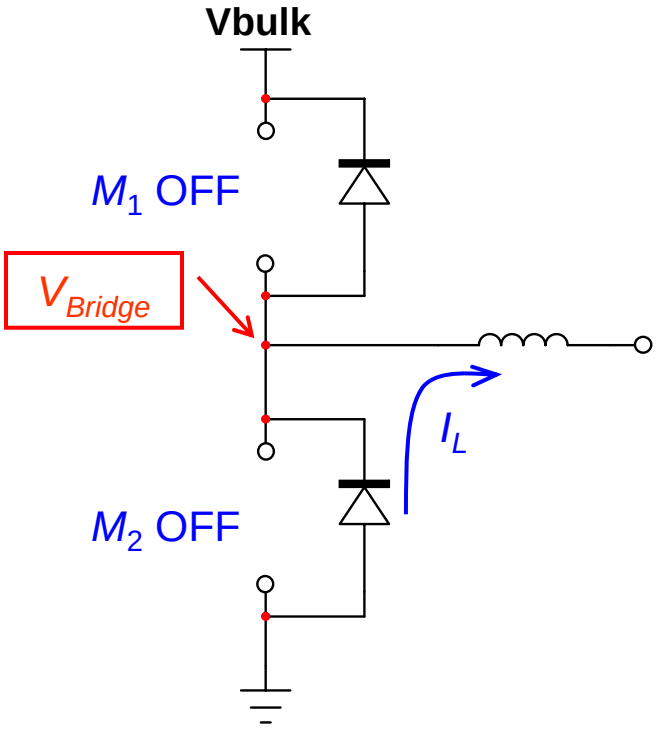
M_1 ON

M_2 OFF



Theory: Buck Converter Operation

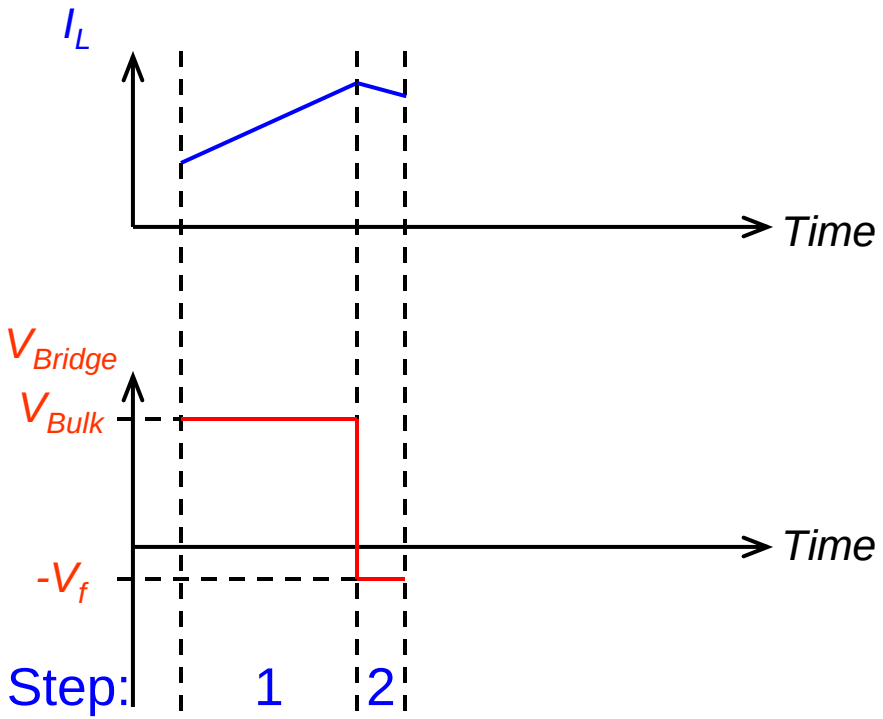
- 2nd step of the buck converter:



Step 2:

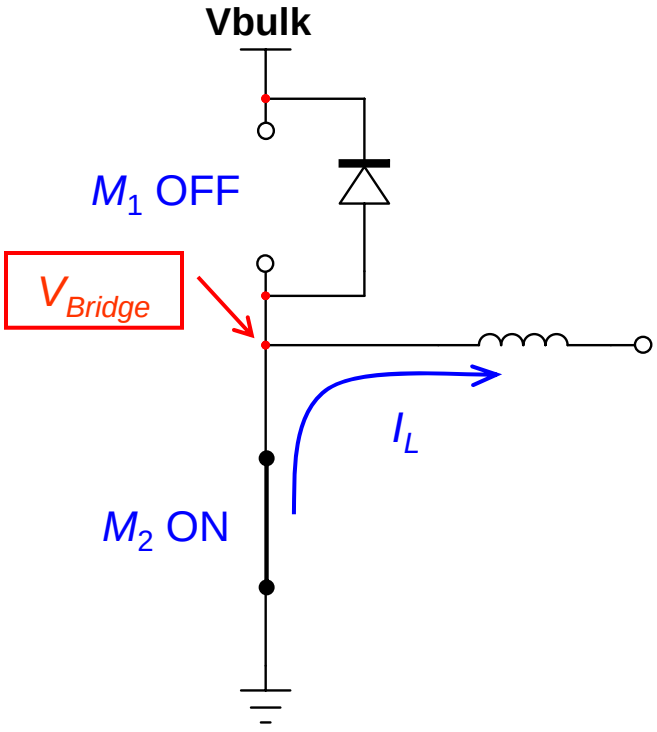
M_1 OFF

M_2 OFF



Theory: Buck Converter Operation

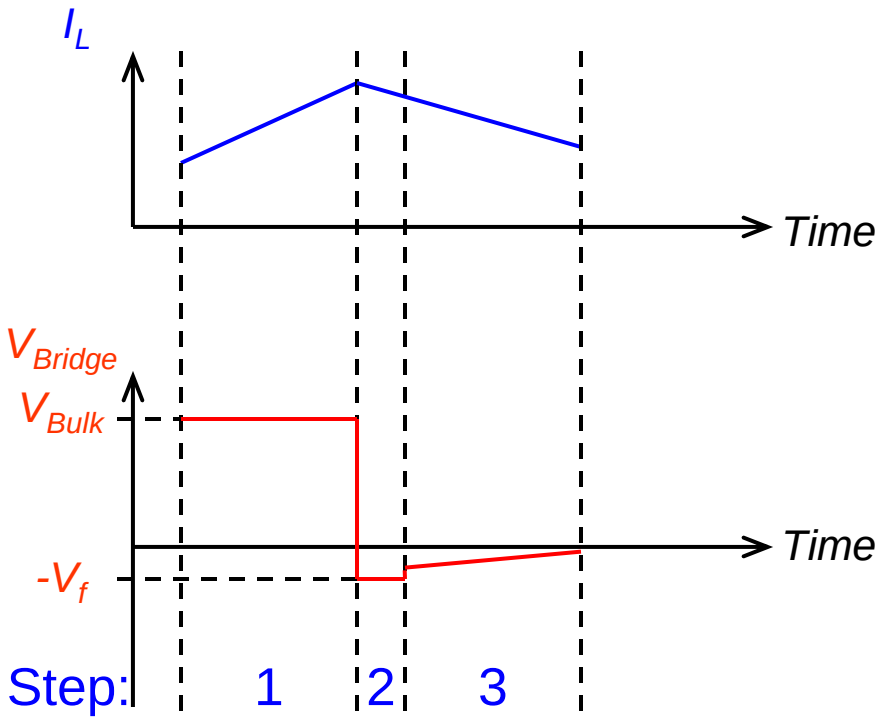
- 3rd step of the buck converter:



Step 3:

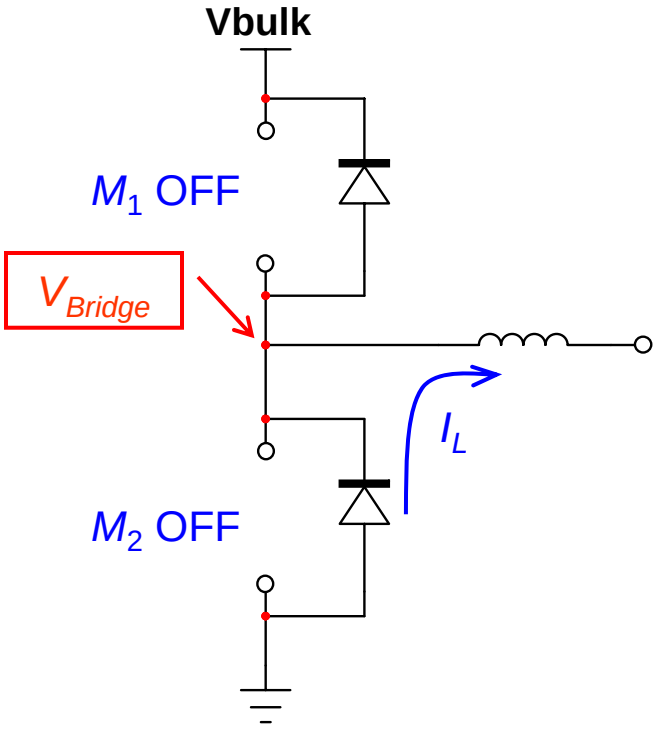
M_1 OFF

M_2 ON



Theory: Buck Converter Operation

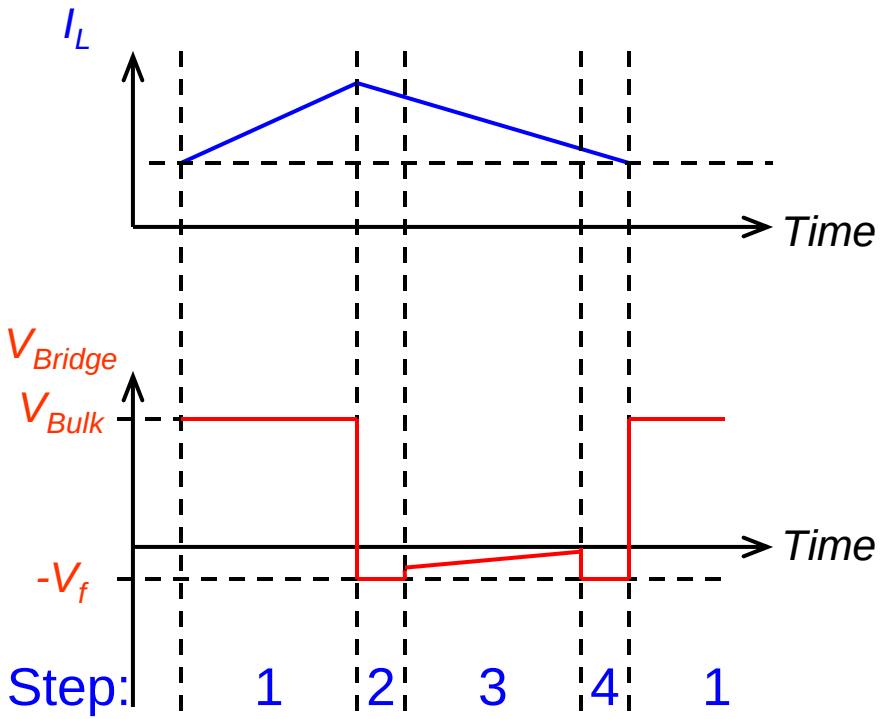
- 4th step of the buck converter:



Step 4:

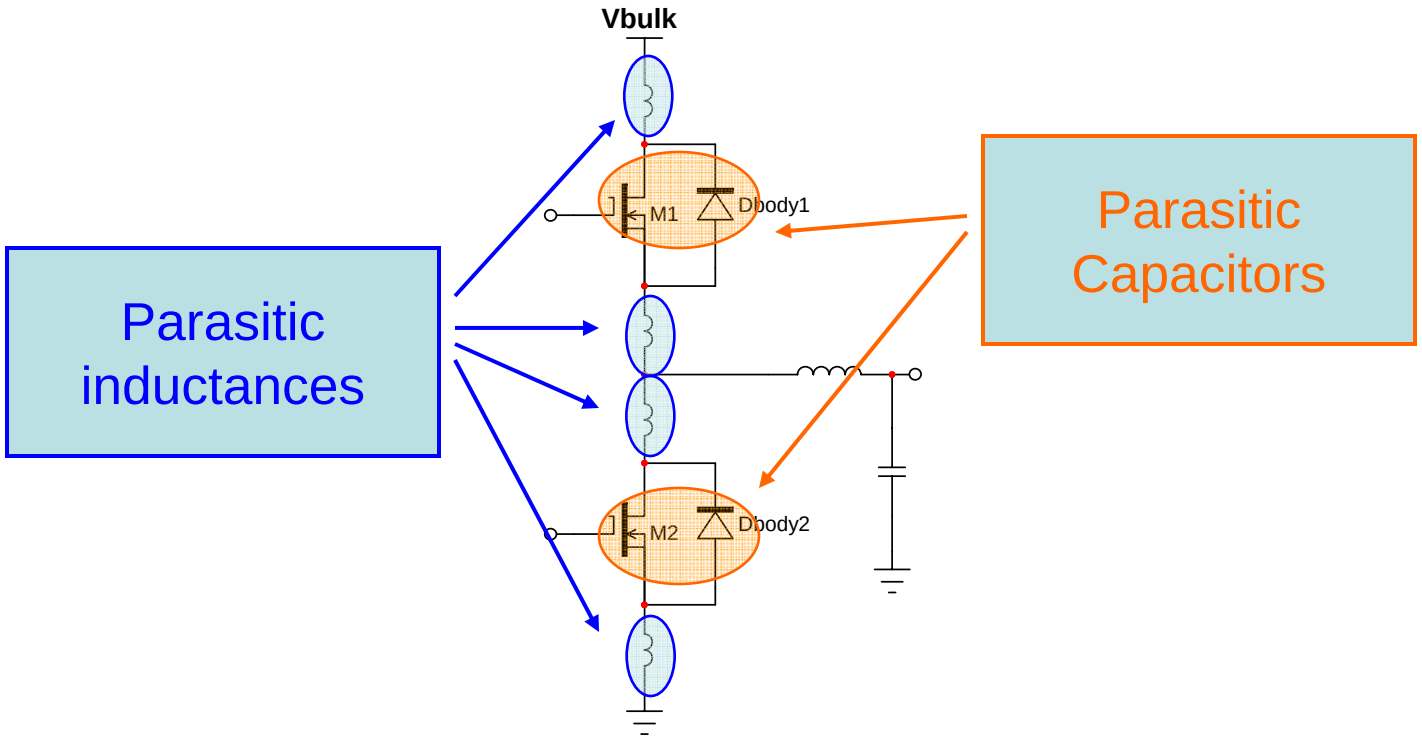
M_1 OFF

M_2 OFF



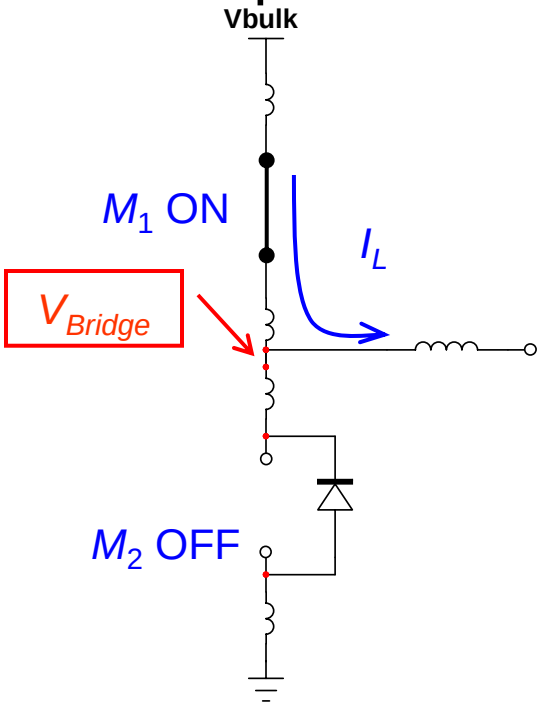
Bench: Buck Converter Operation

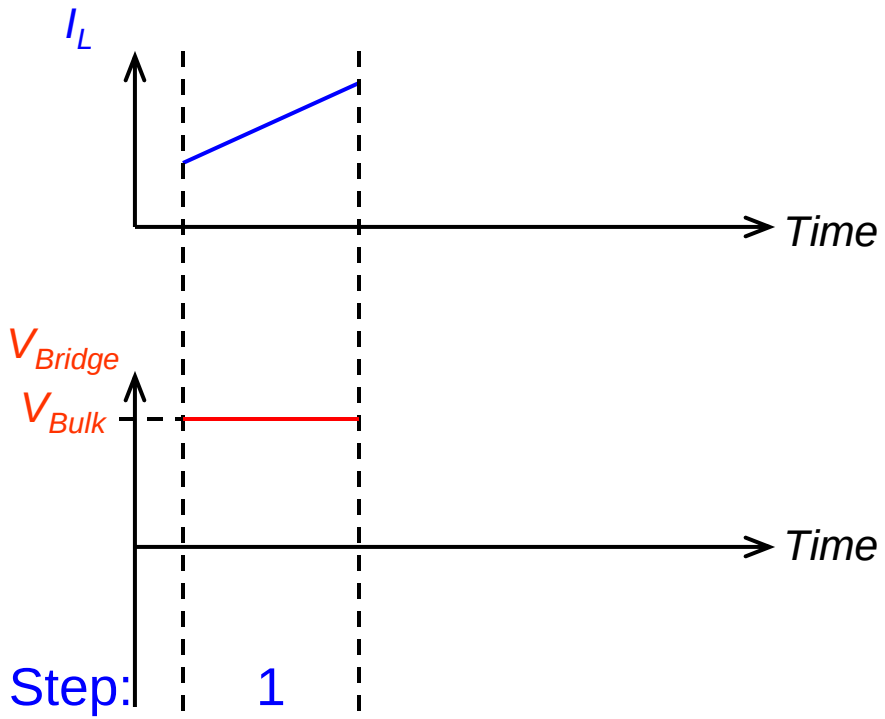
- Anywhere but in a ppt file there are parasitic elements:
  - True buck converter:



Bench: Buck Converter Operation

- 1st step of the buck converter:





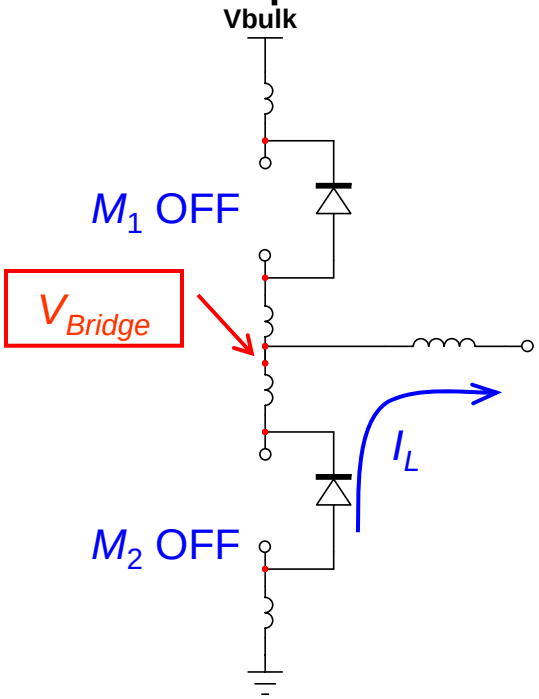
Step 1:

M_1 ON

M_2 OFF

Bench: Buck Converter Operation

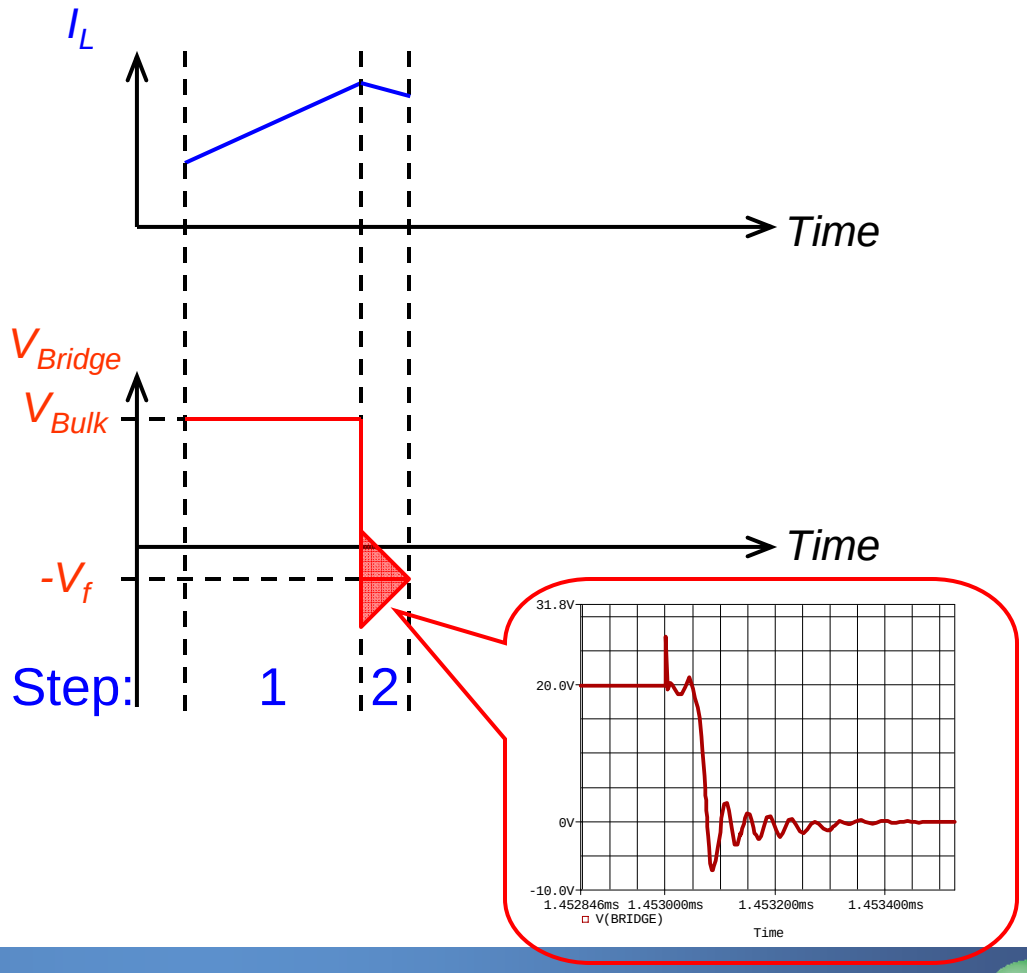
- 2nd step of the buck converter:



Step 2:

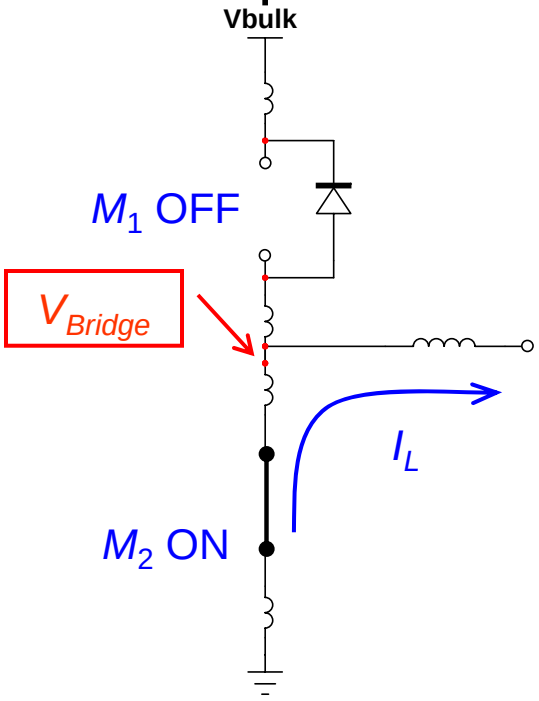
M_1 OFF

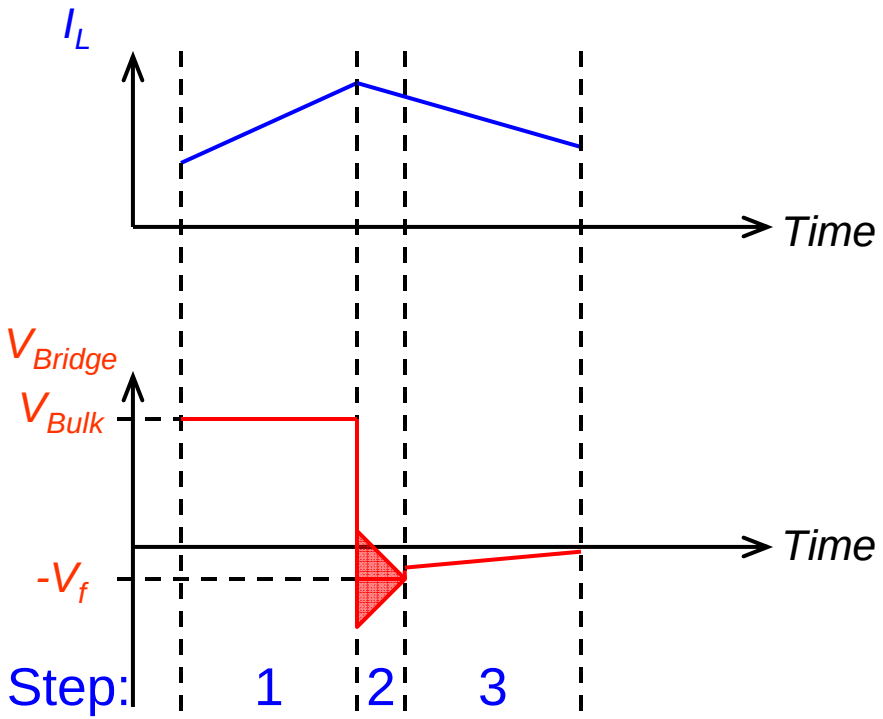
M_2 OFF



Bench: Buck Converter Operation

- 3rd step of the buck converter:





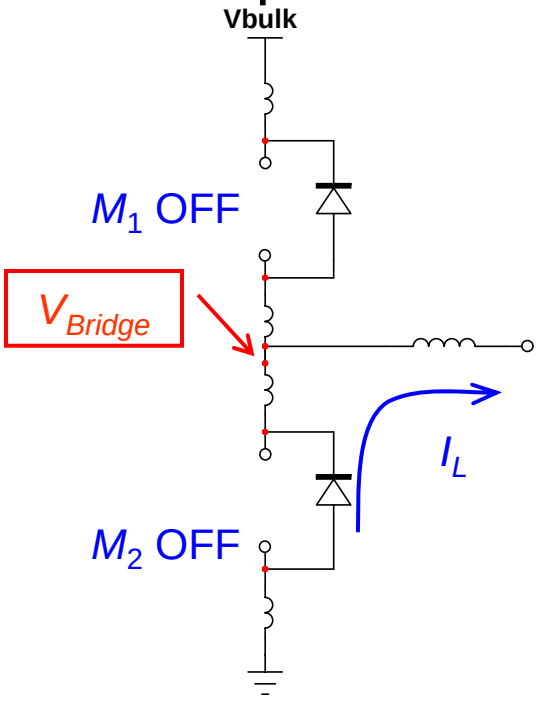
Step 3:

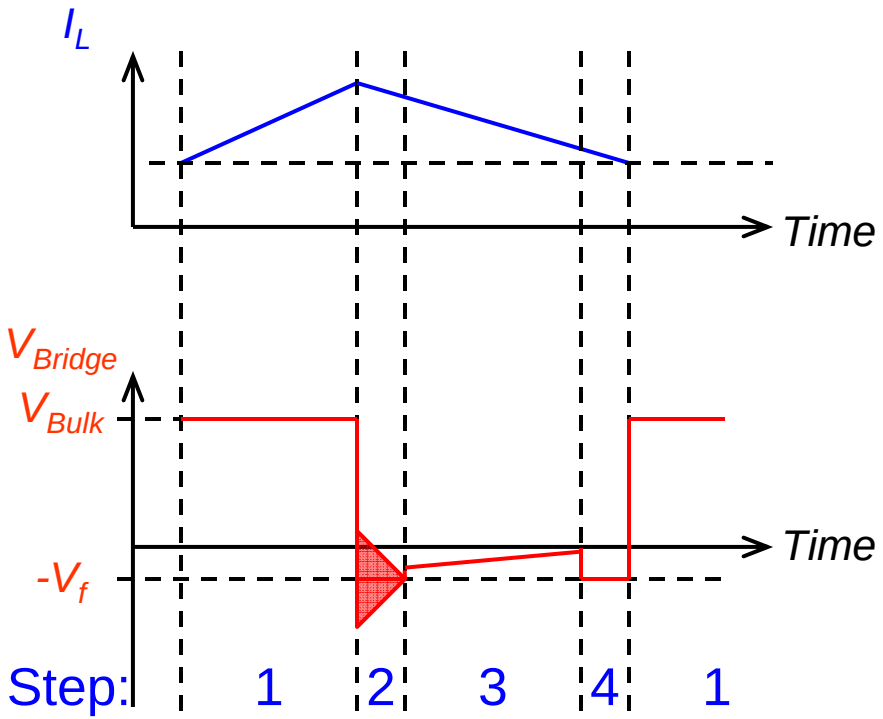
M_1 OFF

M_2 ON

Bench: Buck Converter Operation

- 4th step of the buck converter:





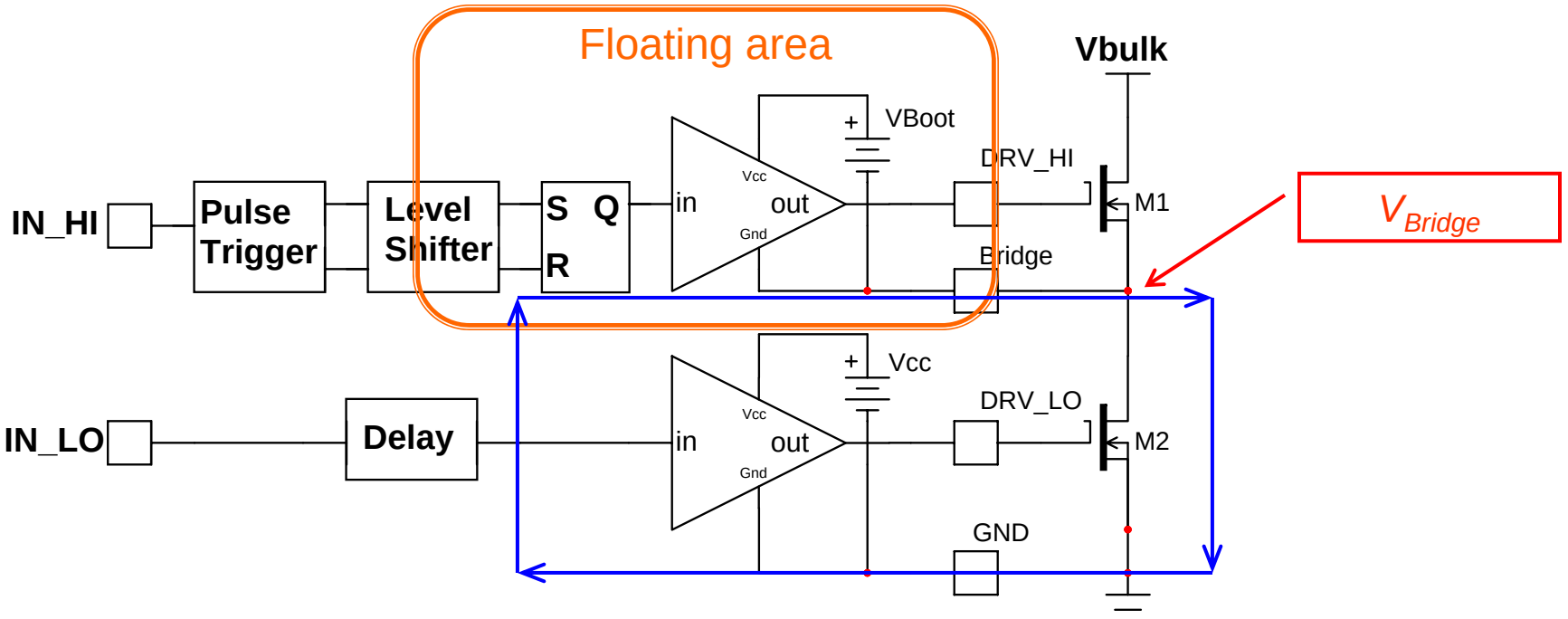
Step 4:

M_1 OFF

M_2 OFF

Bench: Buck Converter Operation

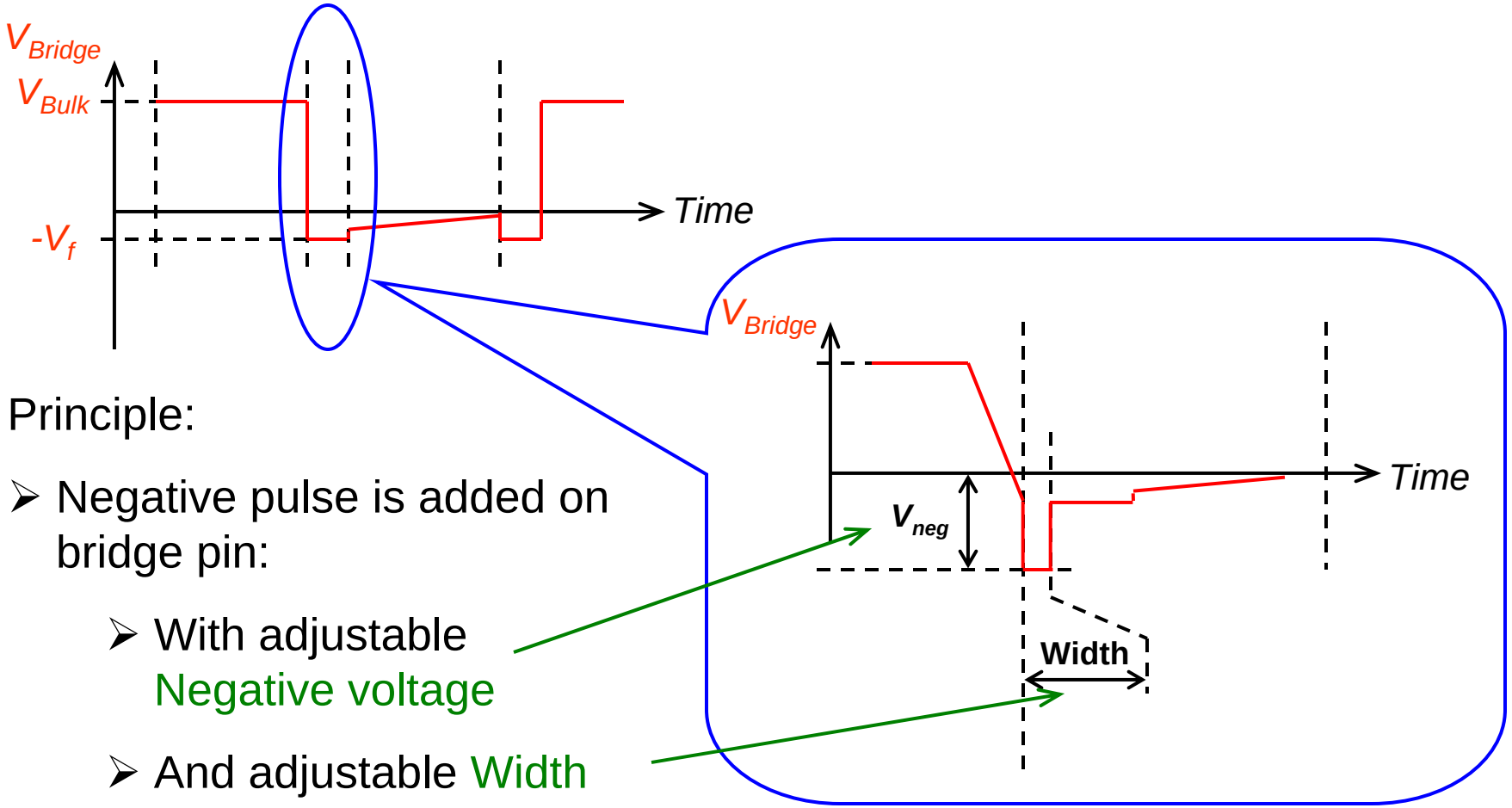
- Negative voltage on bridge pin will create negative current injection inside the IC driver.



Leaky path when $V_{Bridge} < 0V$

This leakage path could create some trouble inside the driver IC.

How to Characterize the Negative Voltage?

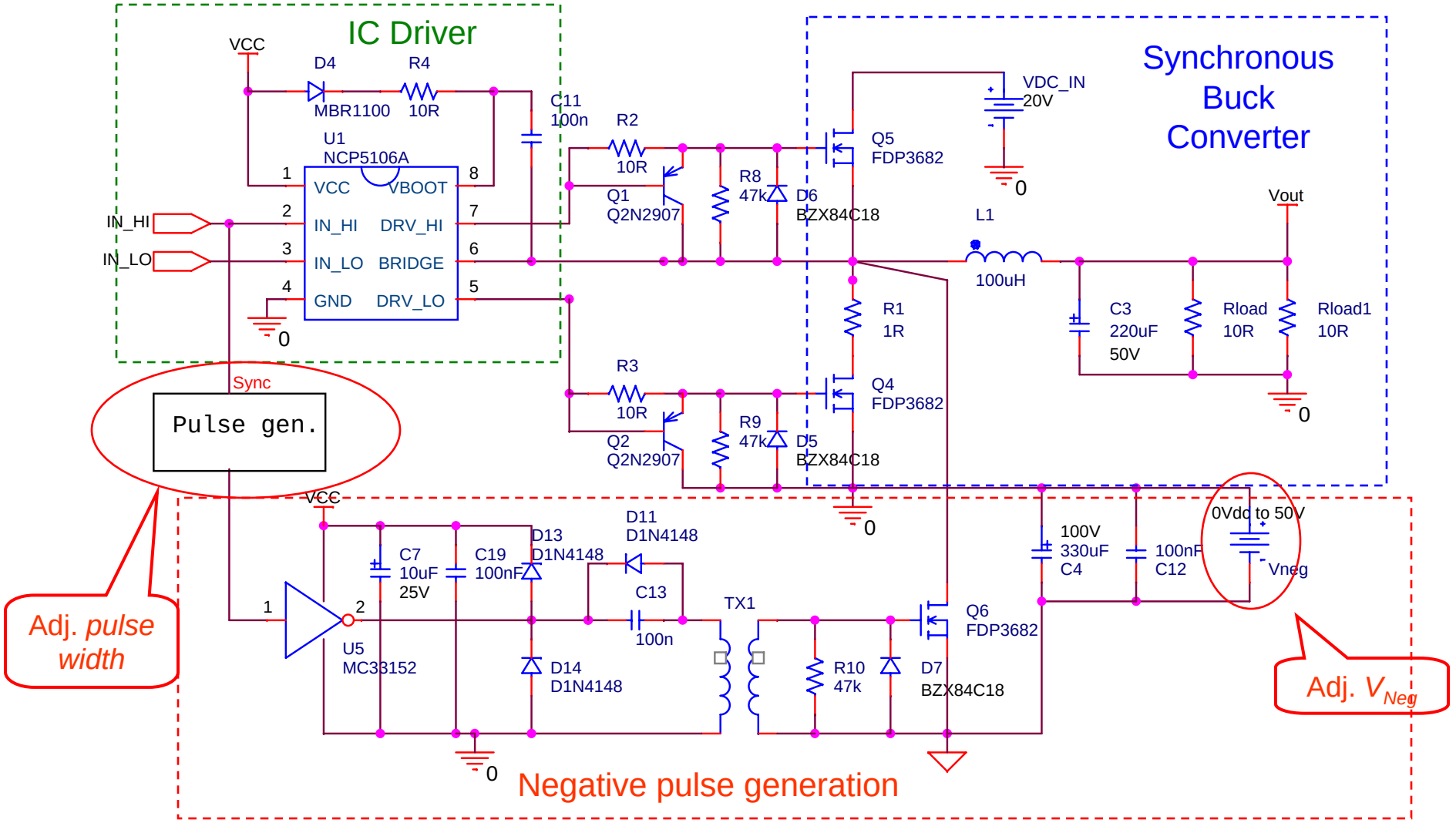


Principle:

- Negative pulse is added on bridge pin:
  - With adjustable Negative voltage
  - And adjustable Width

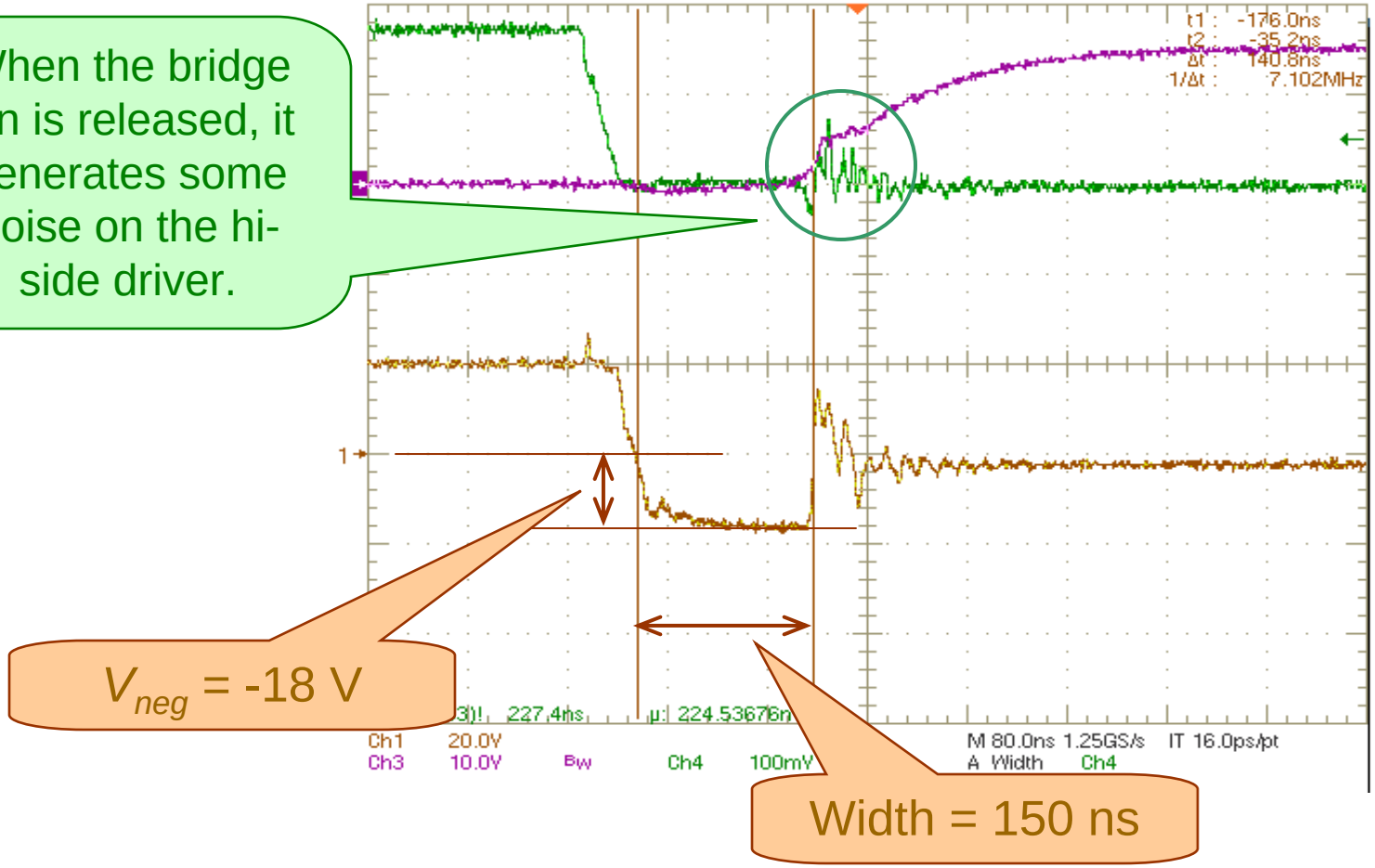
At each pulse width the neg. voltage is increased until the driver IC fails.

How the Negative Voltage has Been Created?



Example of Negative Voltage Measurement

When the bridge pin is released, it generates some noise on the hi-side driver.



V_{neg} = -18 V

Width = 150 ns

VG_LO

(10 V/div)

VG_HI

(10 V/div)

Vbridge pin

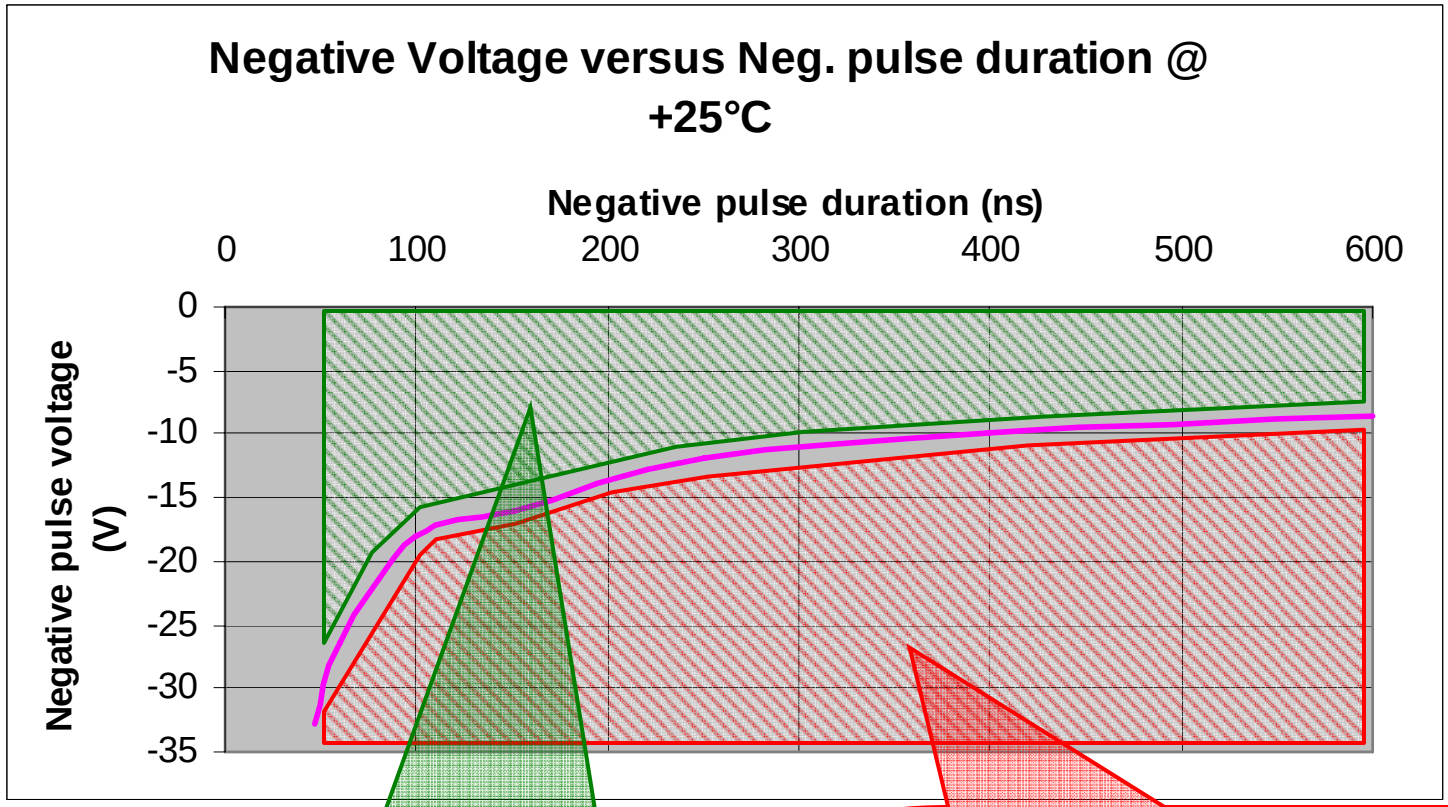
(20 V/div)

Time

(80 ns/div)

Note: Negative voltage pulse is applied when the bridge pin voltage is reaching zero.

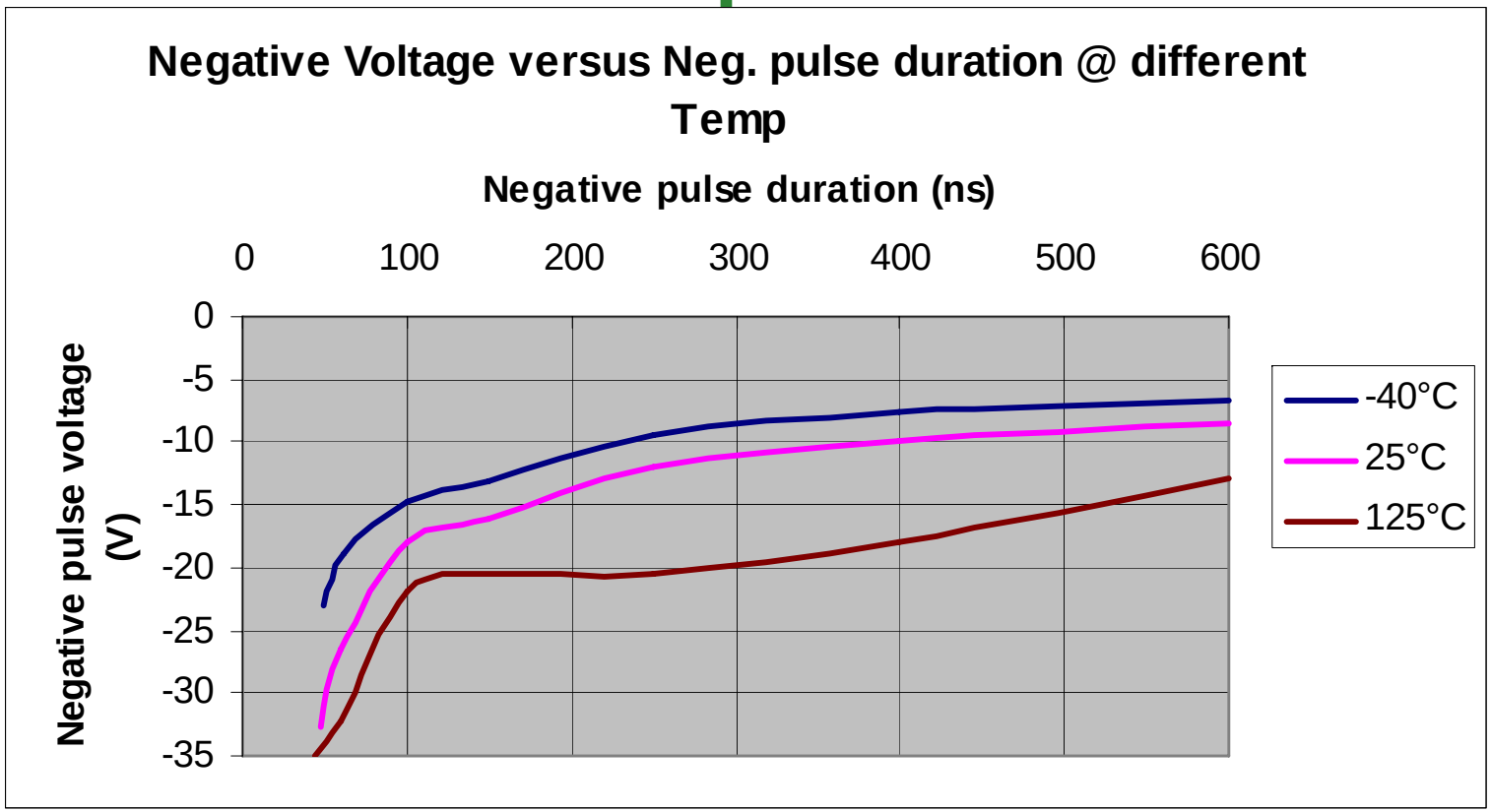
Negative Voltage Characterization



If the negative pulse is inside this area, the driver will work properly.

If the negative pulse is inside this area, the driver will not work properly or can be damaged.

Negative Voltage Characterization in Temperature



- Note: These characterizations will be available in each IC driver datasheet

Driver IC Remarks

- ON Semiconductor defines electrical parameters on overall temperature range (here -40℃ < T_j < +125 ℃). See electrical table & characterization curves.

- Competitors define the electrical parameters only at T_{amb} = +25℃. Temp characterization is not always available

  ➔ what about min & max over extended temperature range?

- The competitors values extracted from the curves probably do not take into account the lot to lot process variations

  ➔ the range variation is probably wider.

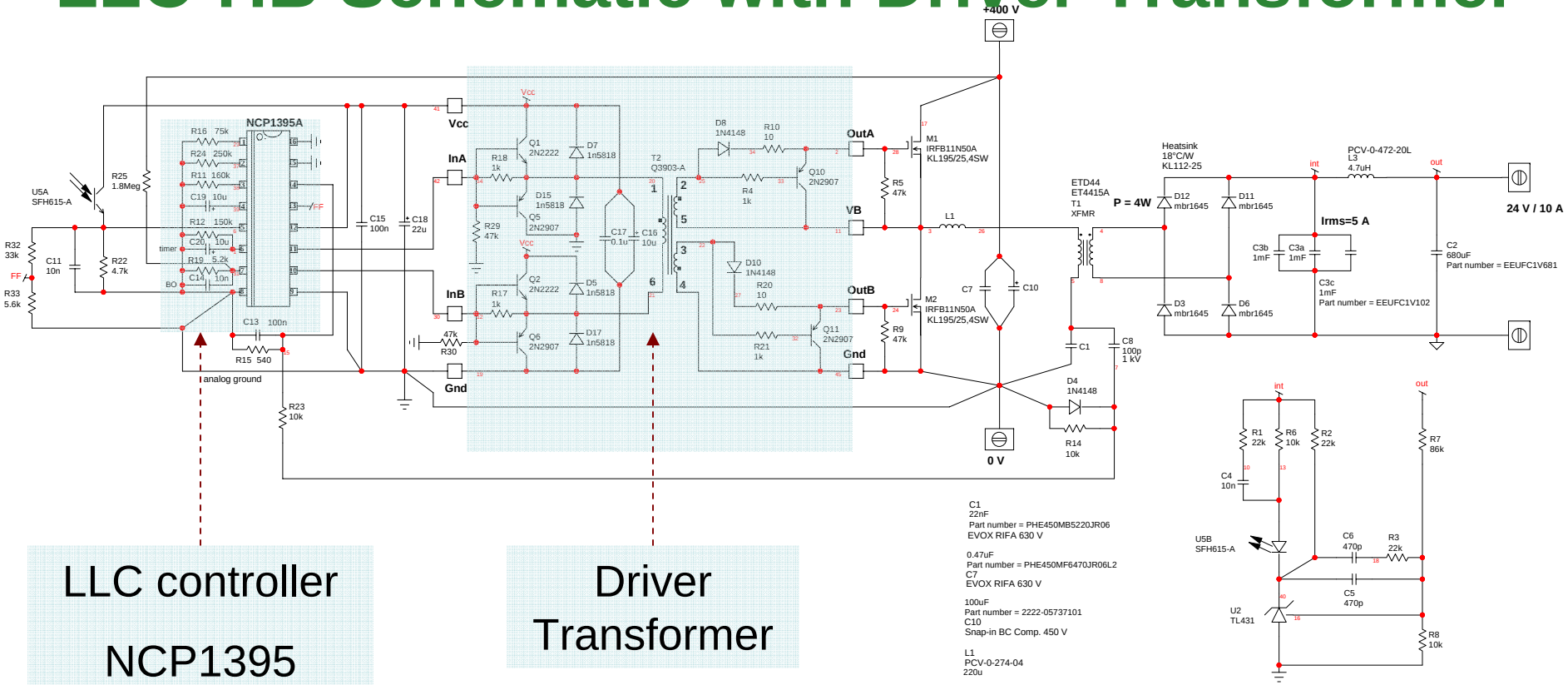
ON Semiconductor IC Driver Cross Reference

	Drive trise / tfall typ. (C_L=1 nF)	Propag. Delay typ. t_{ON} / t_{OFF}	Matching Delay Typ / Max	Cross Conduction Protection	Pin-Out Compati-bility	Remarks
NCP5181	40 ns / 20 ns	100 ns / 100 ns	20 ns / 35 ns	-	IR2181 – IRS2181	•3.3 V CMOS/TTL inputs
NCP5106A	85 ns / 35 ns	100 ns / 100 ns	20 ns / 35 ns	-	IR2106 – IRS2106, FAN7382	•3.3 V CMOS/TTL inputs
NCP5106B	85 ns / 35 ns	100 ns / 100 ns	20 ns / 35 ns	✓	IR2106 – IRS2106, FAN7382	•3.3 V CMOS/TTL inputs •Internal fixed dead time 100 ns
NCP5304	85 ns / 35 ns	100 ns / 100 ns	20 ns / 35 ns	✓	IR2304 - IRS2304, L6388/84 FAN7380	•3.3 V CMOS/TTL inputs •Internal fixed dead time 100 ns
NCP5111	85 ns / 35 ns	750 ns / 100 ns	30 ns / 60 ns	**NA**	IR2111 – IRS2111,	•3.3 V CMOS/TTL input •Internal fixed dead time 650 ns •One pin for creepage
NCP5104	85 ns / 35 ns	620 ns / 100 ns	10 ns /45 ns	**NA**	IR2104 – IRS2104	•3.3 V CMOS/TTL input •Internal fixed dead time 520 ns

Agenda

- Topologies using a half-bridge configuration
- The difference between soft and hard-switching
- The gate-drive transformer
- The all-silicon-solution
- Comparison
- Conclusions

LLC-HB Schematic with Driver Transformer



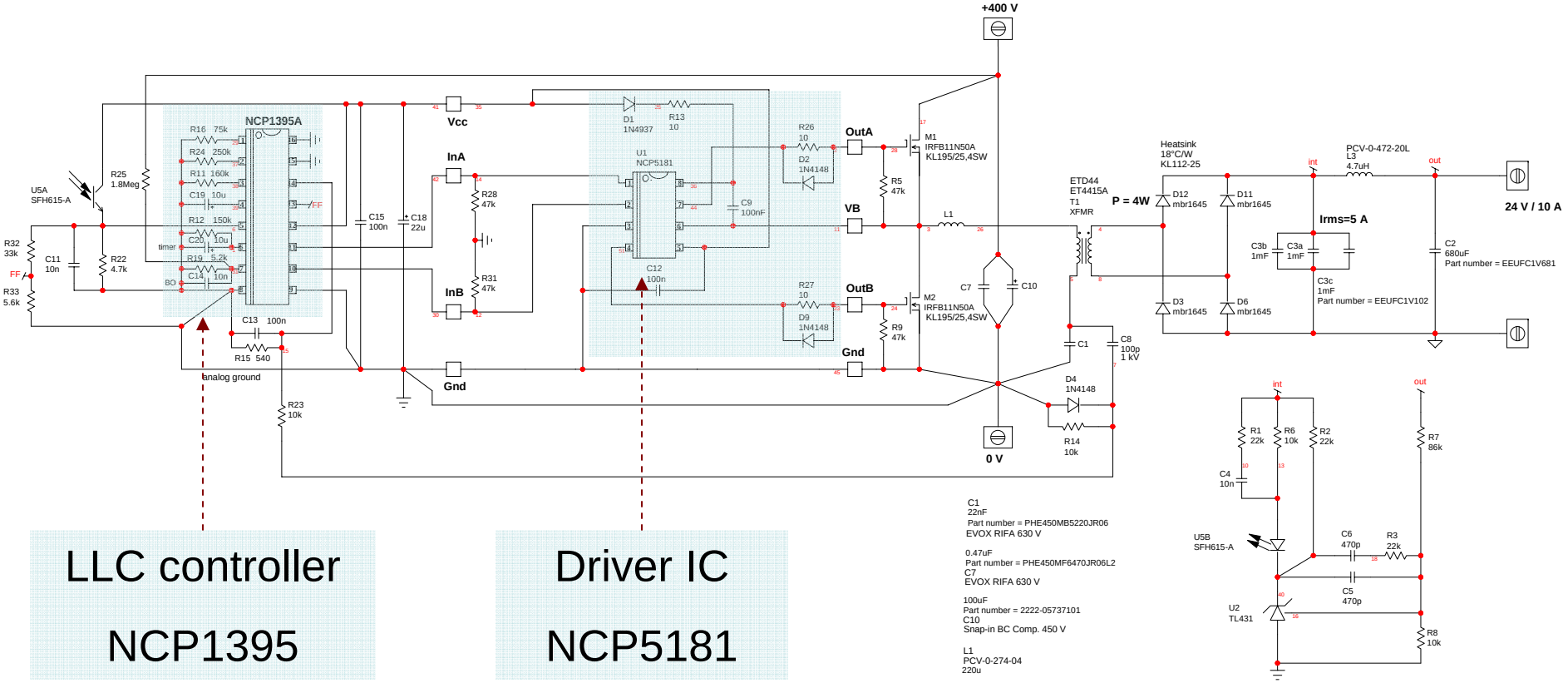
LLC controller

NCP1395

Driver Transformer

- LLC-HB with 24 V @ 10 A
- NCP1395, the LLC controller with dual DRV outputs.
- Transformer drivers the MOSFETs of LLC converter.

LLC-HB Schematic with Driver IC



LLC controller

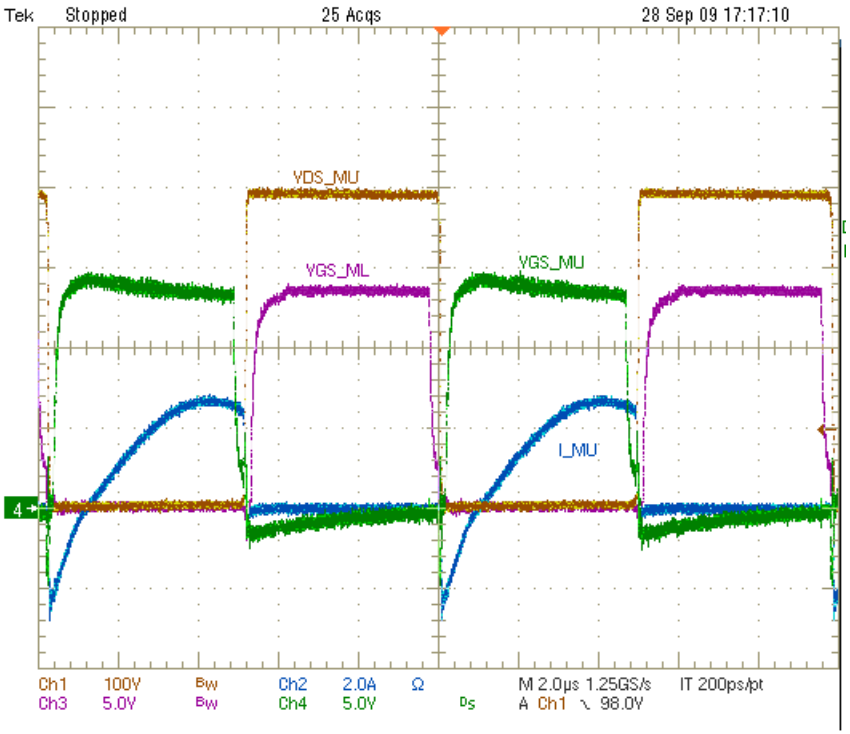
NCP1395

Driver IC

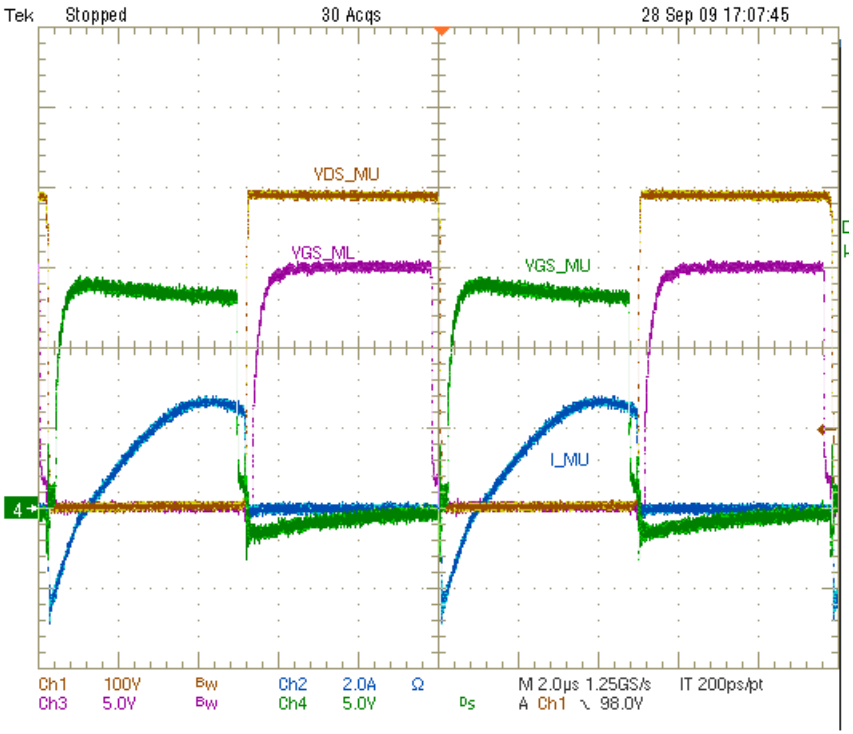
NCP5181

- LLC-HB with 24 V @ 10 A
- NCP1395, the LLC controller with dual DRV outputs.
- NCP5181, driver IC drives the MOSFETs of LLC converter.

V_{GS} Waveform



Driver transformer



Driver IC (NCP5181)

V_{GS_ML} (5 V/div)

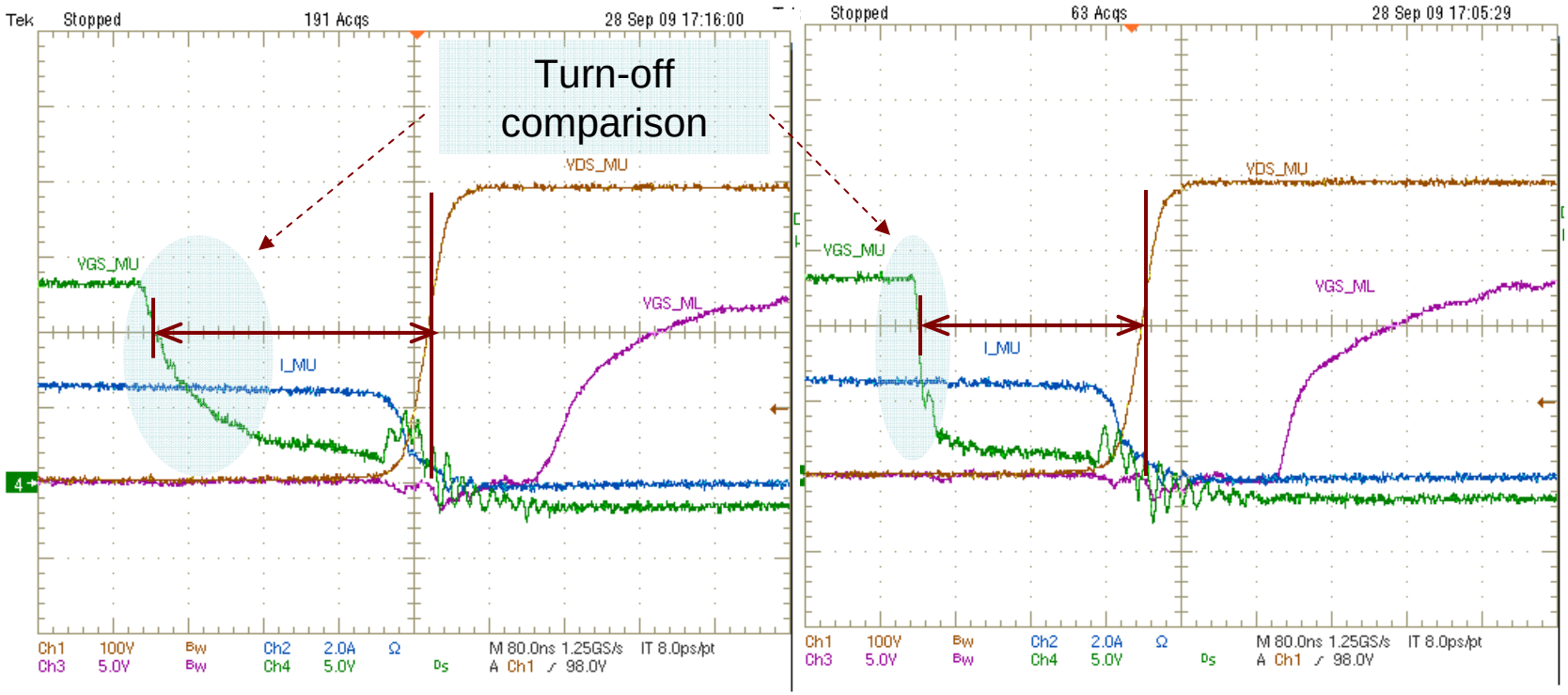
V_{GS_MU} (5 V/div)

I_{MU} (2 A/div)

V_{DS_ML} (100 V/div)

- The waveforms seem similar.

High Side MOSFET Turns Off



80 ns / div

V_{GS_ML} (5 V/div)

V_{GS_MU} (5 V/div)

I_{MU} (2 A/div)

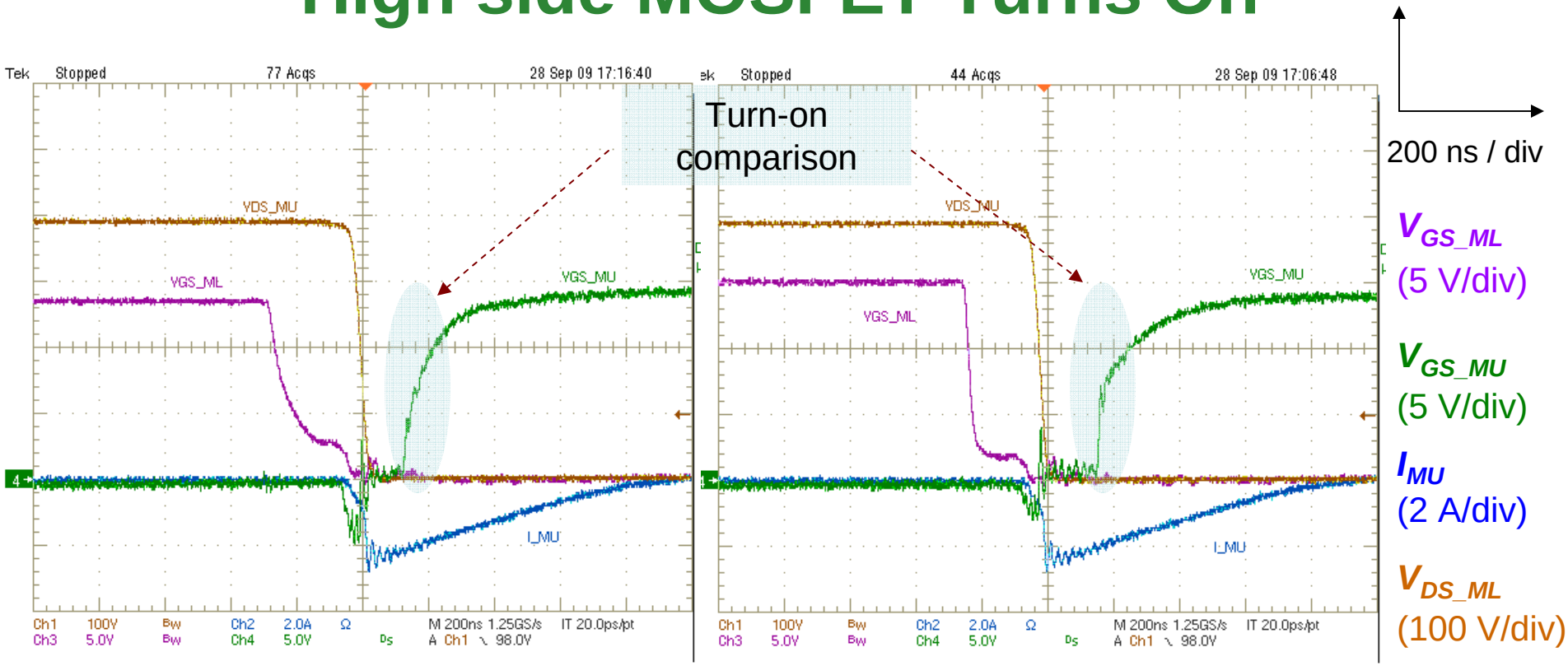
V_{DS_ML} (100 V/div)

Driver transformer

Driver IC (NCP5181)

- The driver IC turns off the MOSFETs more vigorously.
- IC turn-off is 70 ns faster, lowering the switching losses

High side MOSFET Turns On



Driver transformer

Driver IC (NCP5181)

- The driver IC keeps safe and enough dead time between high and low side MOSFETs.

The Efficiency Comparison

	Input power (W)	Output power (W)	*Vout* (V)	*Iout* (A)	η
Driver IC	128.33	119.72	23.96	5.00	93.29%
	257.2	235.46	23.57	9.99	91.55%
Driver Transformer	128.34	119.72	23.96	5.00	93.29%
	258.5	236.46	23.67	9.99	91.48%

- There is no efficiency difference between the IC driver and transformer solutions.

Agenda

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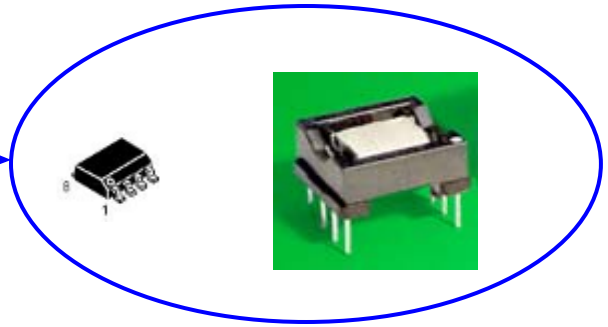
Conclusion: Transformer or IC?

- Both solutions work if well-trimmed.
- We recommend the IC solution because:
  - We don’t sell the transformer.
  - Manual insertion for the transformer.
  - Ease the layout
  - Ease the design
  - Free of transformer problems, e.g.:
    - isolation is destroyed,
    - flux walking away,
    - unexpected ringing after turn off,
    - Height of the transformer in low profile PSU



For More Information

- View the extensive portfolio of power management products from ON Semiconductor at www.onsemi.com
- View reference designs, design notes, and other material supporting the design of highly efficient power supplies at www.onsemi.com/powersupplies