



Is Now Part of



ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

AN-6601

Low Noise JFET Amplifiers

Introduction

Discrete JFETs reign supreme as low noise amplifiers. JFETs are virtually free from the problems of current noise, popcorn noise and limited bandwidth which plague bipolar transistors and bipolar input op amps.

Unfortunately, JFETs are awkward to use because of low gain and the need of extensive biasing networks. However, monolithic op amps are cheap and easy to use but suffer from poor noise performance. By combining JFETs with an op amp yields single and differential input amplifiers that have the best of both worlds; low noise, high gain and ease of use.

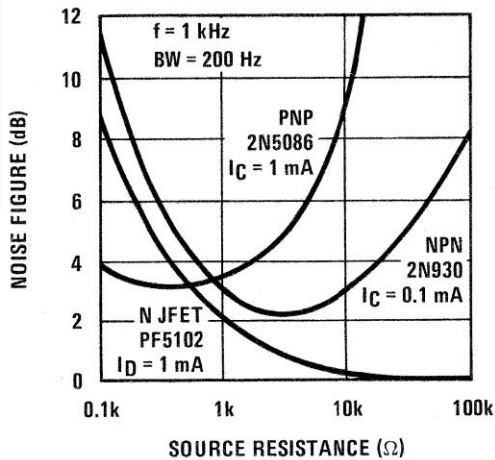


Figure 1. Bipolar and JFET Transistor Noise Comparison

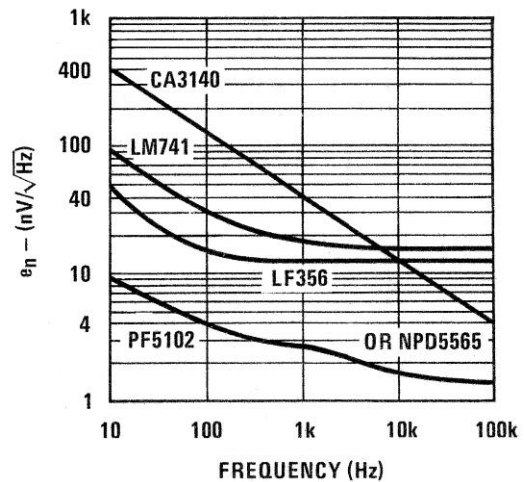
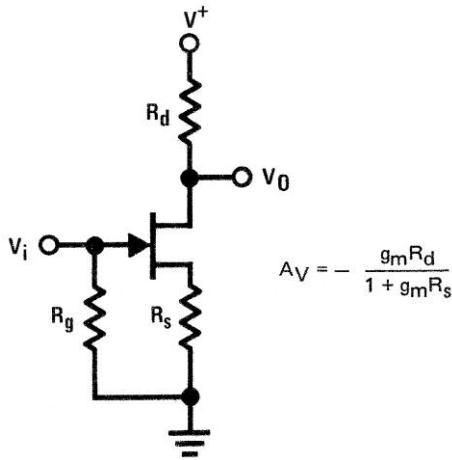
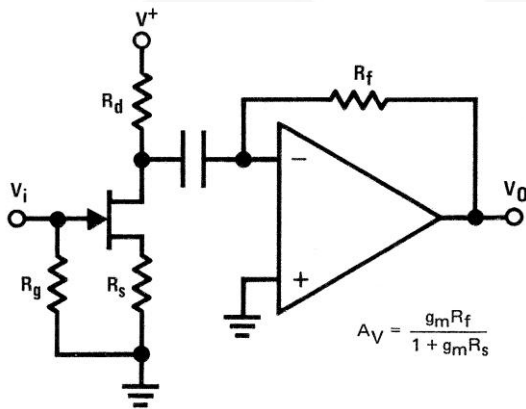


Figure 2. Discrete JFET and Op Amp Noise Comparison

The main problem with JFETs is that the voltage gain is limited by the size of the load resistance which is limited by the power supply voltage and the FET operating current. The voltage gain can be increased by combining the JFET (a transconductance amplifier) with an op amp current to voltage (I/V) amplifier, circumventing the limited load resistor.



Single FET Stage



FET with I/V Amplifier

Figure 3. FET Gain Stages

In the FET/op amp configuration, the FET AC drain current is shunted to the op amp virtual ground and through its feedback resistor, bypassing the FET drain resistor, Rd. The drain resistor is used to bias the FET in a linear region with the feedback resistor, Rf, used to set the gain.

Biasing problems associated with lot and device to device parameter variations are minimized by biasing the source through a large resistor to the negative supply of the op amp. A portion of the source resistor should be unbypassed to minimize gain variations between FETs. From a design standpoint, the maximum AC drain current should be 1/10 of the FET quiescent current for low distortion. The unbypassed portion of the source resistor should be limited to 220 Ω for minimum noise and to increase the op amp feedback resistor (decreased AC current).

Expressions for the single and differential amplifier configurations are needed for optimizing the noise to meet system noise requirements.

Amplifier noise performance is adequately described by modeling the noise sources as a series voltage generator and a shunt current generator with a series voltage generator for the source resistance thermal noise. The thermal noise of a resistor is given by Nyquist's relation and has a spectral density given by $e_n^2 R$ where:

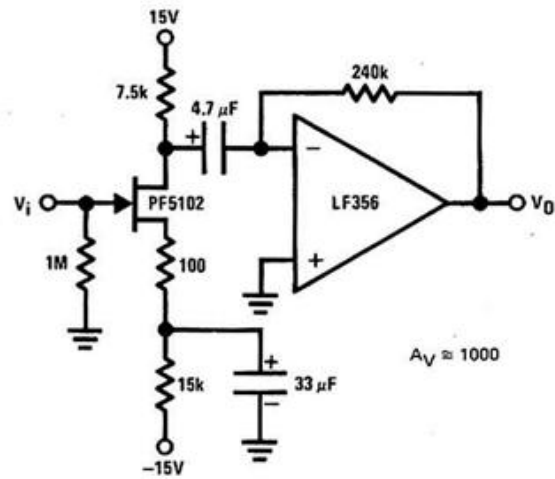
$$e_n^2 R = 4kTR$$

$e_n^2 R$ = mean square noise voltage per unit bandwidth (nV²/Hz)

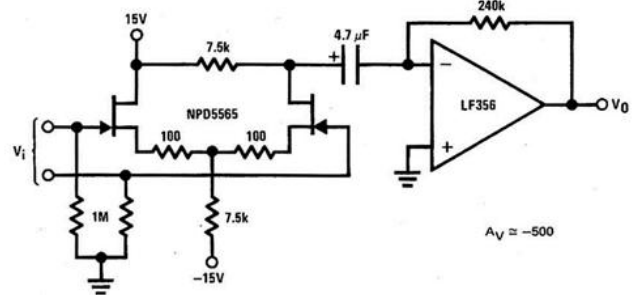
k = Boltzmann constant (1.38 x 10⁻²³ VAS/°K)

T = absolute temperature (°K)

R = resistance (Ω)



Single-Ended



Differential Input

Figure 4. High Gain FET/Op Amp AC Amplifiers

The single ended and differential input amplifier input noise (FET noise current is negligible) is given by the RMS sum of the noise generators.

Single-ended:

$$e_{nt}^2 = e_{nf}^2 + e_{ns}^2 + \left(\frac{1 + g_m R_s}{g_m R_d} \right)^2 (e_{nA}^2 + e_{nR}^2 + i_{nA}^2 R^2)$$

Differential Input:

$$e_{nt}^2 = 2 (e_{nf}^2 + e_{ns}^2) + 4 \left(\frac{1 + g_m R_s}{g_m R_d} \right)^2 (e_{nA}^2 + e_{nR}^2 + i_{nA}^2 R^2)$$

with

e_{nt} = total input noise voltage (nV/ $\sqrt{\text{Hz}}$)

e_{nf} = FET noise voltage (nV/ $\sqrt{\text{Hz}}$)

e_{nA} = op amp noise voltage (nV/ $\sqrt{\text{Hz}}$)

i_{nA} = op amp noise current (pA/ $\sqrt{\text{Hz}}$)

e_{ns} = source resistor thermal noise (nV/ $\sqrt{\text{Hz}}$)

e_{nR} = drain and feedback ($R_d//R_f$) resistor thermal noise (nV/ $\sqrt{\text{Hz}}$)

g_m = FET transconductance at the FET operating current (mmho)

R = parallel resistance of R_d and R_f (Ω)

The differential configuration has higher noise and lower gain than the single-ended version, but is useful when low distortion or balanced inputs are of paramount importance.

The noise of the op amp and the FET drain resistor is reduced by the gain of the FET portion of the amplifier $\frac{g_m R_d}{1 + g_m R_s}$. The noise of the feedback resistor has little effect on the noise but in conjunction with the drain resistor, it can have a dramatic effect on the total circuit noise. The drain resistor is the input leg of an inverting amplifier with the op amp and the feedback resistor. This amplifier has a gain of $-R_f/R_d$ which boosts the op amp noise, limiting the size of R_f to about 390 k.

Practical low noise, high gain AC amplifiers can be built using a low noise JFET and just about any op amp. The op amp needs to meet the slew rate and bandwidth

requirements of the circuit, eliminating selected low noise op amps or complex discrete amplifiers.

A note of caution is in order for the op amp noise. Virtually any JFET input or bipolar input op amp can be used without trouble, but MOSFET input op amps should be avoided. MOSFET 1/f noise is one or more orders of magnitude greater than discrete JFETs, JFET op amps or bipolar input op amps. MOSFETs have 1/f corner frequencies (where the noise power rises as 1/f) starting as high as 100 kHz. The other forms of amplifiers have 1/f corner frequencies of 1 kHz and less. Quite a difference.

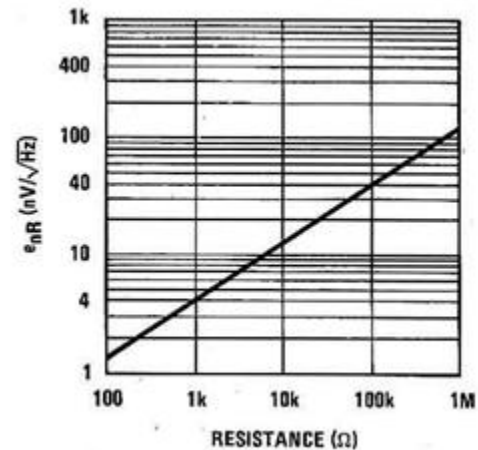


Figure 5. Thermal Noise vs Resistance

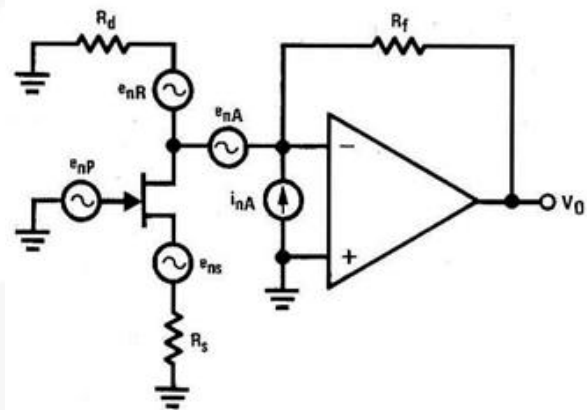


Figure 6. Single-Ended Noise Model

References

- [1] *Aspandiar, Raiyo, "Voids in Solder Joints," SMTA Northwest Meeting, September 21, 2005, Intel Corporation.*
- [2] *Bryant, Keith, "Investigating Voids," Circuits Assembly, June 2004.*
- [3] *Comley, David, et al, "The QFN: Smaller, Faster, Less Expensive," Chip Scale Review.com, August/September 2002.*
- [4] *Englemaier, Werner, "Voids in solder joints-reliability," Global SMT & Package, December 2005.*
- [5] *IPC Solder Products Value Council, "Round Robin Testing and Analysis of Lead Free Solder Pastes with Alloys of Tin, Silver and Copper," 2005.*
- [6] *IPC-A-610-D, "Acceptance of Electronic Assemblies," February 2005.*
- [7] *IPC J-STD-001D, "Requirements for Soldered Electrical and Electronic Assemblies."*
- [8] *IPC-SM-7525A, "Stencil Design Guidelines," May 2000.*
- [9] *JEDEC, JESD22-B102D, "Solderability," VA, Sept. 2004.*
- [10] *Syed, Ahmer, et al, "Board Level Assembly and Reliability Considerations for QFN Type Packages," Amkor Technology, Inc., Chandler, AZ.*

Author: John Maxwell, March 1977

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local
Sales Representative