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Designing a PSR Quasi-Resonant Adaptor Driven by the NCP1362

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APPLICATION NOTE

Quasi−square wave resonant converters also known as Quasi−Resonant (QR) converters are widely used in the adaptor market. They help designing flyback Switched−Mode Power Supply (SMPS) with a reduced Electro−Magnetic Interference (EMI) signature and improved efficiency. However, a major drawback of the structure is that the frequency can become dramatically high at light load.

In traditional QR converters, the frequency is limited by a frequency clamp. But, when the switching frequency of the system reaches the frequency clamp limit, valley jumping occurs: the controller hesitates between two valleys resulting in an instable operation and acoustic noise can be heard in the transformer at medium and light output loads.

In order to overcome this problem, the NCP1362 features a proprietary “valley lockout” circuit: the switching frequency is decreased step by step by changing valley from valley n to valley $(n + 1)$ as the load decreases. Once the controller selects a valley, it stays locked in this valley until the output power changes significantly. This technique extends the QR operation of the system towards lighter loads without degrading the efficiency.

The battery charger market also requests to reduce drastically the size of the adaptor. One of the solutions is to limit the component numbers. Thanks to the NCP1362, also called Primary Side Regulation (PSR) controller, the voltage and current regulation, usually made in a chip placed in the secondary side and communicating via an optocoupler with the primary−side controller, is performed in the primary side thanks to a patented method. All components related to a classical feedback loop (optocoupler, shunt regulator, bridge resistance) are saved and the circuit gains in reliability and assembly costs

This application note focuses on the design of an adapter driven by the NCP1362. The equations developed are further used to build a 12−W adapter.

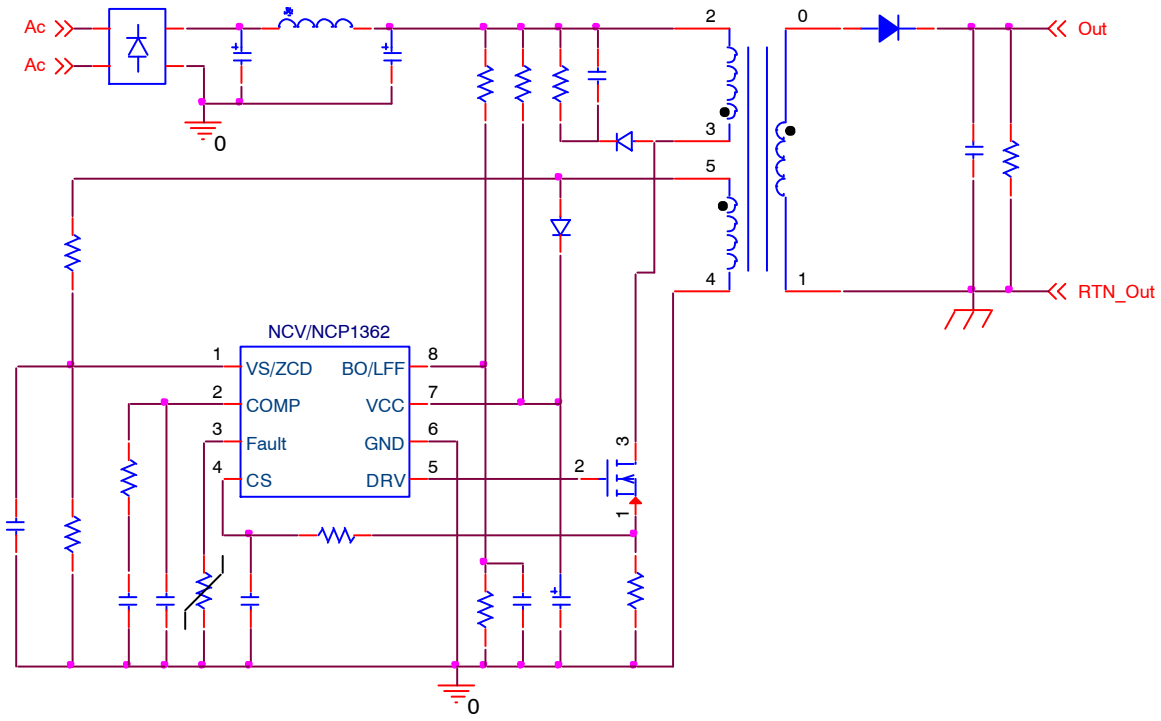

Figure 1. Application Schematic of the 12 W Adapter

Introduction

The NCP1362 is a flyback power supply (PSU) controller providing a means to implement primary side constant−current regulation and secondary side constant−voltage regulation. NCP1362 implements a current−mode architecture operating in quasi−resonant mode. The controller prevents valley−jumping instability and steadily locks out in a selected valley as the power demand goes down. As long as the controller is able to detect a valley, the new cycle or the following drive remain in a valley. Owing to a dedicated valley detection circuitry operating at any line and load conditions, the power supply efficiency will always be optimized. In order to limit a high switching frequency, three clamp options are available.

Quasi−Resonance Current−mode Operation: implementing quasi−resonance operation in peak current−mode control optimizes the efficiency by switching in the valley of the MOSFET drain−source voltage. Thanks to a proprietary circuitry, the controller locks−out in a selected valley and remains locked until the input voltage significantly changes. Only the four first valleys could be locked out. When the load current diminishes, valley switching mode of operation is kept but without valley lock−out. Valley−switching operation across the entire input/output conditions brings efficiency improvement and lets the designer build higher−density converters.

Frequency Clamp: As the frequency is not fixed and dependent on the line, load and transformer specifications, it is important to prevent switching frequency runaway for applications requiring maximum switching frequencies up to 90 kHz or 130 kHz. Three frequency clamp options at 80 kHz, 110 kHz or 140 kHz are available for this purpose. In case frequency clamp is unnecessary, a specific version of the NCP1362 exists in which the clamp is deactivated.

Primary Side Constant Current Regulation: NCP1362 controls and regulates the output current at a constant level regardless of the input and output voltage conditions. This function offers tight over power protection by estimating and limiting the maximum output current from the primary side, without any particular sensor.

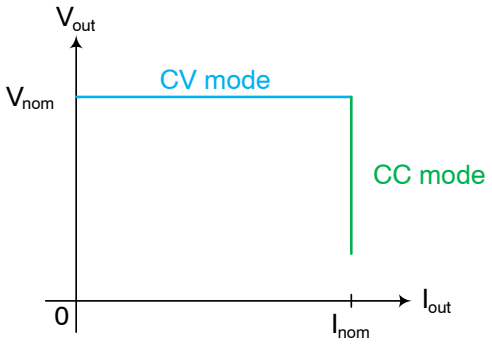

Figure 2. Constant−Voltage & Constant−Current Mode

Soft−Start: A 4−ms internally−fixed soft−start guarantees a peak current starting from zero to its nominal value with a smooth transition. It helps preventing an overstress on the power components at each startup.

Cycle−by−Cycle Peak Current Limit: If the max peak current reaches the V_{ILIM} level, the over current protection timer is enabled and starts counting. If the overload lasts T_{OCP} delay, then the fault is detected and the controller stops immediately driving the power MOSFET. The controller enters in a double hiccup mode before auto−recovering with a new startup cycle.

V_{cc} Over Voltage Protection: If the V_{CC} voltage reaches the $V_{CC(OVP)}$ threshold the controller enters in fault mode. Thus it stops driving pulses on DRV pin: the V_{CC} capacitor is internally discharged to the $V_{CC(Clamp)}$ level with a very low power consumption: the controller is completely disabled. Resuming operation is possible by unplugging the line in order to releasing the internal V_{CC} thyristor with a V_{CC} current lower than the $I_{CC(Clamp)}$.

Winding Short−Circuit Protection: An additional comparator senses the CS signal and stops the controller if V_{CS} reaches V_{ILIM}+50% (after a reduced LEB: t_{LEB2}). Short−circuit protection is enabled only if 4 consecutive pulses reach SCP level. This count prevents any false triggering of short circuit protection during surge test for instance. This fault is detected and operations will be resumed like in a case of V_{cc} Over Voltage Protection.

V_{out} Over Voltage Protection: if the internally−built output voltage becomes higher than the V_{OVP} level (V_{ref_CV1} + 26%) a fault is detected. This fault is detected and operations are resumed like in the *V_{cc} Over Voltage Protection* case.

V_{out} Under Voltage Protection: After each circuit power on sequence, V_{out} UVP detection is enabled only after the startup timer T_{EN_UVP}. This timer ensures that the power supply is able to fuel the output capacitor before checking the output voltage in on target. After this startup blanking time, UVP detection is enabled and monitors the output voltage level. When the power supply is running in constant−current mode and when the output voltage falls below V_{UVP} level, the controller stops sending drive pulses and enters a double hiccup mode before resuming operations.

V_s/ZCD Pin Short Protection: at the beginning of each off−time period, the V_s/ZCD pin is tested to check whether it is shorted or left open. In case a fault is detected, the controller enters in a double hiccup mode before resuming operations.

EMI Jittering: a low−frequency triangular voltage waveform is added to the CS pin. This helps spreading out energy in conducted noise analysis. Jittering is disabled in frequency foldback mode.

Frequency Foldback and Skip Cycle Mode: In frequency foldback mode, the system reduces the switching frequency by adding some dead−time after the 4th valley is detected. The controller will still run in valley switching mode even when the FF is enabled.

Cable Drop Compensation: The cable drop compensation value (for example 300 mV) will be reached at the maximum constant current value. Then the cable compensation is proportional to the output current as illustrated by the following figure.

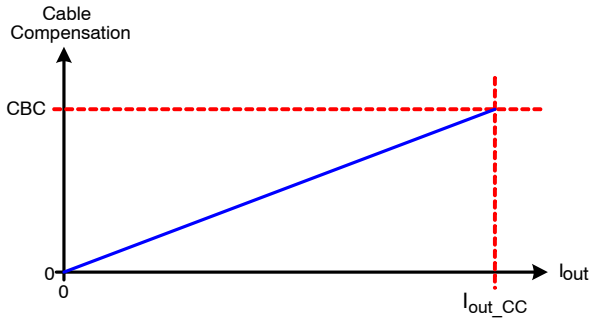

Figure 3. Cable Compensation versus Output Current Load

Temperature Shutdown: if the junction temperature reaches the T_{SHTDN} level, the controller stops driving the power MOSFET until the junction temperature decreases to $T_{SHTDN(off)}$. The operation is then resumed after a double hiccup mode.

POWER STAGE DIMENSIONING

The design of the power stage driven by the PSR controller can be divided in 6 steps:

1. Specification of the Adapter
2. Transformer Design
3. Sense Resistance
4. ZCD Bridge Resistance
5. Secondary−side Components (diode and capacitor)
6. Compensation Network

Step 1: Specification of the Adapter

In order to illustrate this application note, a 12−V/12−W adapter will be the design example.

The specifications are detailed in Table 1.

Table 1. SPECIFICATION OF THE 12 V, 12 W ADAPTER

Parameter	Symbol	Value
Minimum input voltage	$V_{in,min}$	85 V rms
Maximum input voltage	$V_{in,max}$	265 V rms
Output voltage	V_{out}	12 V
Nominal output power	$P_{out(nom)}$	12 W
Switching frequency at $V_{in,min}$, $P_{out(nom)}$	F_{sw}	50 kHz
Efficiency	η	85%
Maximum startup time	$T_{startup}$	< 1 s

Step 2: Transformer Design

The principal component in an adapter is the transformer. The whole structure works around this part so we will start the design with its characteristics. Three mains parameters are needed to define a transformer:

1. Primary to secondary turn ratio (N_{ps})
2. Primary inductance (L_p)
3. Primary to auxiliary winding turns ratio (N_{aux})

Primary to Secondary Turns Ratio (N_{ps})

The turns ratio between the primary and the secondary winding is intimately connected to the maximum MOSFET voltage (BV_{DSS}), the maximum input voltage and the nominal output voltage. The typical drain voltage is shown in Figure 4 for a flyback topology.

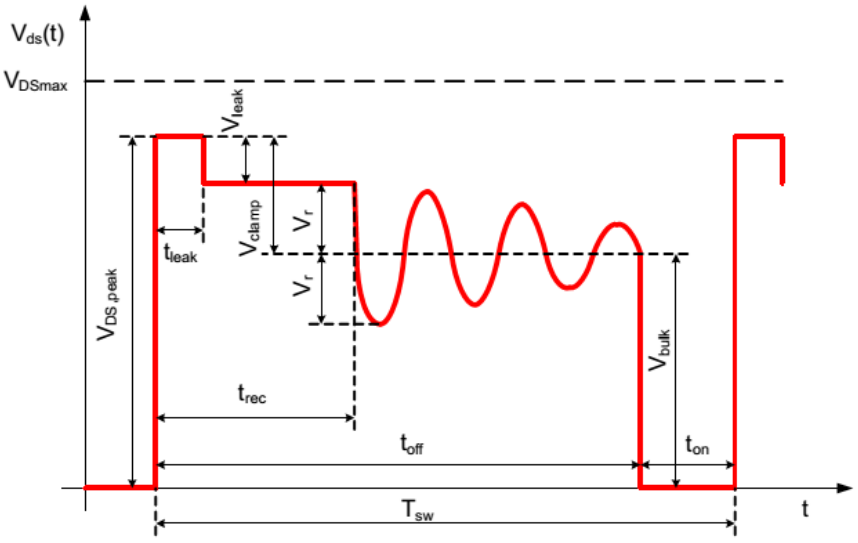

Figure 4. Drain−source MOSFET Voltage

The voltage on the drain pin during the off time is the addition of different parameters. The first contributor is the input voltage (V_{bulk}). Then we have the output voltage reflected on the primary side via the transformer turns ratio (V_r). Finally, the leakage inductance will bring an additional voltage called V_{leak}. Also, due to the slow reaction of the clamping network, another voltage is added (typically V_{os} = 20 V). The addition of these four voltages must remain below the maximum voltage allowed by the MOSFET after applying the choosing derating factor (k_d = 90% generally).

The ratio between the reflected voltage and the clamp voltage is called k_c.

$$k_c = \frac{V_{clamp}}{V_r} \quad \text{(eq. 1)}$$

The selection of k_c depends on design choices. Poorly designed transformers with a large leakage inductance will require a greater k_c coefficient ($k_c > 2$). On the other hand, less than 1% leakage inductance will allow the reduction of the difference between the clamp threshold and the reflected voltage ($1.3 < k_c < 1.5$). In this example we will set $k_c = 1.9$.

Thanks to the above explanation, the turns ratio can be defined by:

$$N_{ps} = \frac{k_c(V_{out} + V_f)}{k_d BV_{DSS} - V_{os} - V_{in\_maxDC}} \quad \text{(eq. 2)}$$

Applying the equation 2 to our adaptor specification:

$$N_{ps} = \frac{1.9(12 + 0.6)}{0.9 \times 650 - 20 - 375} = 0.12 \quad \text{(eq. 3)}$$

Let us pick a turns ratio of 0.123 or $1/N_{ps}$=8.13. In the above equation, we assume the diode forward drop to be 0.6 V.

Primary Peak Current (I_{pk})

Knowing the turns ratio, we are able to determine the primary peak current. The parameter will be needed to set the primary current saturation of the transformer. The worst case will happen when the input voltage is to the minimum level. The lower input voltage is 85 V rms so 120 V dc but, due to the bulk capacitor ripple, the voltage can be lower. The experience shows that, for a 12−W application with a 20−μF bulk capacitor (10 μF // 10 μF), the measured ripple is 45 V.

The minimum input voltage will be:

$$V_{min} = V_{in\_min}\sqrt{2} - V_{ripple} = 85\sqrt{2} - 45 = 75\ V \quad \text{(eq. 4)}$$

Now, we have the all necessary data to evaluate the maximum primary peak current:

$$I_{pk,pri} = \frac{2P_{out}}{\eta}\left(\frac{1}{V_{min}} + \frac{N_{ps}}{V_{out} + V_f}\right) + \pi\sqrt{\frac{2P_{out}(C_{OSS} + C_{DS})f_{sw}}{\eta}} \quad \text{(eq. 5)}$$

Where C_{OSS} is the MOSFET output capacitance and C_{DS} the optional added capacitor in parallel with the Drain−Source.

Applying eq.5 to our adapter specification:

$$I_{pk,pri} = \frac{2 \times 12}{0.85}\left(\frac{1}{75} + \frac{0.123}{12 + 0.6}\right) + \pi\sqrt{\frac{2 \times 12\ (38n + 0)\ 50k}{0.85}} = 0.67\ A \quad \text{(eq. 6)}$$

Primary Inductance (L_p)

The traditional formula to calculate the output power for a Flyback topology is:

$$P_{out} = \frac{1}{2} L_p I_{pk,pri}^{\ 2} f_{sw} \eta \quad \text{(eq. 7)}$$

By rearranging eq.7, the primary inductance can be extracted:

$$L_p = \frac{2P_{out}}{I_{pk,pri}^{\ 2} \eta f_{sw}} \quad \text{(eq. 8)}$$

$$L_p = \frac{2 \times 12}{0.67^2 \times 0.85 \times 50k} = 1.24\ mH \quad \text{(eq. 9)}$$

Primary to Auxiliary Winding Turns Ratio (N_{aux})

The last parameter that has to be defined relates to the transformer turns ratio affecting the primary and the auxiliary windings. The turns ratio is chosen in order to have the right supply voltage for the controller regardless of operating conditions. Due to the leakage inductance, the voltage on the V_{cc} pin will be higher when the power supply (PSU) operates at full load compared to the level in stand−by mode. In this last case, the part works at the minimum switching frequency (i.e. 1 kHz) so the duration between each cycle is longer. Also, due to the low frozen peak current, the energy stored in the transformer during the on−time is reduced and the demagnetization time will be narrow. The V_{cc} capacitor refresh will be limited. The auxiliary winding will thus be defined to have enough voltage in no−load condition to supply the controller and have some margins regarding the UVLO threshold (i.e. 6.5 V typ.).

Also, the V_{cc} voltage excursion must remain reasonable otherwise the stand−by performance will be affected by the driver stage power dissipation. In a no−load condition, the MOSFET peak current during the on−time is limited so there is no need to have a strong gate−source voltage (at 12−13 V).

Accounting for all these criteria, a good trade−off for this controller is to set the V_{cc} voltage around 8 V in no−load condition.

$$N_{aux} = \frac{N_{ps}(V_{cc} + V_{f,aux})}{V_{out} + V_f} \quad \text{(eq. 10)}$$

Where V_f is the forward voltage of the secondary diode and $V_{f,aux}$ the forward voltage of the V_{cc} diode.

The turns ratio between the primary and the auxiliary winding should be:

$$N_{aux} = \frac{0.123 \times (8 + 0.6)}{12 + 0.6} = 0.086 \quad \text{(eq. 11)}$$

The four mains transformer characteristics have been calculated in the above section:

1. Primary to secondary turns ratio
2. Primary to auxiliary turns ratio
3. Primary current saturation
4. Primary inductance

Step 3: Sense Resistance

Another key component for the primary−side constant current regulation (CC) patented by ON Semiconductor is the sense resistance.

The controller is able to reconstruct the output current by sensing two parameters:

1. The primary current through the CS pin voltage
2. The demagnetization time thanks to the auxiliary winding

The leakage inductance brings an error in the CC regulation. The primary current negative slope at turn−off is reduced as depicted in the Figure 5. The consequence is that the secondary peak current is lower than expected:

$$I_{pk,sec} < \frac{I_{pk,pri}}{N_{ps}} \quad \text{(eq. 12)}$$

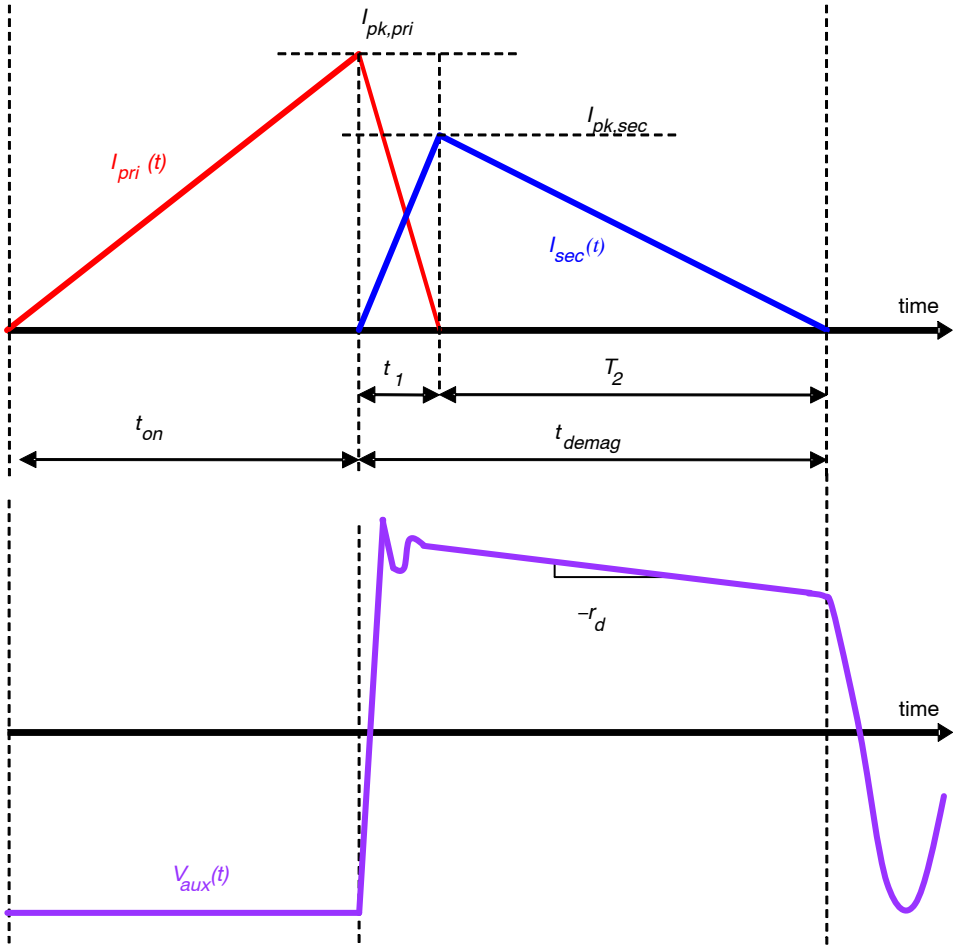

Figure 5. The Ripple Voltage during the Off−time is Mainly Dictated by the Diode Dynamic Resistance r_d

Thanks to its internal constant−current block, the controller accounts for the leakage inductance effect and forces a constant output current with a value defined by:

$$I_{out} = \frac{V_{Ref\_CC}}{2K_{comp}N_{ps}R_{sense}} \quad \text{(eq. 13)}$$

NOTE: In this formula, V_{Ref_CC} is the internal voltage reference for the CC regulation.

The output current limit is set by choosing the sense resistance:

$$R_{sense} = \frac{V_{ref\_CC}}{2K_{comp}N_{ps}I_{out}} \quad \text{(eq. 14)}$$

The internal reference voltage V_{ref_CC} is 1 V and the K_{comp} divider is 4.25. For the 12−V/12−W application, the nominal output current will be 1 A. Applying a 10% margin, the sense resistance should be:

$$R_{sense} = \frac{1}{2 \times 4.25 \times 0.123 \times 1.1} = 0.869\ \Omega \quad \text{(eq. 15)}$$

Step 4: ZCD Resistive Bridge

When the load is below the maximum threshold allowed by the CC loop, the controller operates in constant voltage (CV) regulation. How is the CV regulation implemented for this controller?

When the energy stored in the transformer is delivered to the secondary during the demagnetization time, the auxiliary voltage is the sum of the output voltage scaled by the auxiliary to secondary turns ratio and the secondary

forward diode voltage. This secondary forward diode voltage could be split in two elements: the first one is the forward voltage of the diode (V_{T0}) and the second is related to the dynamic resistance of the diode multiplied by the secondary current ($r_d \cdot i_{sec}(t)$). The illustration of the dynamic resistance can be seen in Figure 5. This second term, especially the secondary current, will depend on the load and line conditions.

To reach an accurate primary−side constant−voltage regulation, the controller detects the end of the demagnetization time and precisely samples the output voltage level seen on the auxiliary winding. Because this moment coincides with a secondary−side current equal to zero, the diode forward voltage drop becomes independent from the loading conditions.

$$V_{aux} = \frac{N_{aux}}{N_{ps}} \left(V_{out} + V_{fo}\right) \qquad \text{(eq. 16)}$$

The internal reference voltage for the CV regulation is 2.5 V. We already defined the auxiliary winding (step 1) to deliver 8 V when the output voltage is regulated to 12 V. A resistor divider has to be added to set 2.5 V on the ZCD pin when the output voltage is regulated to 12 V, the nominal voltage.

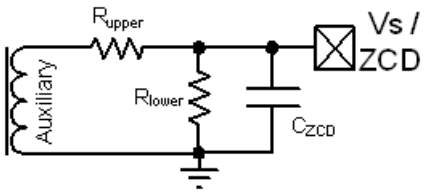

Figure 6. ZCD Pin Network

Let's arbitrarily fix the upper resistance to 10 kΩ. According to the internal voltage reference V_{ref_CV}, the lower resistor will be:

$$R_{lower} = \frac{V_{ref\_CV}}{V_{aux} - V_{ref\_CV}} R_{upper} \qquad \text{(eq. 17)}$$

$$R_{lower} = \frac{2.5}{8.0 - 2.5} \times 10k = 4.5\ k\Omega \qquad \text{(eq. 18)}$$

These resistances have to be adjusted in the laboratory to obtain the exact output voltage value.

The capacitor C_{ZCD}, connected in parallel to the pull−down resistor offers a way to delay the MOSFET turn−on event and exactly switch in the minimum of the drain−source voltage: switching losses are greatly reduced in this case.

Please note that this capacitor must be of reasonable value to keep a good accuracy on the CV regulation in stand−by mode when the demagnetization time is really limited. The maximum recommended time constant τ is around 300 ns.

We can deduce the ZCD capacitor:

$$C_{ZCD} \leq \frac{R_{upper} + R_{lower}}{R_{upper}\, R_{lower}} \tau \qquad \text{(eq. 19)}$$

In our application, the capacitor on the ZCD pin must be below:

$$C_{ZCD} \leq \frac{10k + 4.5k}{10k \times 4.5k}\ 300n \leq 97\ nF \qquad \text{(eq. 20)}$$

Step 5: Secondary Side Components

The component count in the secondary is limited owing to the PSR topology. In a classical application, an optocoupler with a voltage reference (TL431) are needed. In our case, these components are saved, only the power parts are inserted like the output rectifier diode and capacitor.

Output rectifier

Let's talk about the output rectifier. Two parameters will help choosing this diode. The first one is the maximum peak repetitive reverse voltage noted V_{RRM}. The second one is related to the power dissipation at the nominal output power. Indeed, as explained above, the forward voltage can be expressed by:

$$V_f = V_{T0} + r_d\, I_d \qquad \text{(eq. 21)}$$

The power dissipated by the diode will be:

$$P_d = V_{T0}\, I_{out} + r_d\, I_{rms,sec}^{\ 2} \qquad \text{(eq. 22)}$$

This equation highlights the impact of the dynamic resistance (r_d) and the forward voltage without current (V_{T0}).

We will compare two different diodes and see the power dissipation in our application. The first diode will be a classical Schottky diode, MBR5100MFS. This diode will be compared to the trench−based diode (NRVTSS5100E). One of the advantages of this second diode is a lower forward voltage. Both diodes see an average current to 5 A. The characterization curves help us to extract r_d and V_{T0}.

In our application according to the transformer specification, the secondary rms current will be 1.4 A for the worst case. By doing the ΔV over ΔI around the operating current (the nominal I_{out}), the dynamic resistance is defined. We took the 125°C curve to be as closed as possible to the normal condition when the ambient temperature is above 50°C.

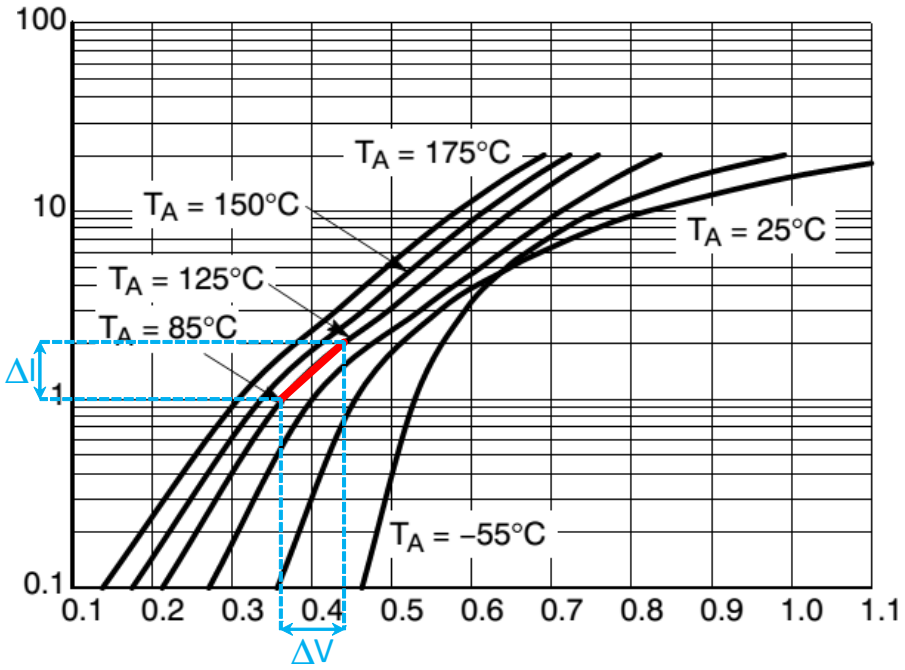

Figure 7. V_f vs. I_f for NRVTSS5100E

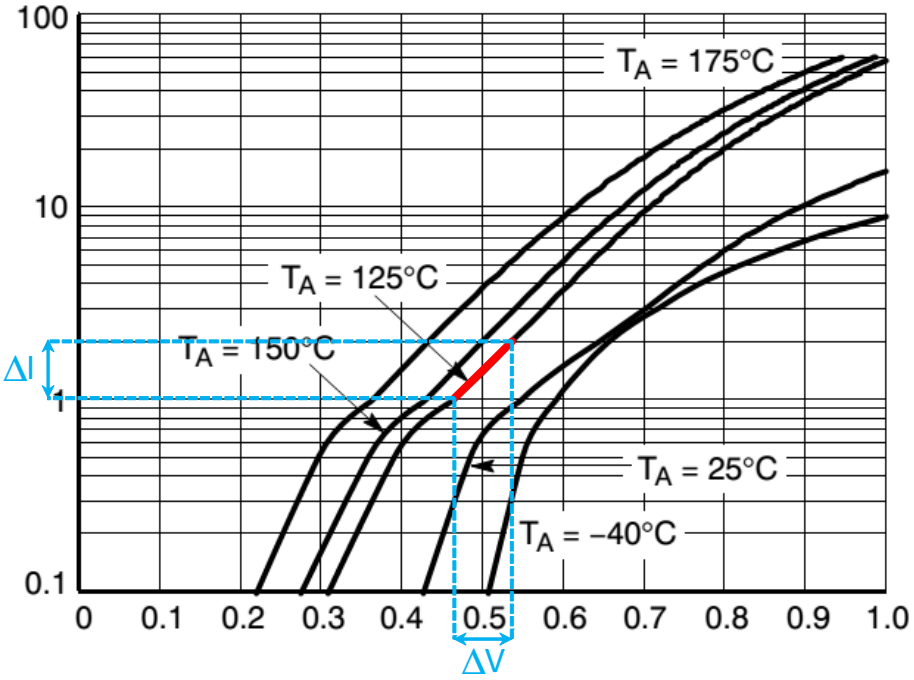

Figure 8. V_f vs. I_f for MBR5100MFS

Table 2. COMPARISON BETWEEN NRVTSS5100E AND MBR5100MFS

Parameters @ 125°C	NRVTSS5100E	MBR5100MFS
V_{f0}	0.21 V	0.31 V
r_d around 1.4 A	90 mΩ	80 mΩ
P_d (eq. 22)	0.386 W	0.467 W

By choosing a diode with a lower forward voltage (and the same average current), the losses can be reduced by almost 20%.

Now, why a 100−V breakdown voltage has been used for the comparison?

This parameter is mostly dependent from the transformer turns ratio and the maximum input voltage. The Peak Inverse Voltage (PIV) is defined by:

$$PIV = N_{ps} V_{in,maxdc} + V_{out} \quad \text{(eq. 23)}$$

Applying to our case:

$$PIV = 0.123 \times 265\sqrt{2} + 12 = 58\ V \quad \text{(eq. 24)}$$

Due to the leakage inductance, some oscillations can occur at the MOSFET turn−off event so, including some margins, a 100−V maximum reverse voltage is the right choice.

Output Capacitor

The output capacitor is the second component on the secondary side. Combined to the output diode, it contributes to absorb the ac current delivered by the transformer while the dc component is transmitted to the load.

For a classical flyback topology, the output capacitor C_{out} is selected to accept the adequate rms current (1.4 A in our application) and to limit the undershoot ΔV when the output is subjected to a current step ΔI.

The undershoot depth can be divided in two parts:

1. The drop related to the Equivalent Series Resistance (ESR) of the capacitor.
2. The drop related to the closed−loop operation of the converter. Considering a bandwidth f_c, it can be evaluated via the following formula:

$$\Delta V \approx \Delta I \cdot f_c \cdot C_{out} \quad \text{(eq. 25)}$$

The typical undershoot during a step load is depicted in the Figure 9.

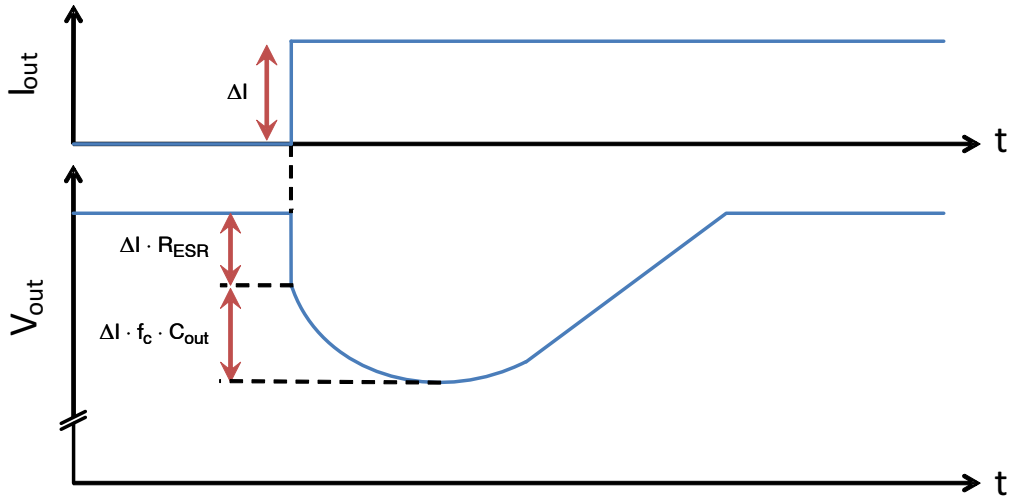

Figure 9. The Typical Response of a Flyback Converter operated in a Closed−loop Condition

An undershoot corresponding to 5% of the output voltage (i.e. 12 V) allows a drop voltage to 600 mV.

For a PSR Flyback application, another parameter has to be considered. Because the output voltage is not directly sensed, the controller limits the minimum switching frequency to 1 kHz in no load condition to have an acceptable step load response.

Indeed, the main limitation of the PSR with the F_{min} is the step load answer. As explained in the datasheet, the output voltage is read on the auxiliary winding at the end of the demagnetization time. Between two cycles, the internal feedback loop is not refreshed so if the step load is applied, the primary controller will not be able to react until 1 ms for the worst case (1 kHz period).

Taking in account this behaviour, the ESR impact can be negligible as shown in Figure 10.

$$\Delta I \cdot R_{ESR} << \frac{\Delta I \cdot t_r}{C_{out}} \quad \text{(eq. 26)}$$

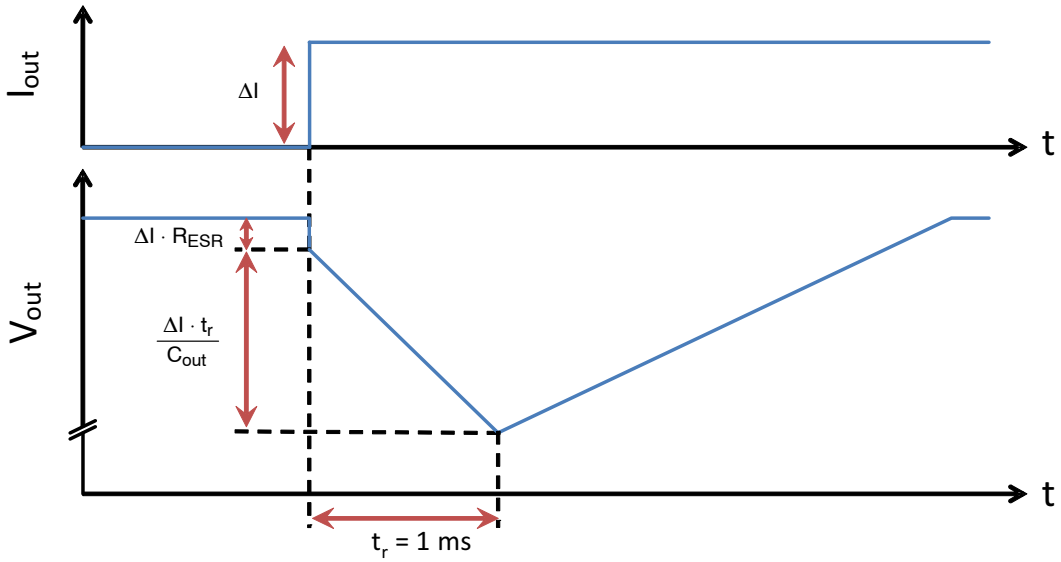

Figure 10. Typical PSR Flyback Output Voltage during a Step Load

Following the above explanation, if we want to limit the undershoot below a 5% deviation, the output capacitor should be:

$$C_{out} = \frac{\Delta I \cdot t_r}{\Delta V} = \frac{1\ A \times 1\ ms}{5\% \times 12\ V} = 1.66\ mF \qquad \text{(eq. 27)}$$

By adding a dummy load on the output, the minimum switching frequency can be increased from 1 kHz to 3 kHz for instance. Thanks to this additional SMD resistance, the output capacitor can be reduced to:

$$C_{out} = \frac{1\ A \times 0.33\ ms}{5\% \times 12\ V} = 550\ \mu F \qquad \text{(eq. 28)}$$

Step 6: Compensation Network

The PSR controller needs a type 2 compensation to ensure stability. The type 2 has two additional components (a series RC network is added in parallel with a capacitor) compared to the type 1 network. These parts will be needed to implement phase boost at the selected crossover frequency.

All equations related to the power stage with the internal patented implementation have been defined and can be found in the Mathcad spreadsheet (reference [5]). The reference [6] give also the explanation of these formula. From these both references, we can now extract the compensation network values according to the needed Phase Margin (PM) and the Crossover Frequency (F_c).

For our 12−V / 12−W demoboard, the type 2 compensator looks like:

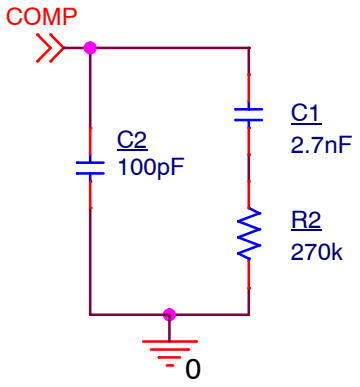

Figure 11. Type 2 Compensation

Conclusion

This paper summarizes the key steps when dimensioning a NCP1362 PSR flyback demonstration board. The proposed approach being systematic, it can be easily applied to other applications. All the equations (and more) presented have been implemented inside a Mathcad® spreadsheet that can be downloaded from our website [5].

The process has been illustrated by the example of the 12−W, 12−V output voltage wide−mains evaluation board. You can find the experimental results of the 12−W adapter in the “A 12 W adaptor with NCP1362 Quasi resonant controller” [3]. Implementation details (Schematic, BOM, GERBER file...) can be found on our web site [4].

More details on the circuit operation can be found in its data sheet [2].

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